DSPIS

Serial Peripheral Interface –Slave

ver 1.05

OVERVIEW

The DSPIS is a fully configurable SPI ma slave device, designated to operate with passive devices like memories, LCD drivers etc. The DSPIS allows user to configure polarity and phase of serial clock signal SCK.

A serial clock line (SCK) synchronizes shifting and sampling of the information on the two independent serial data lines. DSPIS data are simultaneously transmitted and received.

The DSPIS system is flexible enough to interface directly with numerous standard product peripherals from several manufacturers. Data rates as high as CLK/4. Clock control logic allows a selection of clock polarity and a choice of two fundamentally different clocking protocols to accommodate most available synchronous serial peripheral devices.

The DSPIS allows the SPI Master to communicate with passive devices. When transmission starts (SS Line goes low) the first portion of data is copied to the address register and then to the ADDRESS bus output, after transmission of the address the DSPIS generates the read signal (RD) and copy DATAI bus contents to the transmitter shift register, and prepare data to be exchanged with SPI Master. During the next data portion transmission DSPIS simultaneously transmits data out and in. When the first data portion is received the DSPIS asserts DATAO bus generates the write signal (WE), then increments ADDRESS bus performs a read operation and prepare another data portion to be exchanged with SPI master. Transmission is ended when the SS line goes high.

The DSPIS is a technology independent design that can be implemented in a variety of process technologies.

DSPIS is **fully customizable**, which means it is delivered in the exact configuration to meet users' requirements. *There is no need to pay extra for not used features and wasted silicon.* It includes **fully automated testbench** with **complete set of tests** allowing easy package validation at each stage of SoC design flow.

APPLICATIONS

- Embedded microprocessor boards
- Consumer and professional audio/video
- Home and automotive radio
- Digital multimeters

http://www.DigitalCoreDesign.com
http://www.dcd.pl

KEY FEATURES

- SPI Slave
  - *Slave operation*
  - *Automatic read and write operations*
  - *Automatic address incrementation after any data portion transfer*
  - *Configurable address and data length.*
  - *Configurable SCK phase and polarity.*
  - *Supports speeds up ¼ of system clock*
  - *Simple interface allows easy connection to passive devices, and SPI Master*
- Fully synthesizable, static synchronous design with no internal tri-states

DELIVERABLES

- Source code:
  - VHDL Source Code or/and
  - VERILOG Source Code or/and
  - Encrypted, or plain text EDIF netlist
- VHDL & VERILOG test bench environment
  - Active-HDL automatic simulation macros
  - ModelSim automatic simulation macros
  - Tests with reference responses
- Technical documentation
  - Installation notes
  - HDL core specification
  - Datasheet
- Synthesis scripts
- Example application
- Technical support
  - IP Core implementation support
  - 3 months maintenance
    - Delivery the IP Core updates, minor and major versions changes
    - Delivery the documentation updates
    - Phone & email support

LICENSING

Comprehensible and clearly defined licensing methods without royalty fees make using of IP Core easy and simply.

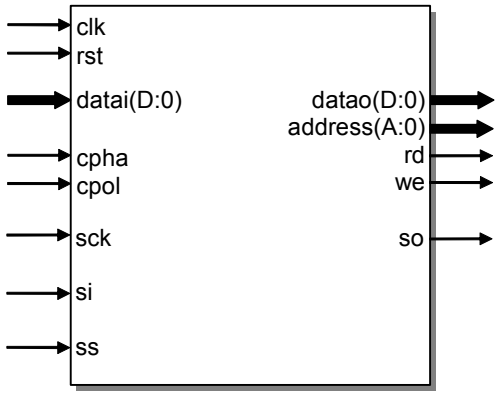
Single Design license allows use IP Core in single FPGA bitstream and ASIC implementation.

Unlimited Designs, *One Year* licenses allow use IP Core in unlimited number of FPGA bitstreams and ASIC implementations.

In all cases number of IP Core instantiations within a design, and number of manufactured chips are unlimited. There is no time restriction except *One Year* license where time of use is limited to 12 months.

- Single Design license for
  - *VHDL, Verilog source code called HDL Source*
  - *Encrypted, or plain text EDIF called Netlist*
- One Year license for
  - *Encrypted Netlist only*
- Unlimited Designs license for
  - *HDL Source*
  - *Netlist*
- Upgrade from
  - *HDL Source to Netlist*
  - *Single Design to Unlimited Designs*

SYMBOL



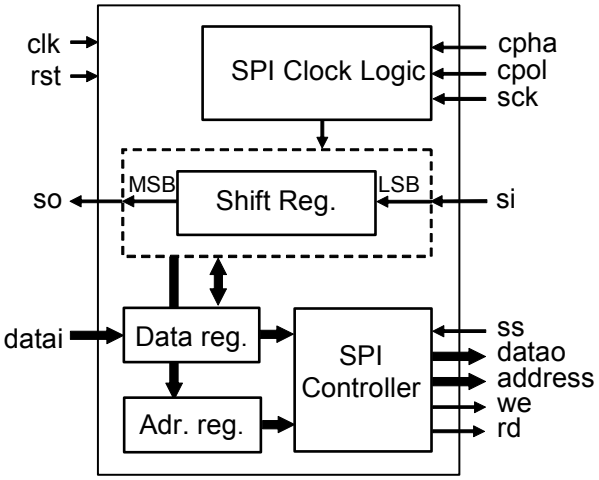
PINS DESCRIPTION

PIN	TYPE	DESCRIPTION
clk	input	Global clock
rst	input	Global reset
datai(D:0)	input	Data bus input
cpha	input	SCK clock phase
cpol	input	SCK clock polarity
sck	input	SPI serial clock
si	input	SPI serial data input
ss	input	Slave select
datao(D:0)	output	Data bus output
addres(A:0)	output	Address bus output
rd	output	Read output
we	output	Write enable
so	output	Slave serial data output

BLOCK DIAGRAM

SPI Clock logic controls phase and polarity of the SCK clock line, and detects correct sample and shift edge for the Shift register. SPI clock Logic allow user to select any of four combinations of serial clock (SCK) phase and polarity using two pins CPHA and CPOL. The clock polarity is specified by the CPOL, which selects an active high or active low clock and has no significant effect on the transfer format. The clock phase CPHA selects one of two fundamentally different transfer formats. The clock phase and polarity should be identical for the master SPI device and the communicating slave device. In some cases, the phase and polarity are changed between transfers to allow a master device to communicate with peripheral slaves having different requirements. The flexibility of the SPI system on the DSPIS allows direct interface to almost any existing synchronous serial peripheral.

Shift register– is a central element in the SPI system. When an SPI transfer occurs, an 8-bit character is shifted out on data pin while a different 8-bit character is simultaneously shifted in a second data pin. Another way to view this transfer is that an 8-bit shift register in the master and another 8-bit shift register in the slave are connected as a circular 16-bit shift register. When a transfer occurs, this distributed shift register is shifted eight bit positions; thus, the characters in the master and slave are effectively exchanged.



Data Register holds data read from passive device and to be sent serially to the SPI Master.

Address Register holds address presented on Address bus. it's contents is incremented every single data portion sent/received serially through the SPI bus.

SPI Controller - detects begin and end of SPI transfer. Manages data exchange between DSPIS and passive device controlled by DSPIS, and increment Address Register (SPAD) after any successful transfer.

PERFORMANCE

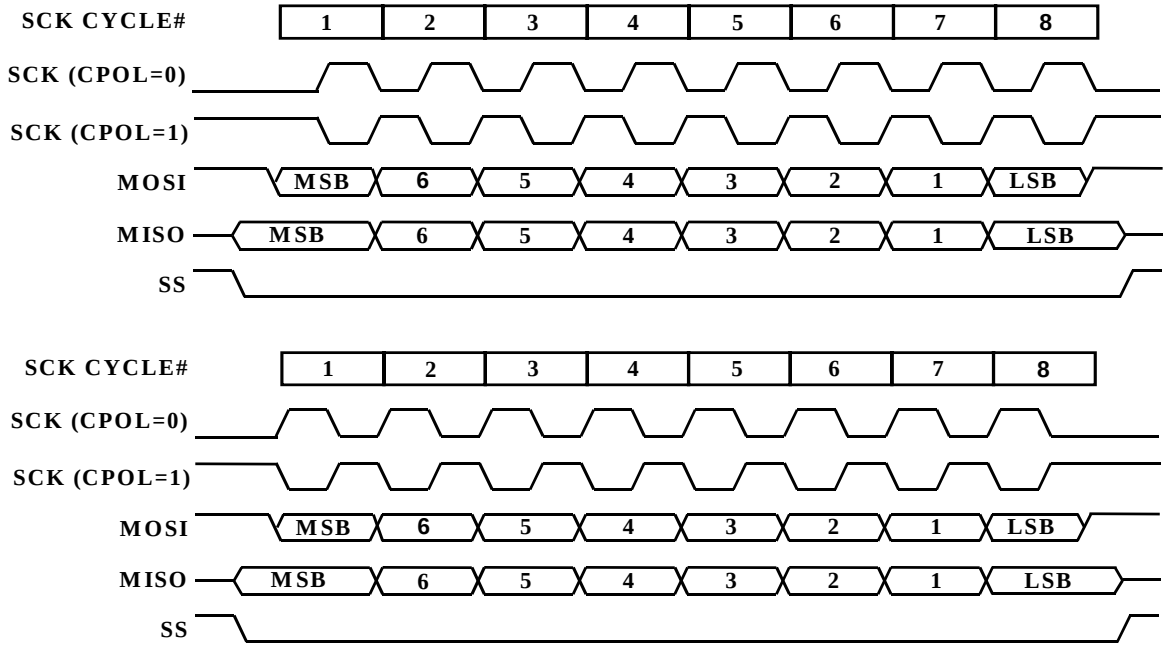
The following table gives a survey about the Core area and performance in the LATTICE® devices after Place & Route (all key features have been included):

Device	Speed grade	LUTs/PFUs	F_{max}
XP	-5	94 / 55	219 MHz
ECP	-5	94 / 55	226 MHz
EC	-5	94 / 55	222 MHz
XP2	-7	69 / 49	306 MHz
ECP2	-7	90 / 55	324 MHz
ECP2M	-7	69 / 49	345 MHz
SC	-7	84 / 55	489 MHz

Core performance in LATTICE® devices

Transfer Formats

Software can select any of four combinations of serial clock (SCK) phase and polarity using two bits in the SPI control register (SPCR). The clock polarity is specified by the CPOL control bit, which selects an active high or active low clock and has no significant effect on the transfer format. The clock phase (CPHA) control bit selects one of two fundamentally different transfer formats. The clock phase and polarity should be identical for the master SPI device and the communicating slave device. In some cases, the phase and polarity are changed between transfers to allow a master device to communicate with peripheral slaves having different requirements. The flexibility of the SPI system on the DSPI allows direct interface to almost any existing synchronous serial peripheral.



CONTACTS

For any modification or special request please contact to Digital Core Design or local distributors.

Headquarters:

Wroclawska 94

41-902 Bytom, POLAND

e-mail: info@dcd.pl

tel. : +48 32 282 82 66

fax : +48 32 282 74 37

Distributors:

Please check http://www.dcd.pl/apartn.php