FPGA EPIC Device Editor Tutorial

Introduction

EPIC (Editor for Programmable Integrated Circuits) is a graphical application for viewing and configuring FPGAs. It contains many advanced features that enable you to quickly and efficiently make design changes. It is especially useful when implementing incremental ECO (engineering change order) changes late in the design cycle. EPIC supports all Lattice Semiconductor FPGAs. It can be used for, but not limited to, the following tasks:

- Visually inspect and modify design connections, PFU logic, I/O types, EBR (embedded block RAM) contents or PLL (phase-locked loops) parameters.
- Document the changes that have been made and play back those steps to reproduce the changes to the design.
- Manually place and route critical components before or after running automatic place-and-route tools on an entire design.
- Read, write, and undo certain preferences in the preference (.prf) file.
- Run TRACE for timing analysis and DRC (design rule check) on your design.

This tutorial familiarizes you with the interface and provides specific examples showing you how to perform some of the tasks just given.

Learning Objectives

When you have completed this tutorial, you should be able to:

- Open a placed and routed physical design in EPIC.
- Zoom and pan in the Editing area to inspect design elements.
- Find and select specific design elements.

- Run a delay report on a selected net.
- Manage engineering change order (ECO) tasks:
  - Change PFU logic.
  - Modify PIO attributes.
  - Edit sysClock PLL configurations.

Time to Complete This Tutorial

The time to complete this tutorial is about 30 minutes.

System Requirements

One of the following software configurations is required to complete the tutorial:

- ispLEVER
- ispLEVER Starter

Accessing Online Help

You can find online help information on EPIC at any time by pressing the F1 key.

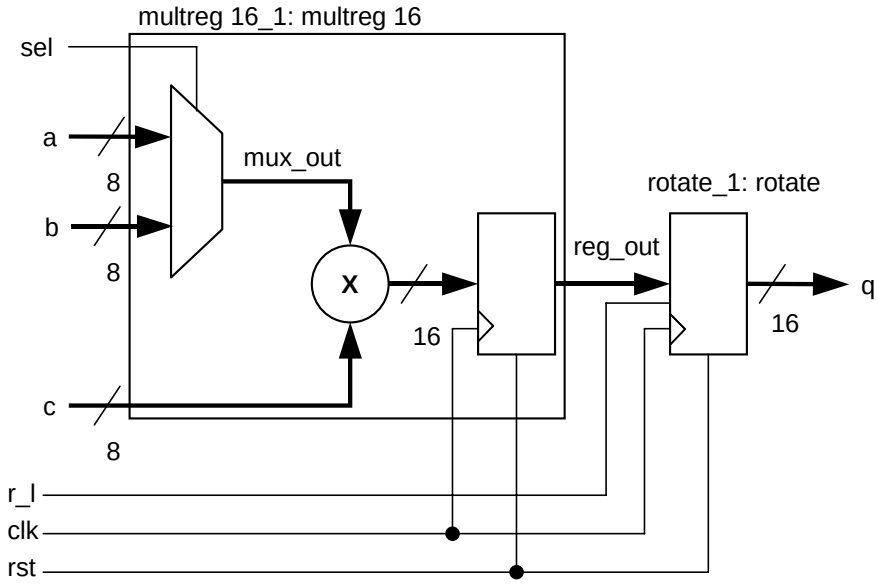
About the Tutorial Design

The tutorial design is a small LatticeEC design featuring a multiplexer (multreg16) - and a multiply, with a registered output followed by another register stage named (rotate) that provides an optional rotate function. You can find the three design files at:

- <*install_dir*>\examples\tutorial\epic_tutor**veriloghsdn.ncd**
- <*install_dir*>\examples\tutorial\epic_tutor**veriloghsdn.prf**
- <*install_dir*>\examples\tutorial\epic_tutor**veriloghsdn_map.ncd**

Please observe the instructions in “Prerequisites” on page 3 on how to use these files. Figure 1 shows a high-level block diagram of the tutorial design.

Figure 1: Block Diagram of the Tutorial Design



Prerequisites

The ispLEVER software provides the post-par .ncd files for this tutorial. Before beginning, you must get the tutorial design files to be used with this tutorial. EPIC needs a physical design (.ncd) file and optionally a physical preference (.prf) file as input. This tutorial uses two .ncd files: one is just mapped and the other both mapped and placed-and-routed.

To perform this tutorial, go to the <*install_dir*>\examples\tutorial\epic_tutor directory and copy all of the three design files to your working directory (for example, C:\myworkbench\ispLEVER\epic_tutor).

Copying the files into you own directory ensures that the original tutorial design files are not altered, so other users can use them later.

Task 1: Start EPIC

To run EPIC:

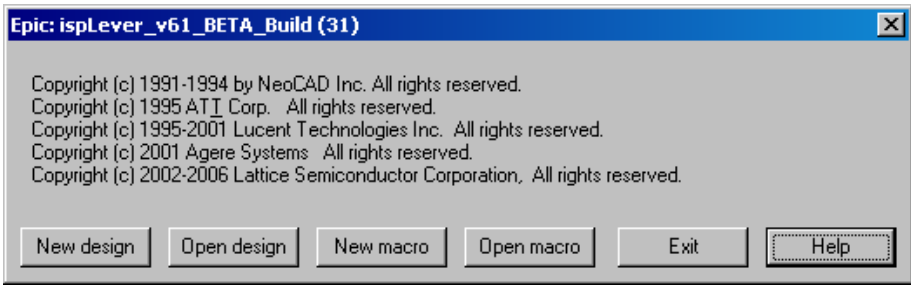
1. In the Start Menu, go to **Programs > Lattice Semiconductor > Accessories** and click the **Epic** menu item.

   Note

   You can run EPIC as a process of your current design implementation in the Project Navigator or independently from a project. Press F1 to see online Help for details.

   The EPIC Start dialog box appear, as shown in Figure 2.

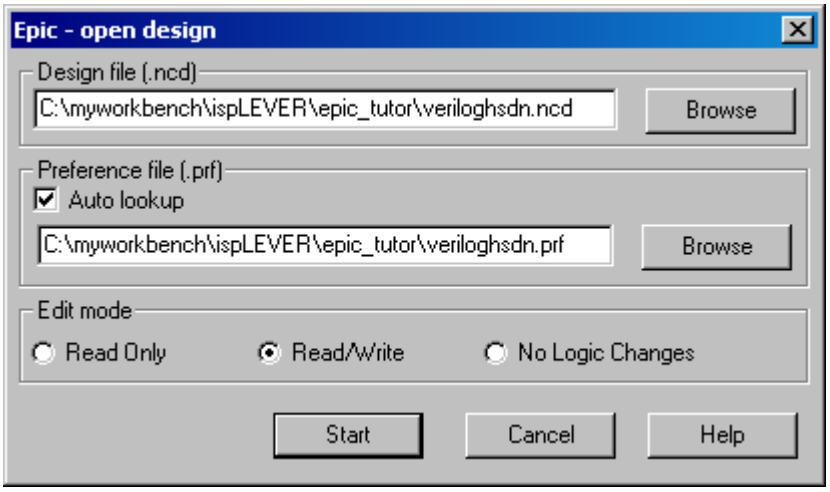
Figure 2: EPIC Start Dialog Box



2. In the EPIC Start dialog box, click **Open design** and navigate to the tutorial **veriloghsdn.ncd** file.
3. Click **Open**.

   The Open design dialog box appears, as shown in Figure 3.

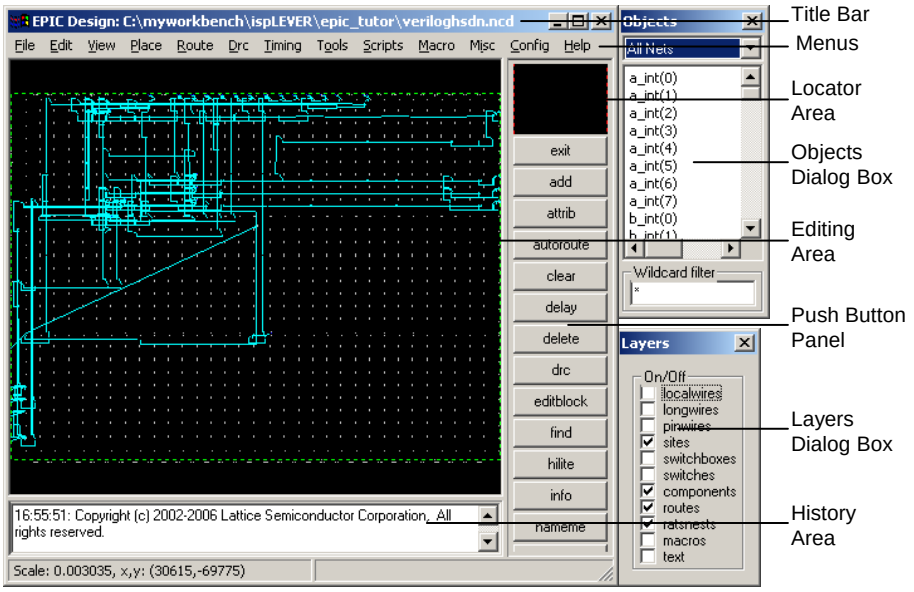
Figure 3: Open Design Dialog Box



4. In the Open design dialog box, make sure that the **Read/Write** Edit mode is selected and that paths to your .ncd file and the accompanying .prf file are correct. The Read/Write Edit mode setting allows changes to be made in the physical design and physical preference files.
5. Click **Start**.

   An Initializing EPIC dialog box appears, giving you status on opening your design. The EPIC main window appears, as shown in Figure 4.

Figure 4: EPIC Main Window



Note

The .prf file may generate some parsing errors. You can ignore these errors since they do not affect this tutorial.

6. Take a quick tour of the EPIC graphical interface.

Observe that the Objects and Layers dialog boxes automatically open to the right of the EPIC main window. These dialog boxes allow you to view certain design elements and control how EPIC displays your design in the Editing area. The Editing area is where your circuit is graphically displayed. You can view, highlight, and edit objects in this area. Objects include components, nets, wires, pins, switch boxes, and a number of other design elements. See “Glossary” on page 21 for definitions of those design elements. The History area displays the succession of command lines that were executed in the open EPIC session. You can choose commands from menus at the top of the main window or from the Push Button panel to the right of the Editing area.

Task 2: View Objects

Now you should begin getting familiar with how to view objects in the EPIC Editing area. You can use several EPIC features to do this, including zooming, panning, and turning on and off different visible layers. You can find more detailed information on these general operations in the EPIC online Help by pressing F1.

Note

You must first activate the EPIC Editing area before you can begin issuing commands. To do so, click anywhere in the Editing area.

Zooming in the Editing Area

To zoom in and out on design elements in the Editing area:

1. In the Editing area, right-click on an object or area of interest.
2. Continue zooming in by right-clicking until the object is properly displayed.

   You can also click the **zoom in** button 

on the Push Button panel.
3. Click the middle mouse button on the object to zoom out one magnification level.
4. Click the **zoom all** button 

on the Push Button panel to zoom all the way out, displaying the entire device.
5. Click and drag your cursor downward in a diagonal direction from left to right.

   Now you should still be at a zoomed-in magnification level.

Panning in the Editing Area

To pan in the EPIC Editing area:

1. Zoom in at least one magnification level in the Editing area.
2. With right button pressed, move your mouse in a circular motion.

   EPIC allows you to pan in any direction to find an object using this panning technique. If you move your right-clicked cursor to the left, right, up or down position, you pan in that direction.

   Note

   You can also use the Home/End/Page Up/Page Down, arrow keys to pan across the Editing area to view and find objects. See the EPIC online Help for more information.

3. Now zoom all the way out in the Editing area by clicking the **zoom all** button.

Toggle Visible Layers

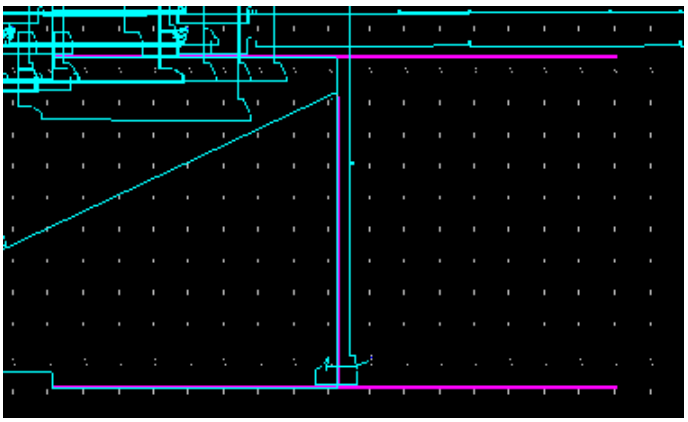
Next you will examine layers in EPIC. Layers refer to an object type that is displayed across the array in the Editing area. By default, EPIC displays layers of sites, components, routes, ratsnests, and macros. The Layers dialog box to the right of the main window shows all of the viewable default layers in EPIC. See “Glossary” on page 21 for definitions of design elements in the Editing area.

To turn on layers using the Layers dialog box:

1. Click the Layers dialog box to activate it.
2. Select **longwires**.

   Longwires appear in the Editing area in magenta, as shown in Figure 5.

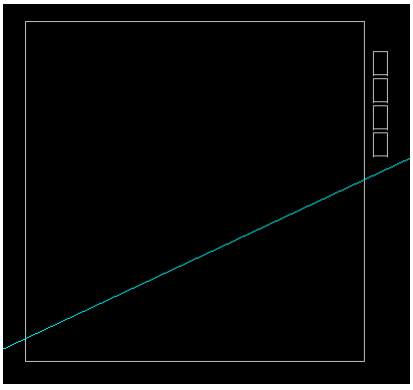
Figure 5: Longwires Layer in the Editing Area



3. Clear the **longwires** option.

   The longwires disappear.
4. Now perform the same operation with the **switchboxes** layer.
5. Zoom in on one of the switchboxes using the mouse drag from left to right over a switchbox, as shown in Figure 6.

Figure 6: Zoom in on One of the Switchboxes



Observe in Figure 5 that there is one large square object that represents the switch box and four smaller rectangular boxes to the square's upper right corner. These smaller rectangular boxes are slices. There is a ratsnest line representing a logical connection running through the switch box.

6. Now zoom all the way out in the Editing area by clicking the **zoom all** button.

Task 3: Select Objects

Now you will use the Objects dialog box and zooming and panning to select objects in the Editing Area. You will also select multiple nets and create a path definition. See the EPIC online Help for information on how to select an object with the Find dialog box.

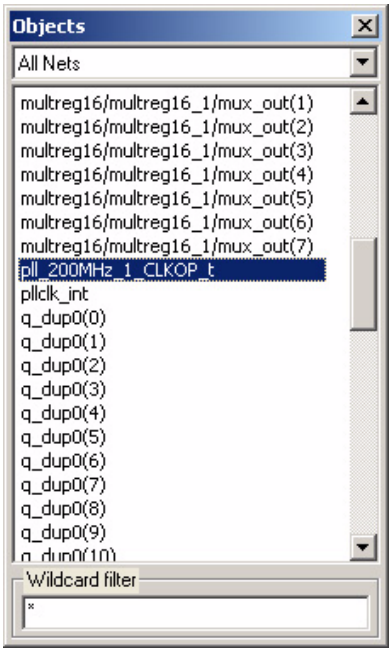
When you select objects in EPIC, you can perform editing functions that affect the .ncd file. For example you can add or delete elements, swap them, change their programming, or highlight them for reference purposes.

Select One Object

To select an object in the Objects dialog box:

1. In the Objects dialog box, select **All Nets** in the object type drop-down list.
2. Click on the **pll_200MHz_1_CLKOP_t** net in the list, as shown in Figure 7.

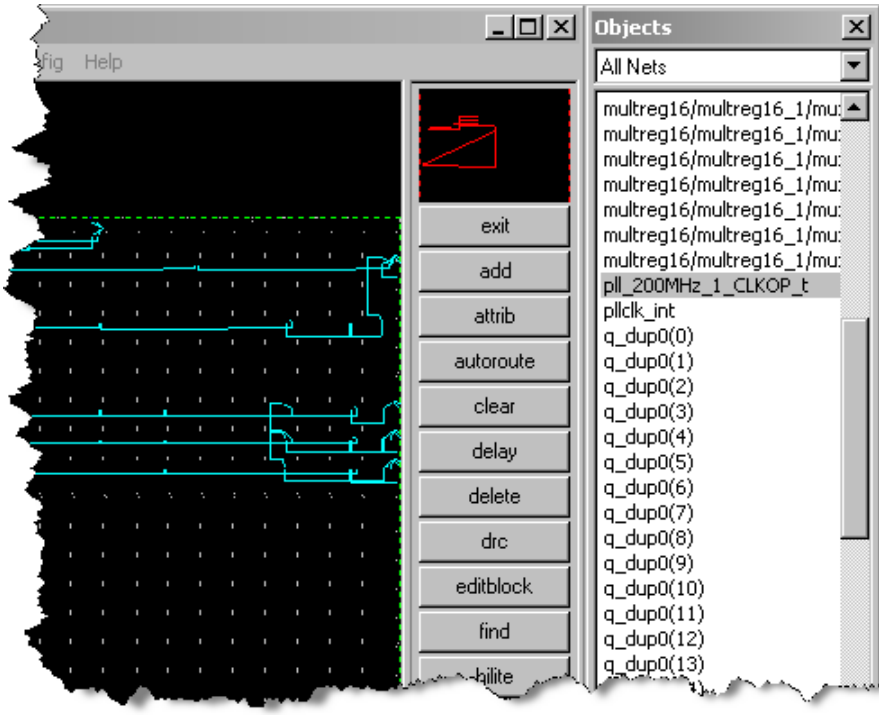
Figure 7: Select a Net in the Objects Dialog Box



3. Look at the Locator area above the Push Button panel.

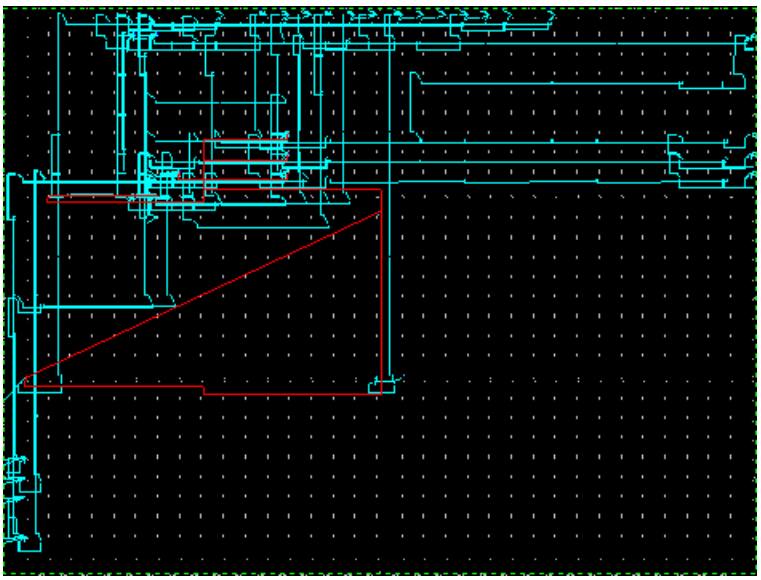
   The minimized panoramic view of the highlighted net displays in the Locator area, as shown in Figure 8.

Figure 8: A Net in the Locator Area



This net is now selected. The red object color indicates that it is selected so you can perform operations on it, as shown in Figure 9.

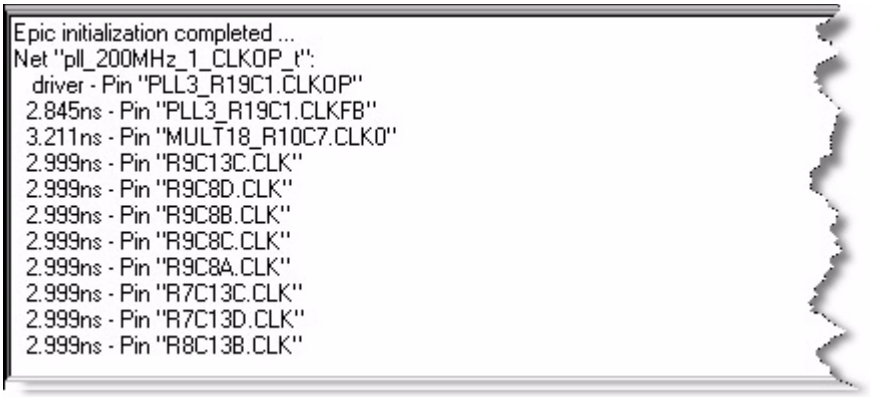
Figure 9: A Highlighted Net in the Editing Area



4. Choose **Timing > Delay**, or click **delay** 

in the Push Button panel to see a quick report in the History area on the pin delays in this net, as shown in Figure 10.

Figure 10: Delay Report on a Net



5. Click the **clear** button 

to deselect all objects in the Editing Area.
6. In the Objects dialog box, click on the **pllclk_int** net.

   The net is barely visible in the Locator area because it is a small net.
7. Click the **zoom to** button 

to zoom in on that net.
8. Click the **clear** button again to ensure that nothing else is selected.
9. Select the **pllclk_int** net again.
10. Choose **View > Highlight** or the **hilite** button 

.

    The net are highlighted in yellow and stay that color for later reference.
11. Select the **pllclk_int** net again, if it is not selected.
12. Choose **View > Unhighlight**.

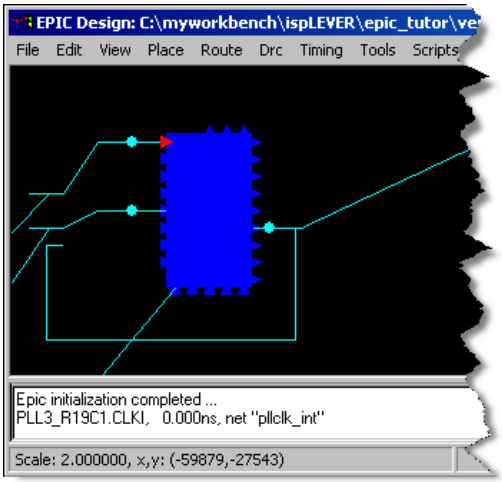
    The net returns to its original color.

    Note

    See the EPIC online Help for how to customize the highlight colors.
13. Use the zoom and pan function to move the viewable area to the upper right end of the net, and click on the pin that appears as a triangle connected to the component.
14. Click it to highlight it in red.

The name of the pin **PLL3_R19C1.CLKI** appears in the History area, as shown in Figure 11.

Figure 11: Pin PLL3_R19C1.CLK



15. Now deselect the pin by clicking it once again.
16. Zoom all the way out in the Editing area by clicking the **zoom all** button.

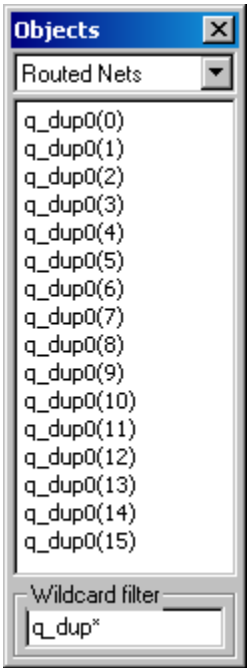
Select Multiple Objects

To select multiple objects using the Objects dialog box and create a path definition:

1. In the Objects dialog box, select the **Routed Nets** object type from the drop-down menu.
2. Enter **q_dup*** in the Wildcard filter text box at the bottom and press **Enter**.

All nets that begin with that name appear in the Objects dialog box, as shown in Figure 12.

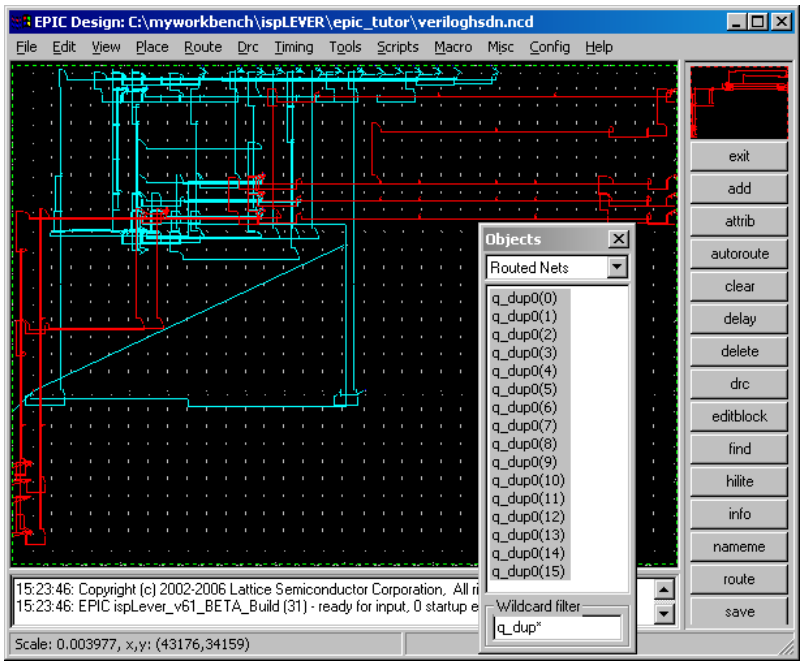
Figure 12: Wildcard Filter in Objects Dialog Box



3. Drag the cursor up over all of the **q_dup*** entries to select all of them.

   They all appear selected in the Editing area, as shown in Figure 13.

Figure 13: Select Multiple Nets with Wildcard Filter

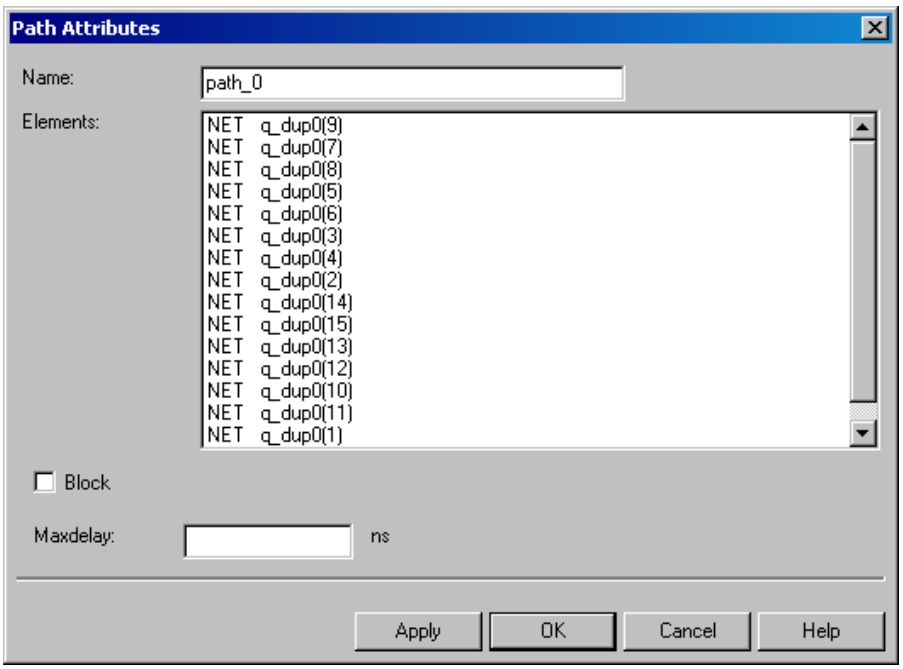


Besides using wildcards, you can also use Ctrl-click to select multiple objects in this dialog box or use the **Shift** key to select multiple contiguous objects in the list.

4. Choose **Edit > Add Path**.

   All of the selected nets are displayed in the Path Attributes dialog box that appears, as shown in Figure 14.

Figure 14: Path Attributes Dialog Box



5. In the Path Attributes dialog box:
   a. Select the **Block** option.
   b. Enter "**10**" in the Maxdelay text box.
   c. Click **Apply** and **OK** to save the changes and close the dialog box.
6. Click **File > Save**.

   A path named **path_0** has been saved in the design.

7. Now go back to the Objects dialog box, and select **Paths** from the drop-down menu, as shown in Figure 15.

Figure 15: Select Path from Objects Dialog Box

8. Select **path_0** and your path is remembered.

   You can analyze it or ascribe preferences to it as required.

9. Click the **clear** button to clear all selection.
10. Click the **zoom all** button to zoom all the way out in the Editing area.

Task 4: Engineering Change Management

It is a common user scenario to make minor changes to the .ncd file and produce a new bitstream late in the design cycle. Last-minute design changes like those are commonly referred to as engineering change orders (ECOs). These changes are usually made when synthesis and placement and routing are completed, that is, on the netlist level. Compared to HDL-level (design entry) changes, netlist-level changes result in greatly reduced compilation time.

Incremental design changes are changes that affect only a few logic groups in a design. While modular FPGA design methods are widely adopted today, a significant amount of time has been invested in modular integration, performance maximization, and design verification, as a project nears completion. It is vital that your ECO changes affect specific parts of your design and have minimal impact on unrelated parts of your design. After each design change, you should verify the impact of the change on your design. You can perform timing analysis and a DRC check to verify your design. For more information on modular-based incremental design methods, refer to the documents listed in “Recommended Reference Materials” on page 22.

While there are many different types of changes that can be made to an FPGA design with EPIC, this task only addresses three of them: editing PFU logic, modify PIO attributes, and change PLL configuration. While it is possible to change routing information, this is not recommended due to the possibility of internal contention during reconfiguration.

Edit PFU Logic

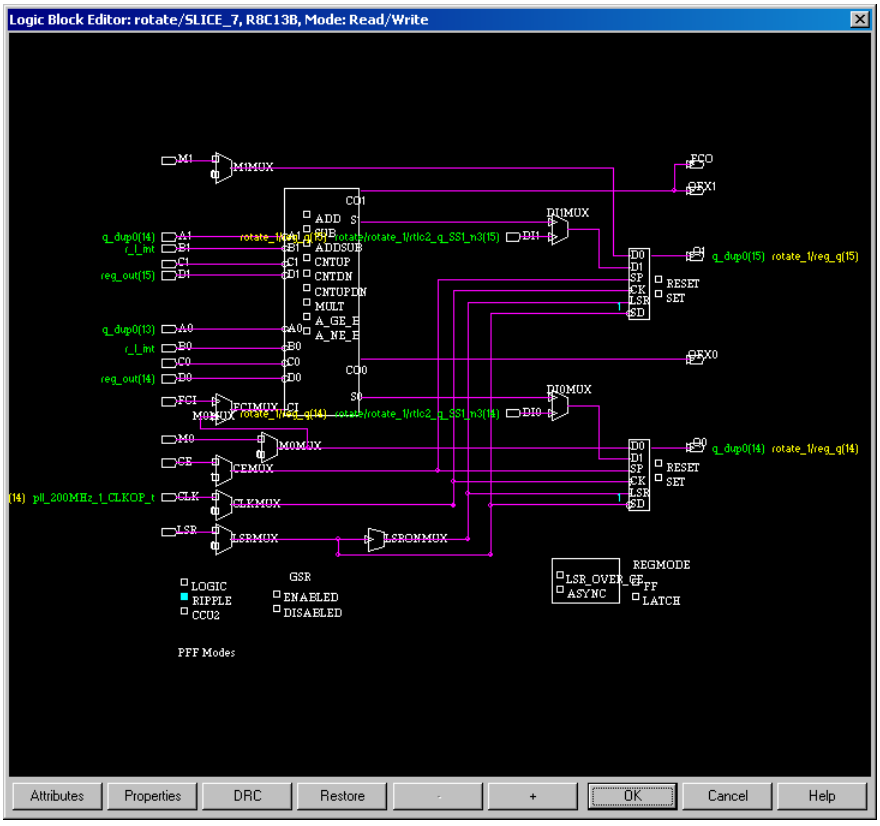
To edit a PFU component's logic in the Editing area:

1. In the Objects dialog box, choose **Placed Comps** in the drop-down list.
2. Select the **rotate/SLICE_7** slice component.

   This slice is used as a multiplier in the design.
3. Click the **zoom to** button.
4. Click the **editblock** button in the Push Button panel to edit this component.

   The Logic Block Editor window appears, as shown in Figure 16.

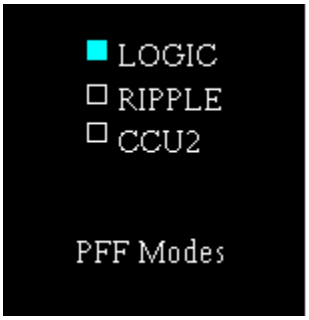
Figure 16: Edit PFU Logic in the Logic Block Editor



5. Find the **PFF Mode Options** in the lower-left corner of the window.

6. Select the **LOGIC** option, as shown in Figure 17.

Figure 17: PFF Mode Options



The entire logical functions of the component are re-programmed to perform in logic mode as opposed to ripple mode.

7. Click **OK** to close the Logic Block Editor.

   The DRC check results appear in the History Area. EPIC automatically runs DRC- once you make changes and click **OK** in the Logic Block Editor.

8. Choose **File > Save** to re-program this slice to this logic function.

   Messages in the History area indicates that the changes have been recorded to the .ncd file.

9. Now zoom all the way out in the Editing area by clicking the **zoom all** button.

Modify PIO Attributes

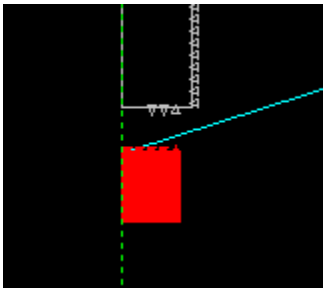
For LatticeECP/EC devices, each PIO cell includes a sysIO buffer and I/O logic (IOLOGIC), and supports the LVTTL, LVCMOS 1.2, 1.5, 1.8, 2.5, 3.3V, SSTL ,and HSTL standards. Differential standards supported include LVDS, RSDS, BLVDS, LVPECL, differential SSTL, and differential HSTL. All LVCMOS buffers have programmable pull, programmable drive and programmable slew configurations that can be set in EPIC.

To modify PIO attributes in the Editing area:

1. In the Objects dialog box, select **Placed Comps** from the drop-down list.
2. Choose the **q(8)** component, a PIO component programmed as a data multiplexer.

3. Click the **zoom to** button to view the PIO component, as shown in Figure 18.

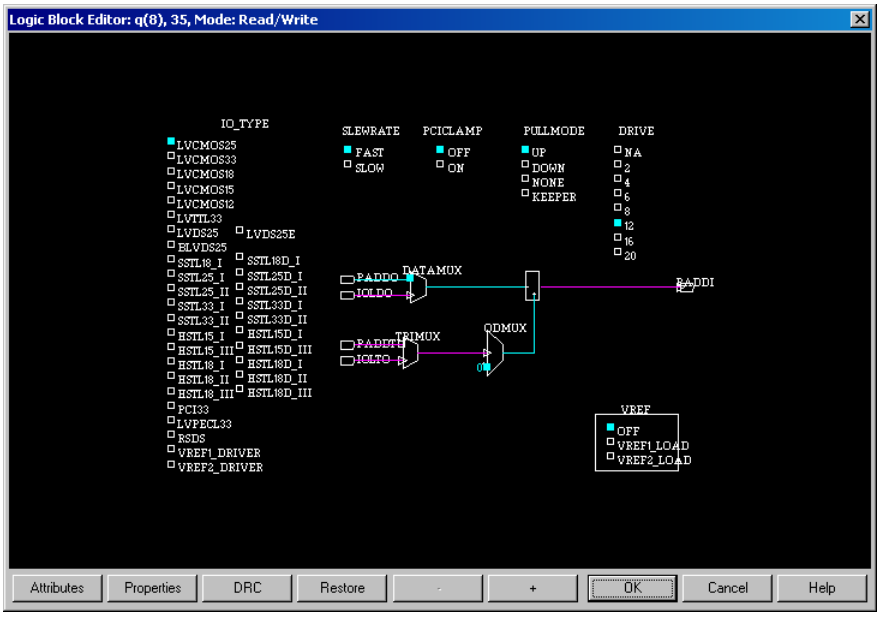
Figure 18: PIO Component q(8)



4. Click the **editblock** button.

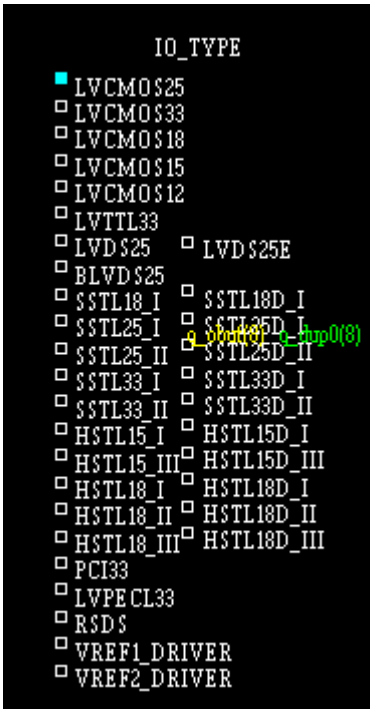
   The Logic Block Editor window appears, as shown in Figure 19.

Figure 19: Modify PIO Attributes in the Logic Block Editor



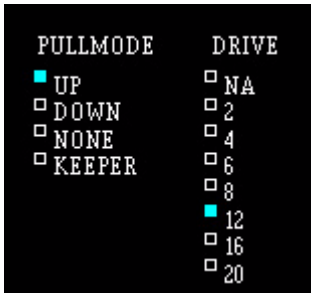
5. Locate the **IO_TYPES** option at the left of the window, as shown in Figure 20.

Figure 20: IO_TYPE Options



6. Locate the **PULLMODE** options and the **DRIVE** options at the right of the window, as shown in Figure 21.

Figure 21: PULLMODE and DRIVE Options



7. Change the IO standard by selecting the **LVCMOS33** option under the **IO_TYPE** label**.**
8. Select **20** under the **DRIVE** label to increase the drive strength.
9. Click **OK** to close the window.

   The DRC check results appear in the History area. EPIC automatically runs DRC, once you make changes and click **OK** to close the Logic Block Editor.

10. Choose **File** > **Save** to save the changes.

    Messages in the History area indicate that the changes are recorded to the .ncd file.

11. Now zoom all the way out in the Editing area by clicking the **zoom all** button.

Change PLL Configuration

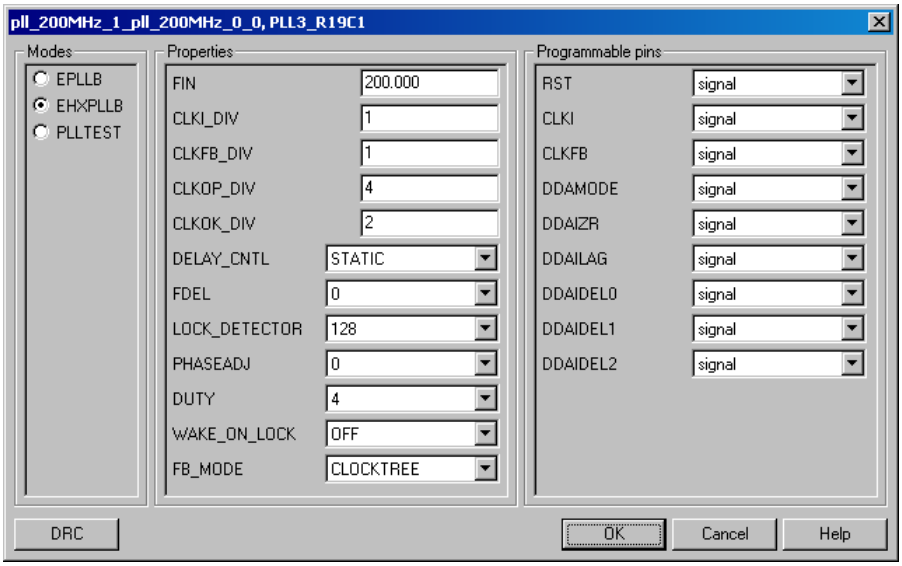
Now you will modify the delay compensation attribute (FDEL) of the sysCLOCK PLL with EPIC. It is usually performed in an attempt to improve placement and routing performance results. The FDEL (Fine Delay Adjust) attribute is used to pass the delay adjustment step associated with the output clock of the PLL. It allows you to advance or retard the output clock by the step value passed multiplied by 250 ps (nominal). The step ranges from -8 to +8, resulting in a total delay range of +/- 2 ns.

To add a delay adjustment factor to the sysCLOCK PLL:

1. Choose **Placed Comps** in the drop-down list of the Objects dialog box.
2. Select the **pll_200MHz_1_pll_200MHz_0_0** PLL component.
3. Click the **zoom to** button.
4. Click the **editblock** button.

   A PLL configuration dialog box appears, as shown in Figure 22.

Figure 22: Change PLL Configuration



5. Under Properties, set FDEL to **-5**.

6. Click DRC and observe the DRC results in the History area, as shown in Figure 23.

Figure 23: DRC Results in the History Area

7. Click **OK** to close the dialog box.

   EPIC automatically runs DRC, once you make changes and click **OK** in the PLL configuration dialog box.

8. Save the changes and close the EPIC device editor.

Apart from using EPIC, you can add a FDEL value in the following ways:

- Enter the FDEL attribute value in the HDL source code generated by IPexpress.
- Use the Pre-map Design Planner (spreadsheet view).
- Edit the preference file directly.

When ECO changes are made in EPIC after a full compilation, recompiling the entire design is not necessary. These changes are made directly to the netlist without performing a new placement and routing. With other methods, changes are made on the HDL level. Changing the FDEL value with the Design Planner is described in Task 6 and 8 of the "*LatticeEC FPGA Design with ispLEVER Tutorial.*" Compared with other methods, ECO changes made in EPIC save recompilation time.

However, EPIC changes are automatically overwritten when you recompile the design, unless they are reapplied. There are change management features such as back-annotation of ECO changes, with which you can reapply the changes on subsequent compilations.

For more information on using FDEL and other PLL attributes, refer to the documents listed in "Recommended Reference Materials" on page 22.

Summary

You have completed the "*FPGA EPIC Device Editor Tutorial.*" In this tutorial, you have learned how to do the following:

- Open a placed and routed physical design in EPIC.
- Zoom and pan in the Editing area to inspect design elements.
- Find and select specific design elements.
- Run a delay report on a selected net.
- Manage ECO changes with EPIC:

- Change PFU logic.
- Modify PIO attributes.
- Edit sysClock PLL configurations.

Glossary

Following are the terms and concepts that you should understand to use this tutorial effectively.

.ncd file. An .ncd file is a binary format FPGA post-map physical design database file generated by the Map Design process of the Project Navigator. The .ncd file includes mapped and potentially placement and route information.

.prf file. A .prf file is an ASCII text file containing preferences (placement, routing, timing constraints, or all three) specified during design entry and preferences that you added. The .prf file is an optional input to MAP, PAR, EPIC, and TRACE.

component. Components are logical configurations that will, at some point, go into a site. In EPIC, you can add components such as PFUs and PICs, tristate buffers, pull-up resistors, oscillators, or clocks. When a component is placed into a site, EPIC shows the figure as filled in.

layer. A layer refers to an object or group of objects that are viewable in the Editing area and can be turned on or off using the Layers dialog box.

net. A net (also called a signal or a signal net) is a set of component pins which are to be electrically connected in the finished design. Nets connect components to each other.

phase-locked loop (PLL). A phase-locked loop is an electronic circuit with a voltage- or current-driven oscillator that is constantly adjusted to match in phase, so it locks on the frequency of an input signal. In addition to stabilizing a particular communications channel (keeping it set to a particular frequency), a PLL can be used to generate a signal, modulate or demodulate a signal, reconstitute a signal with less noise, or multiply or divide a frequency. PLLs are more commonly used for digital data transmission but can also be designed for analog information.

programmable function unit (PFU). A programmable function unit (PFU) is a block within the LatticeECP/EC device that implements combinational logic, memory, and registers. The core of the architecture consists of PFU blocks that can be programmed to perform logic, arithmetic, distributed RAM, and distributed ROM functions.

programmable I/O cell (PIO). A programmable I/O cell (PIO) is an architectural element within an FPGA that handles actual input-output functions. It includes the I/O registers, tristate registers, and control multiplexers of a PIC. For LatticeECP/EC devices, each PIO cell includes a sysIO buffer and I/O logic (IOLOGIC).

programmable interface cell (PIC). A programmable interface cell (PIC) is a cell within a LatticeECP/EC device architecture that contains a group of two PIOs. The edges of the architecture consist of PIC blocks that contain two PIOs connected to sysIO buffers. PICs provide high-speed I/O registers and buffering to support a variety of signal interface standards.

ratsnest. When a component has been placed but has not yet been routed, the connection between that component's net pins (those pins on the net) and net pins from other components is logical, not physical. The pins are associated with each other, even though there is no electrical connection between them. In the Editing area, these logical connections making up a net show up as ratsnest lines - direct point-to-point connections between net pins.

route. Routes refer to routed nets. They are physical electrical connections that are made between the net's net pins. In the Editing area, these routed connections appear as lines following the routing resources available on the device (long lines, pinwires, switch boxes, etc.).

site. A site is a programmable logic element (used or unused) located within the device. In the EPIC Editing area sites appear as outlined figures. Typically, you refer to sites as unused or potential locations for components.

slice. A slice is an architectural element within an FPGA consisting of two LUT4 lookup tables that feed two registers (programmed to be in FF or latch mode), and some associated logic that allows the LUTs to be combined to perform functions such as LUT5, LUT6, LUT7 and LUT8. It also includes control logic to perform set/reset functions (programmable as synchronous/asynchronous), clock select, chip-select and wider RAM/ROM functions. The registers in the slice can be configured for positive or negative and edge or level clocks. There are four interconnected slices per PFU block. Each slice in a PFU is capable of four modes of operation: logic, ripple, RAM, and ROM. Each slice in the PFF is capable of all modes except RAM.

Recommended Reference Materials

- EPIC Device Editor online Help
- Incremental and Modular Design Methods, FPGA Design Guide
- LatticeECP/EC and LatticeXP sysIO Usage Guide (TN1056)
- LatticeXP2 sysIO Usage Guide (TN1136)
- MachXO sysIO Usage Guide (TN1091)
- LatticeECP/EC and LatticeXP sysCLOCK PLL Design and Usage Guide (TN1049)
- LatticeXP2 sysCLOCK PLL Design and Usage Guide (TN1126)
- MachXO sysCLOCK PLL Design and Usage Guide (TN1089)