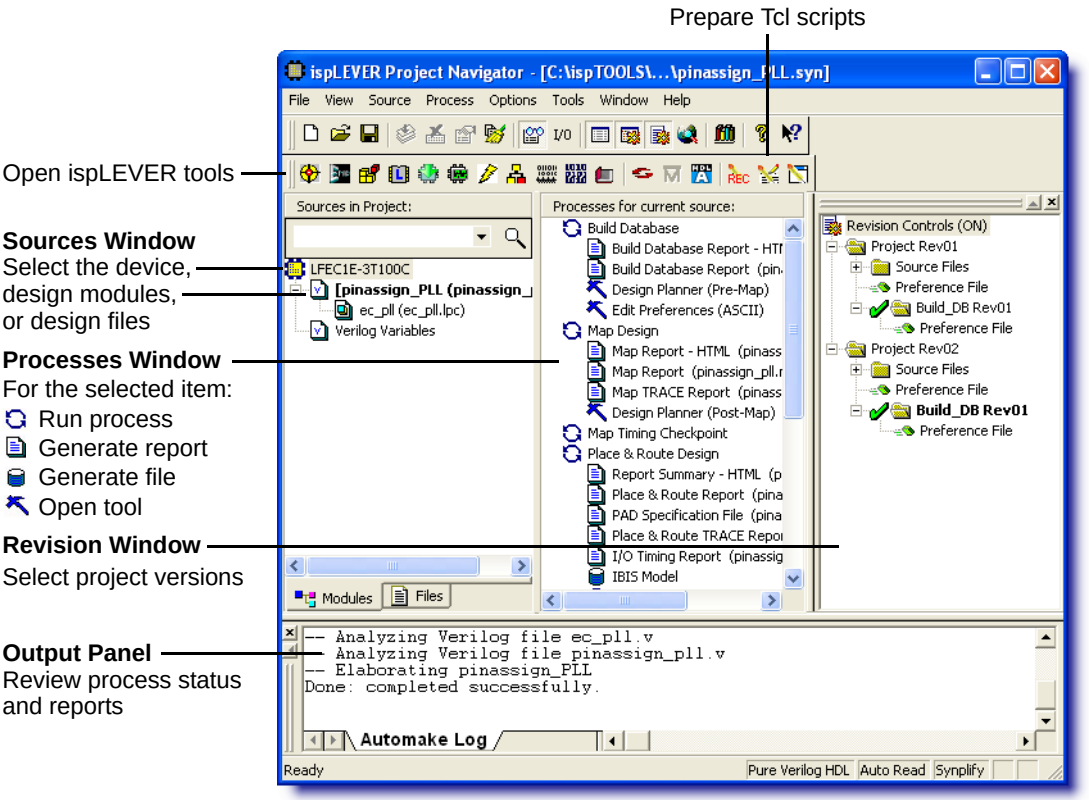
Quick Start Guide for ispLEVER Software

This guide offers a quick overview of using ispLEVER® software to implement a design in a Lattice Semiconductor device. For more information, check the ispLEVER Help in the Help menu.

ispLEVER Project Navigator

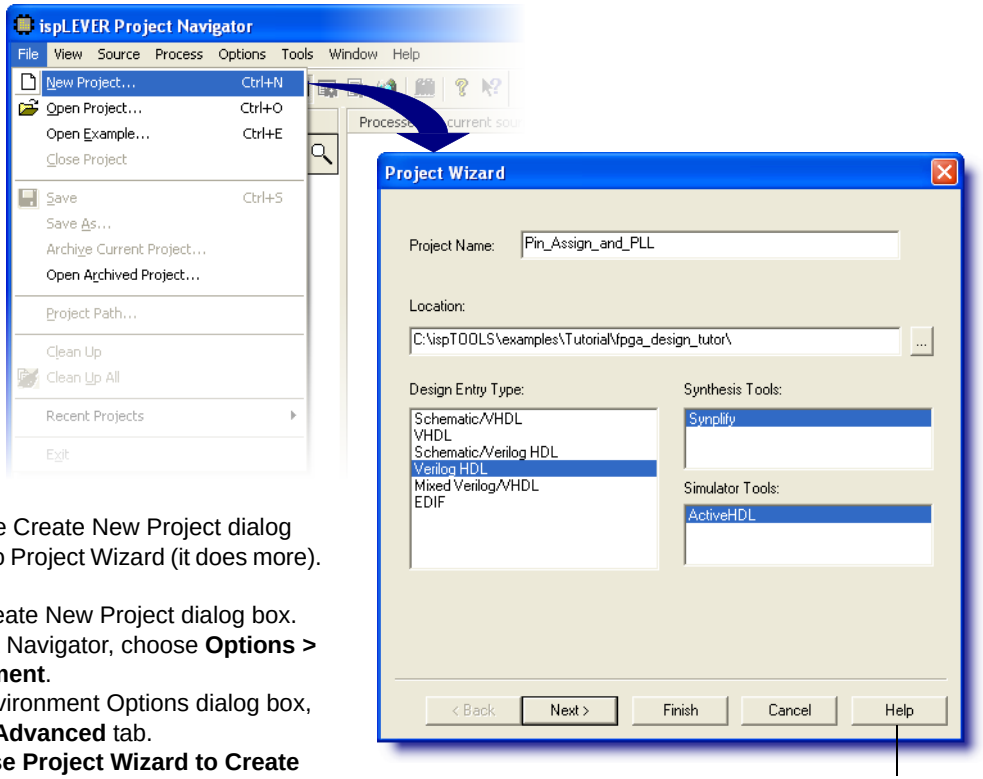
Project Navigator is the primary interface for the ispLEVER software. It organizes the files, gives access to the tools, and delivers messages. To start Project Navigator:

- Windows: choose **Start > Programs > Lattice Semiconductor > ispLEVER Project Navigator**.
- UNIX or Linux: on a command line, enter **ispgui**.



Creating a Project

Choose **File >** **New Project**.



If you see the Create New Project dialog box, switch to Project Wizard (it does more). To switch:

1. Close Create New Project dialog box.
2. In Project Navigator, choose **Options > Environment**.
3. In the Environment Options dialog box, click the **Advanced** tab.
4. Select **Use Project Wizard to Create New Design**.
5. Click **OK**.

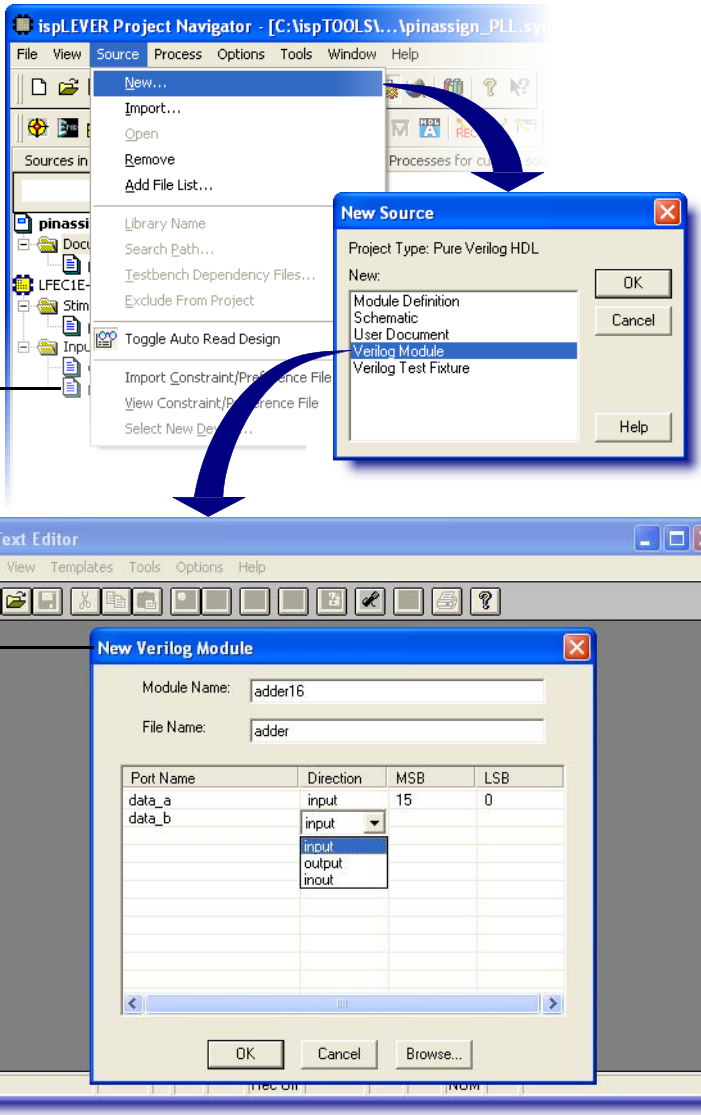
With the Project Wizard, set initial values for:

- Project name
- Location of the files
- Design language
- Synthesis tool
- Simulator tool
- Target device
- Source files

You can also select the I/O Assistant design flow option, helps you select the device pinouts early in the design process.

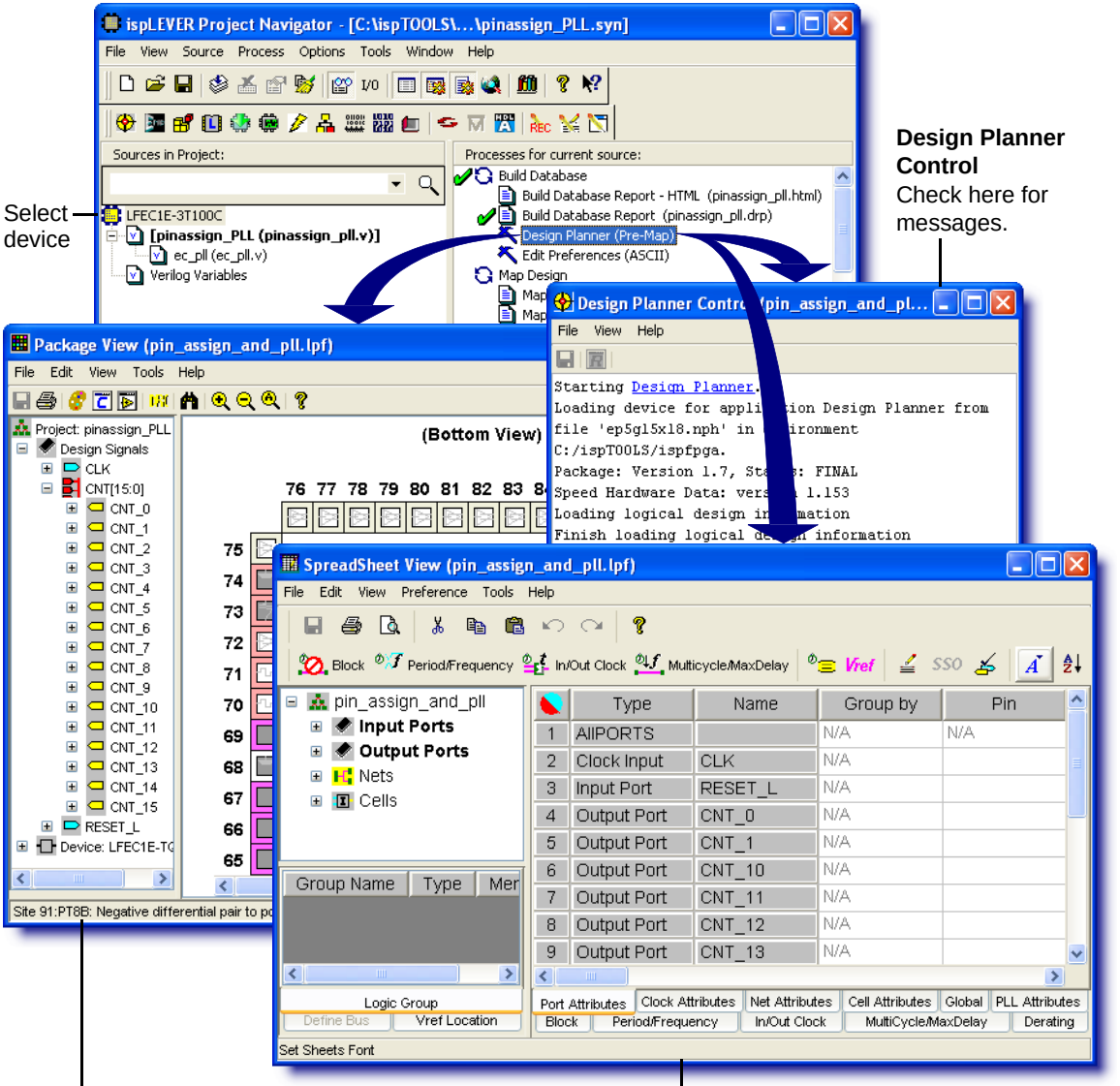
Entering the Design

- To create an HDL or schematic file, choose **Source > New**.
- To import an HDL or schematic file, choose **Source > Import**.
- To add an IP module, choose **Tools >**  **IPexpress**. After generating the IP module, import it and instantiate it in an HDL or schematic module.



Setting Timing and I/O

Select the device . Then, in the Processes Window, double-click **Design Planner**. Design Planner (Pre-Map) starts with three windows.



Package View
Assign pinouts by drag-and-drop.

Spreadsheet View
To set preferences, enter them in the sheet or through the **Preference** menu.

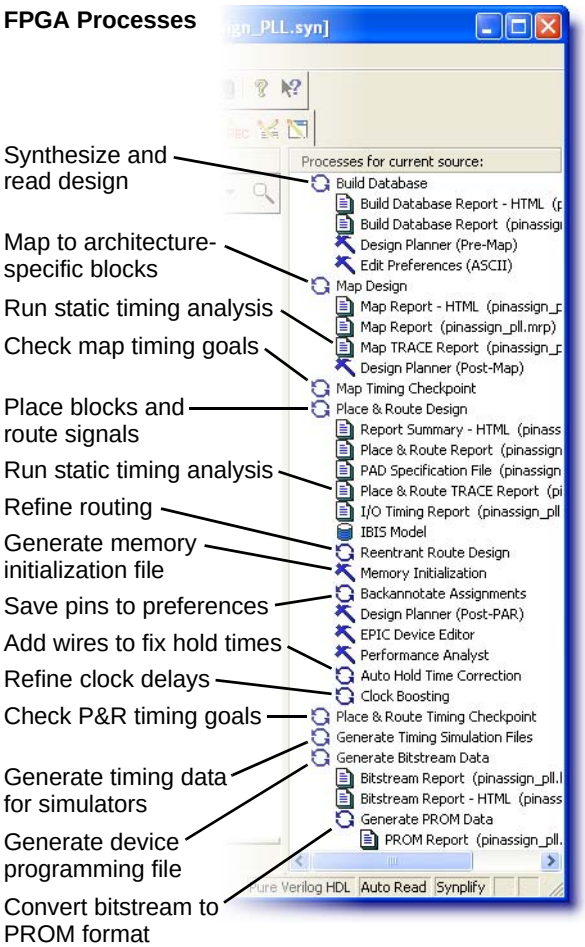
To check assignments against design rules for programmable I/Os, choose **Tools > PIOS DRC**.

Implementing the Design

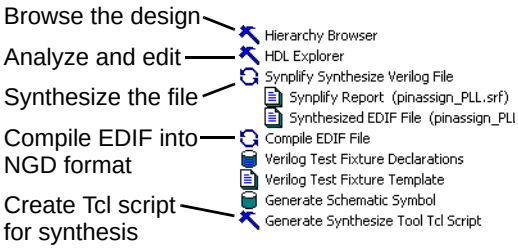
Select the device , then double-click a process . Start at the top and work down. The list of processes varies with the device and the source file selected. Following are some examples.

For more information about a process, select it and press **F1**.

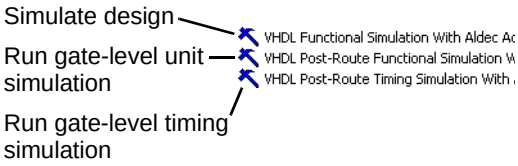
FPGA Processes



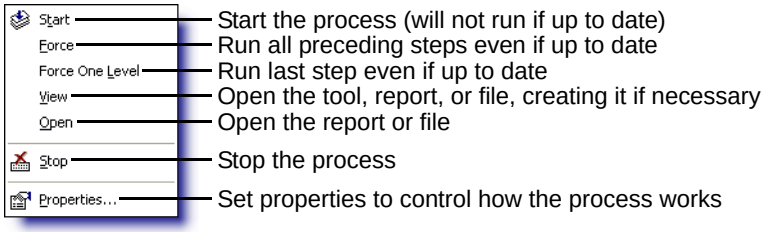
Verilog Design File Processes



VHDL Test Bench Processes



For a menu of options, right-click the process.



Getting More Information

Refer to the Online Help

- Choose **Help > ispLEVER Help**.

- Select an item in a window or dialog box and press **F1**.
- Click **Help** in a dialog box.

From the first topic in the online Help you can also:

- Take tutorials.
- Refer to design guides and reference manuals.
- Refer to synthesis and simulator tool manuals.

Refer to the Web Site

Lattice Semiconductor
www.latticesemi.com

What's New at Lattice
www.latticesemi.com/whatsnew.cfm
or click

What's New in ispLEVER
www.latticesemi.com/products/designsoftware/isplever/isplever/whatsnewinisplever.cfm

Lattice Forums
www.latticesemi.com/latticeforums

Lattice Solutions
www.latticesemi.com/solutions

Lattice Technical Literature
www.latticesemi.com/search/literature.cfm
or click

ispLeverCORE™ Modules
www.latticesemi.com/ip

Customer Support
techsupport@latticesemi.com
USA & Canada: 1-800-LATTICE (528-8423)
Other locations: +1 503 268 8001
Call from 5:30 a.m. to 6 p.m. Pacific Time.

Customer Support—Asia
techsupport-asia@latticesemi.com
Asia: +86 21 52989090
Call from 8:30 a.m. to 5:30 p.m. Beijing Time.
Chinese and English language only.