

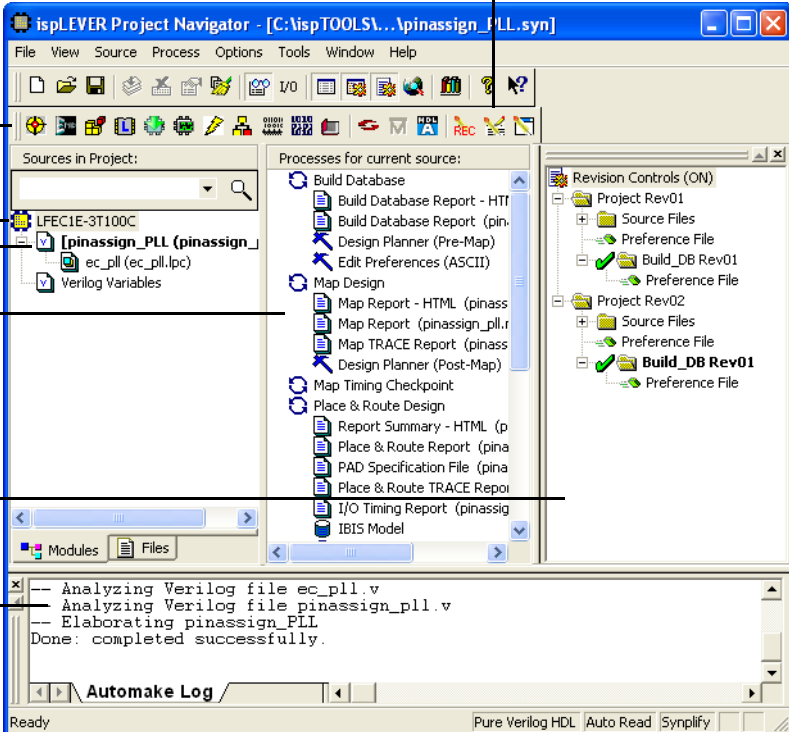
# Quick Start Guide for ispLEVER Software

This guide offers a quick overview of using ispLEVER<sup>®</sup> software to implement a design in a Lattice Semiconductor device. For more information, check the ispLEVER Help in the Help menu.

## ispLEVER Project Navigator

Project Navigator is the primary interface for the ispLEVER software. It organizes the files, gives access to the tools, and delivers messages. To start Project Navigator:

- ◆ Windows: choose **Start > Programs > Lattice Semiconductor > ispLEVER Project Navigator**.
- ◆ UNIX or Linux: on a command line, enter **ispgui**.



Prepare Tcl scripts

Open ispLEVER tools

**Sources Window**  
Select the device, design modules, or design files

**Processes Window**  
For the selected item:  
 Run process  
 Generate report  
 Generate file  
 Open tool

**Revision Window**  
Select project versions

**Output Panel**  
Review process status and reports

```

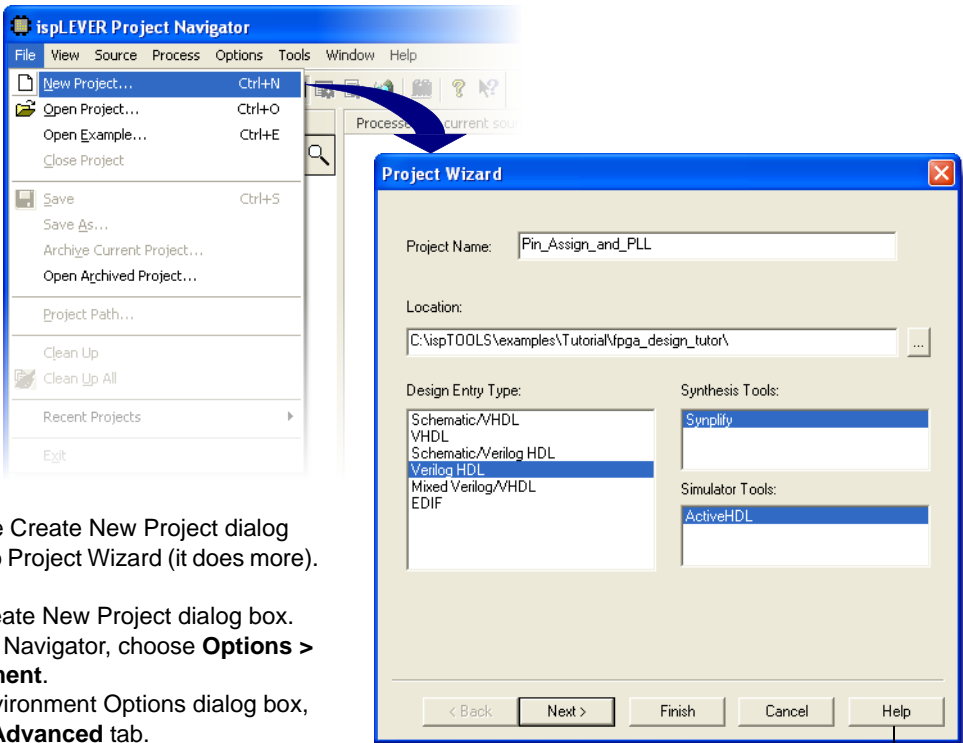
  --- Analyzing Verilog file ec_pll.v
  --- Analyzing Verilog file pinassign_pll.v
  --- Elaborating pinassign_PLL
  Done: completed successfully.
  
```

Automake Log

Ready Pure Verilog HDL Auto Read Synplify

# Creating a Project

Choose **File > New Project**.



If you see the Create New Project dialog box, switch to Project Wizard (it does more). To switch:

1. Close Create New Project dialog box.
2. In Project Navigator, choose **Options > Environment**.
3. In the Environment Options dialog box, click the **Advanced** tab.
4. Select **Use Project Wizard to Create New Design**.
5. Click **OK**.

For more information, click **Help**

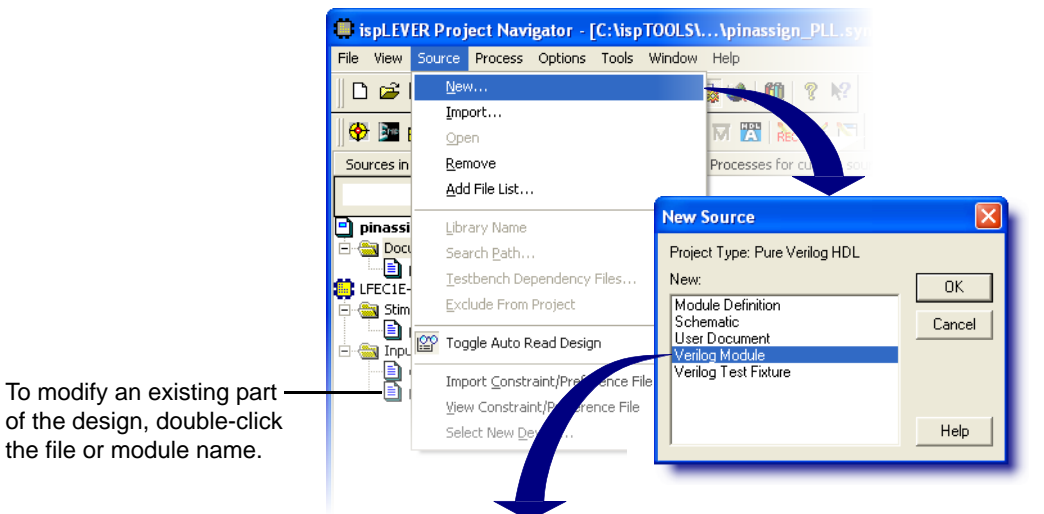
With the Project Wizard, set initial values for:

- ◆ Project name
- ◆ Location of the files
- ◆ Design language
- ◆ Synthesis tool
- ◆ Simulator tool
- ◆ Target device
- ◆ Source files

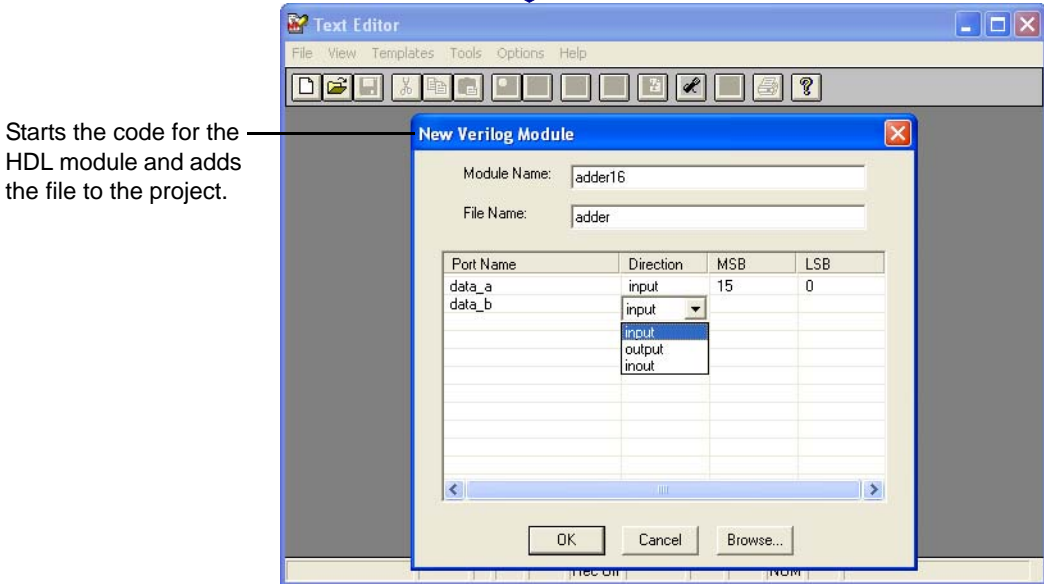
You can also select the I/O Assistant design flow option, helps you select the device pinouts early in the design process.

# Entering the Design

- ◆ To create an HDL or schematic file, choose **Source > New**.
- ◆ To import an HDL or schematic file, choose **Source > Import**.
- ◆ To add an IP module, choose **Tools > IPexpress**. After generating the IP module, import it and instantiate it in an HDL or schematic module.



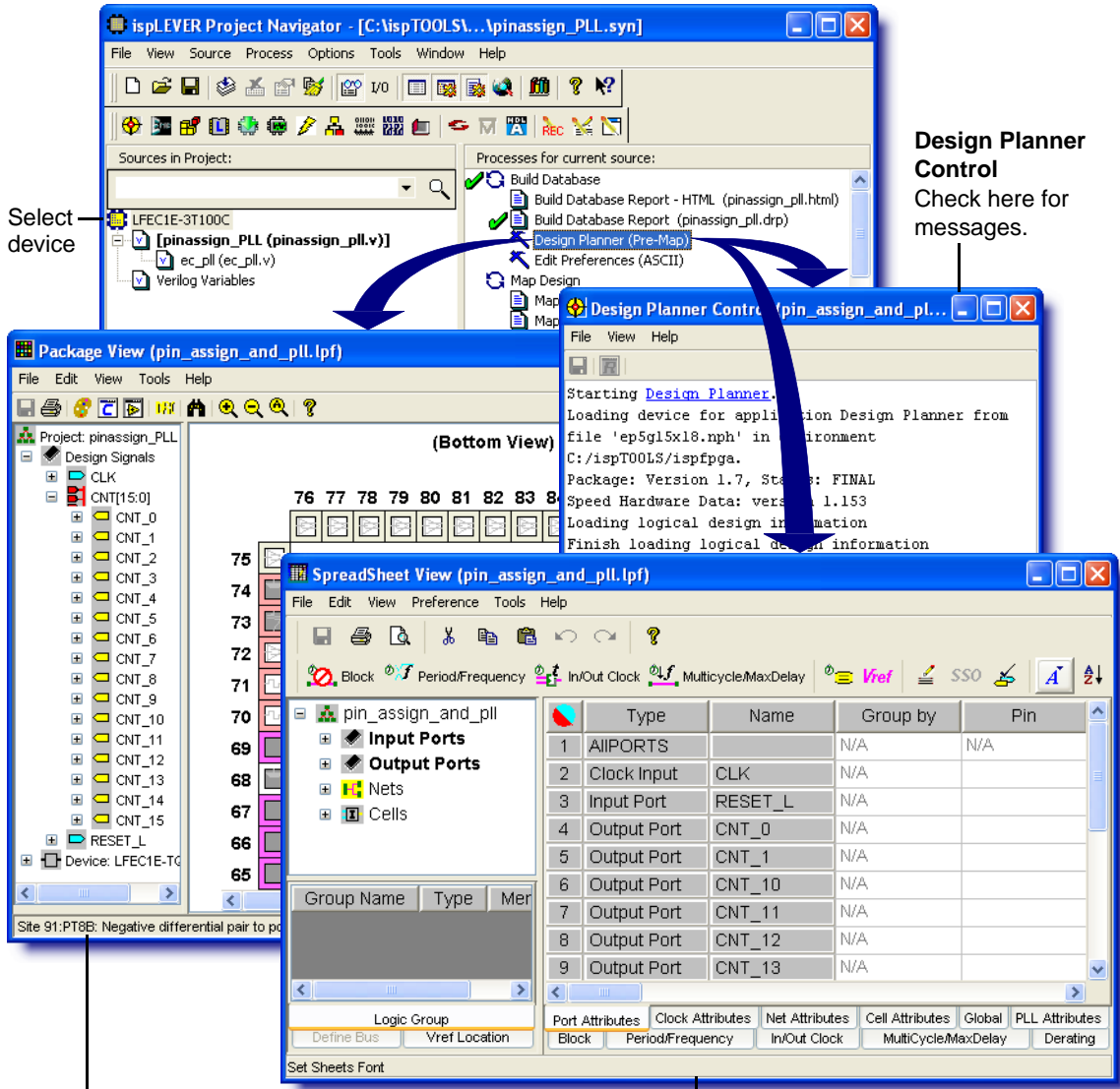
To modify an existing part of the design, double-click the file or module name.



Starts the code for the HDL module and adds the file to the project.

# Setting Timing and I/O

Select the device . Then, in the Processes Window, double-click **Design Planner**. Design Planner (Pre-Map) starts with three windows.





**Package View**  
Assign pinouts by drag-and-drop.

**Spreadsheet View**  
To set preferences, enter them in the sheet or through the **Preference** menu.

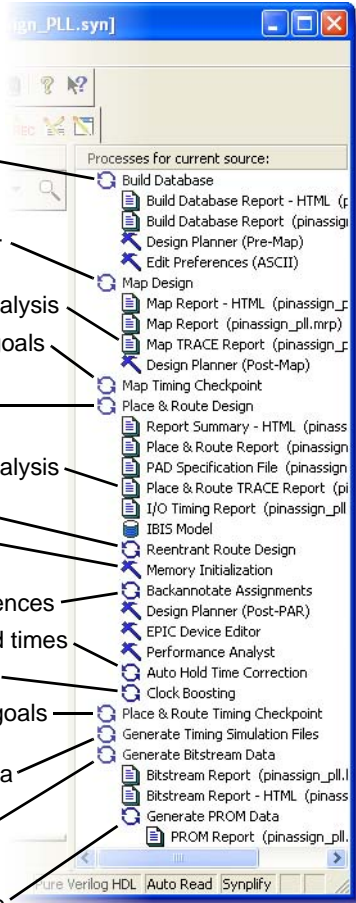
To check assignments against design rules for programmable I/Os, choose **Tools > PIOS DRC**.

# Implementing the Design

Select the device , then double-click a process . Start at the top and work down. The list of processes varies with the device and the source file selected. Following are some examples.

For more information about a process, select it and press **F1**.

## FPGA Processes



**Synthesize and read design** → Build Database

**Map to architecture-specific blocks** → Design Planner (Pre-Map)

**Run static timing analysis** → Map Timing Checkpoint

**Check map timing goals** → Map Report - HTML (pinassign\_...)

**Place blocks and route signals** → Place & Route Design

**Run static timing analysis** → Place & Route Timing Checkpoint

**Refine routing** → Reentrant Route Design

**Generate memory initialization file** → Memory Initialization

**Save pins to preferences** → Backannotate Assignments

**Add wires to fix hold times** → EPIC Device Editor

**Refine clock delays** → Clock Boosting

**Check P&R timing goals** → Place & Route Timing Checkpoint

**Generate timing data for simulators** → Generate Timing Simulation Files

**Generate device programming file** → Generate Bitstream Data

**Convert bitstream to PROM format** → Generate PROM Data

## Verilog Design File Processes

**Browse the design** → Hierarchy Browser

**Analyze and edit** → HDL Explorer

**Synthesize the file** → Synplify Synthesize Verilog File

**Compile EDIF into NGD format** → Compile EDIF File

**Create Tcl script for synthesis** → Generate Synthesize Tool Tcl Script








## VHDL Test Bench Processes

**Simulate design** → VHDL Functional Simulation With Aldec Ac

**Run gate-level unit simulation** → VHDL Post-Route Functional Simulation W

**Run gate-level timing simulation** → VHDL Post-Route Timing Simulation With

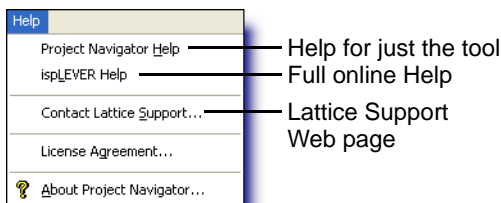
For a menu of options, right-click the process.

	Start	Start the process (will not run if up to date)
	Force	Run all preceding steps even if up to date
	Force One Level	Run last step even if up to date
	View	Open the tool, report, or file, creating it if necessary
	Open	Open the report or file
	Stop	Stop the process
	Properties...	Set properties to control how the process works

# Getting More Information

## Refer to the Online Help

- ◆ Choose **Help > ispLEVER Help**.



- ◆ Select an item in a window or dialog box and press **F1**.
- ◆ Click **Help** in a dialog box.

From the first topic in the online Help you can also:

- ◆ Take tutorials.
- ◆ Refer to design guides and reference manuals.
- ◆ Refer to synthesis and simulator tool manuals.

## Refer to the Web Site

### Lattice Semiconductor

[www.latticesemi.com](http://www.latticesemi.com)

### What's New at Lattice

[www.latticesemi.com/whatsnew.cfm](http://www.latticesemi.com/whatsnew.cfm)

or click 

### What's New in ispLEVER

[www.latticesemi.com/products/designsoftware/isplever/isplever/whatsnewinisplever.cfm](http://www.latticesemi.com/products/designsoftware/isplever/isplever/whatsnewinisplever.cfm)

### Lattice Forums

[www.latticesemi.com/latticeforums](http://www.latticesemi.com/latticeforums)

### Lattice Solutions

[www.latticesemi.com/solutions](http://www.latticesemi.com/solutions)

### Lattice Technical Literature

[www.latticesemi.com/search/literature.cfm](http://www.latticesemi.com/search/literature.cfm)

or click 

### ispLeverCORE™ Modules

[www.latticesemi.com/ip](http://www.latticesemi.com/ip)



### Customer Support

[techsupport@latticesemi.com](mailto:techsupport@latticesemi.com)  
USA & Canada: 1-800-LATTICE (528-8423)  
Other locations: +1 503 268 8001  
Call from 5:30 a.m. to 6 p.m. Pacific Time.

### Customer Support—Asia

[techsupport-asia@latticesemi.com](mailto:techsupport-asia@latticesemi.com)  
Asia: +86 21 52989090  
Call from 8:30 a.m. to 5:30 p.m. Beijing Time.  
Chinese and English language only.

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