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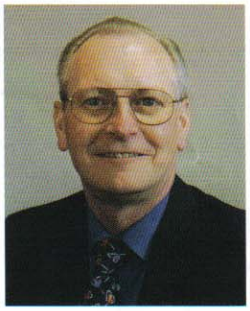


Low-cost and flexible bus interfacing for LIN and MOST

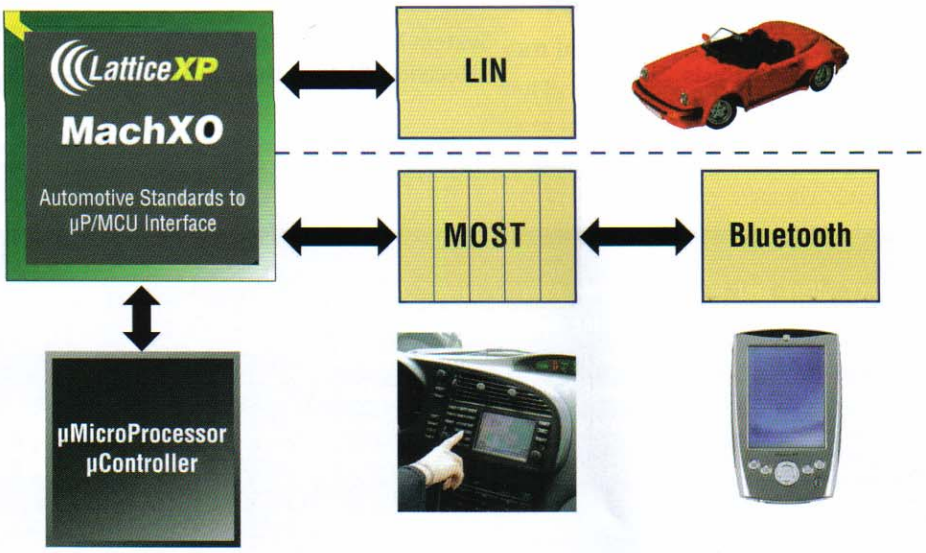
FPGAs with embedded flash technology can help reduce the cost of a flexible interface. **Bernie Perrin** explains.

Today's consumers expect electronic convenience and luxury in their automobiles and it is no surprise that automotive electronics are no longer exclusively dedicated to the engine management system or body control, but have expanded into new areas such as infotainment, communications and driver / passenger assistance systems. For instance, the rapid evolution of 8-tracks to audiotapes to compact discs to MP3 players continues to serve as a reminder to automobile designers of the relatively short lifecycle of in-car electronics. Emerging and changing automobile standards are further reason to choose standards based upon longevity, flexibility and broad acceptance.

Additional challenges for automotive electronic component designers continue to be low-cost targets, extended temperature and small form-factor requirements. As FPGA's have evolved over the past decade, providing increased performance, lower power consumption, extended temperatures, small form-factor and low-cost, they have become increasingly attractive to automotive designers.

Changes can be readily implemented even after field deployment, through programming of the FPGA. This is referred to as in-system programmability (ISP), and can be accomplished through standard programming protocols such as IEEE1149.1 JTAG. Designers are able to update in-car electronics in the same manner as an engine tune-up that is carried out as part of a regularly scheduled maintenance programme.

In addition to the implementation of the CAN bus for high-performance in-vehicle network applications, the Local Interconnect Network (LIN) bus is increasingly being implemented to connect together distributed nodes with low communication requirements along with the Media Oriented Transport System (MOST) bus for multimedia requirements. This multi-bus approach to automotive electronics design and the constantly evolving



nature of the bus standards coupled with the automotive industry's incessant drive for cost minimisation, extended temperature requirements, lower power consumption and smaller form factors, is presenting automotive engineers with some interesting challenges in terms of the necessary interface bridging.

As well as supporting complex, DSP-based devices, MOST technology provides a low overhead, low-cost network interface to the simplest multimedia device, maximising the flexibility of the overall automotive communication system. The versatile, high-performing, low-cost multimedia fibre-optic network technology is based on synchronous data communication and is ideal for multimedia applications such as analog audio gateways, analog video interface, digital video display interface, navigation and communication in automobiles. The different layers within the MOST standard cover a wide range of applications ranging from a few kbps up to 24.8Mbps.

MOST technology is similar to a switched telephone in that it is a synchronous network. This technology eliminates the need for buffering and sample rate conversion, so very simple and inexpensive devices can be connected. Defining data and control channels identify incoming and outgoing data channels, allowing continuous flow, without the need to further process packet information.

A LIN network is primarily targeted at automotive applications using smart sensors, actuators or illumination that are easily connected to the car network and accessible to all type of diagnostics and services.

The synchronisation mechanism feature allows clock recovery by slave nodes without additional quartz or ceramic resonators. The specification of the line driver and receiver complies with the ISO 9141 single-wire standard, with additional enhancements. Maximum speed is 20kbit/s; this limitation stems from EMI considerations as well as clock synchronisation mechanisms.

Comprising of one master node and one or more slave nodes, the communication in an active LIN network is always initiated by the master task, which sends a message header comprised of the synchronisation break, the synchronisation byte and the message identifier. Exactly one slave task is activated upon reception and filtering of the identifier and initiates the transmission of the message response, comprising of two, four or eight data bytes and a checksum byte. The header and the response part form one message frame.

Low-cost FPGA devices are well suited to implement the LIN standards and provide

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added flexibility in interfacing to the microprocessors or microcontrollers of choice. Clock synchronisation and the single-wire medium are major factors in the cost efficient of LIN, with the low-cost, low-speed LIN implementation requiring relatively modest FPGA resources, approximately 500 LUT's and 42 I/O's.

The bridging implementation of various automotive bus standards to a microprocessor or a microcontroller interface can be simplified on a single platform; this not only simplifies the inventory process automotive manufacturers by allowing them to scale the electronic content and options for each grade of car, using the same FPGA ordering part number, but greatly increases cost savings due to volume pricing.

Cost savings continue throughout the life cycle of the automobile as through reprogramming or reconfiguring, the FPGA can accommodate upgrades without incremental non-recurring engineering changes, as in an ASIC implementation. Several FPGA manufacturers offer density migration within the same package footprint.

A designer using an FPGA implementation has the option to choose either cost effective microprocessors or microcontrollers or those with rich feature sets, directly controlling the total solutions cost of electronic content.

A cost saving feature offered by the new LatticeXP and LatticeXO devices, is that they have embedded FLASH memory to hold the configuration data. Traditionally, SRAM-based FPGAs have required expensive, proprietary non-volatile boot PROMs, supplied by the FPGA vendor. These PROMs can account for over 35% of the total FPGA solution cost. In contrast the LatticeXP and LatticeXO are single chip devices, with the additional capability of being "instant-on". The low-cost devices can be in-system reconfigured in less than a millisecond and are ideal for high-volume applications.

Conclusion

Maximum flexibility and adaptability are essential considerations for automotive designers as new automotive standards continue to emerge. Use of the LatticeXP and LatticeXO devices provides automotive designers to easily accommodate changing and emerging bus standards after initial deployment and realise a lower total cost solution of 30% to 50% when compared to existing FPGA solutions.

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