



# **Low-Cost Automotive Multi-Bus Bridging Using LatticeECP/EC FPGAs**

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## ***Introduction***

The electronics content in automobiles continues to grow rapidly, and it is reasonable to compare the growth of automotive electronics with the growth of consumer electronic portable products. Today's consumers expect the same electronic convenience and luxury in their automobiles as they do in their hand-held portable electronic devices. No surprise, then, that automotive electronics are no longer exclusively dedicated to the engine management system or body control, but have expanded into new areas such as infotainment, communications and driver/passenger assistance systems.

A daunting design challenge is matching the lifetime of the automobile with that of the in-car electronics, in order to avoid increased cost due to obsolete technologies and outdated equipment. The rapid evolution of 8-tracks to audiotapes to compact discs to MP3 players continues to serve as a reminder to automobile designers of the relatively short lifecycle of in-car electronics. Emerging and changing automobile standards are further cause to choose standards based upon longevity, flexibility and broad acceptance. The standards currently in use include, among others, Local Interconnect Network (LIN), Control Area Network (CAN), Media Oriented System Transport (MOST<sup>®</sup>) and Bluetooth.

Additional challenges for automotive electronic component designers continue to be low-cost targets, extended temperature and small form-factor requirements. As programmable logic devices (PLDs) have evolved over the past decade, providing increased performance, lower power consumption, extended temperatures, small form-factor and low-cost, they have become increasingly attractive to automotive designers.

According to industry analyst Gartner Dataquest (November 2004), the worldwide automotive electronics application segment is expected to grow from approximately \$79.1 billion in 2004 to \$84.2 billion in 2005 to \$88.4 billion in 2006. The key automotive electronic systems include GPS navigation systems, engine control units and digital stereo.

## ***Programmable Logic Device (PLD) Benefits***

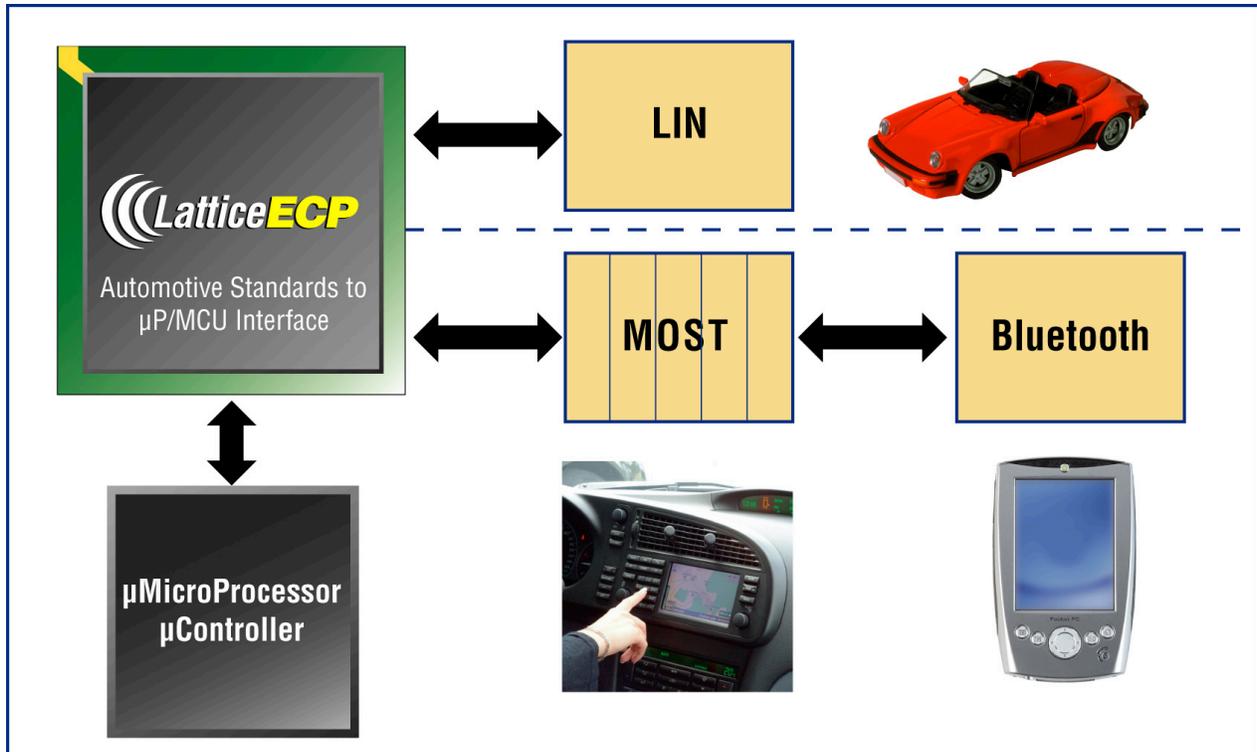
Due to the reprogrammable and flexible nature of PLDs, they are well suited to adapt to inevitable changes. Evolving standards can be readily implemented, even after field

deployment, through reprogramming of the PLD. The reprogramming is done with the system in place, without having to physically remove the PLD. This is referred to as in-system programmability (ISP), and can be accomplished through standard programming protocols such as IEEE1149.1 JTAG. Designers are able to update in-car electronics much like an engine tune-up. Indeed, it is not much of an exaggeration to suggest that an automotive electronics update will become as commonplace as a regularly scheduled maintenance program.

Of course, cars vary in class, from economy to standard to luxury models. In turn, in-car electronics vary according to the class of the car. Again, recognizing the reprogrammability and flexibility of the PLD, automotive designers are able to offer various feature sets, from standard to elaborate, on the identical platform. This helps to explain why an application specific integrated circuit (ASIC) is typically not considered, despite its advantage of lower manufacturing cost. By definition, the high NRE (non-recurring expense) and, more importantly, the inflexibility of an ASIC bridging implementation eliminate it as a viable solution.

## ***Bridging Functions***

The microprocessor or microcontroller is the heart of the automotive electronics system. A field programmable gate array (FPGA) PLD is a good choice to achieve the interface bridging of various automotive bus standards to a microprocessor or microcontroller interface. Below are two examples of a low-cost yet flexible bridging implementation of two popular automotive bus protocols, LIN and MOST, to either a microprocessor or a microcontroller interface. Central to the success of these applications is that the FPGA's flexible architecture and reprogrammability enable it to interface with many microprocessors or microcontrollers, resulting in maximum flexibility for the designer. Simple reprogramming of the FPGA is all that is necessary to implement new requirements, or any modifications to the existing design, without changing components.



## Flexible Multi-Bus Bridging Using Low-Cost FPGAs

### ***Local Interconnect Network (LIN)***

Intellectual property (IP) cores for automotive bus standards, such as LIN and CAN, are now readily available. LIN is a low-cost, single-wire (12Volt bus) serial communications protocol based on the common Serial Communications Interface (UART) data format and a single-master/multiple-slave concept intended for use in distributed electronic systems in automobiles. This low-cost network system is designed to connect distributed nodes with low communication requirements, and is not intended to replace high-performance networks such as CAN. LIN is primarily targeted at automotive applications using smart sensors, actuators or illumination. These can be connected easily to the car network and become accessible to all types of diagnostics and services.

A notable feature of LIN is the synchronization mechanism that allows clock recovery by slave nodes without additional quartz or ceramic resonators. The specification of the line driver and receiver complies with the ISO 9141 single-wire standard, with additional enhancements. The maximum transmission speed is 20kbit/s; this limitation stems from EMI considerations as well as clock synchronization mechanisms.

A LIN network is comprised of one master node and one or more slave nodes. All nodes include a slave communication task which includes transmit and receive tasks, while the master node includes an additional master transmit task. The communication in an active LIN network is always initiated by the master task: it sends a message header comprised of the synchronization break, the synchronization byte and the message identifier.

Exactly one slave task is activated upon reception and filtering of the identifier, and initiates the transmission of the message response. The response is comprised of two, four or eight data bytes and a checksum byte. The header and the response part form one message frame.

The clock synchronization, the simplicity of UART communication and the single-wire medium are the major factors in the cost efficiency of LIN. The low-cost, low-speed LIN implementation requires relatively modest FPGA resources: approximately 500 LUTs and 42 I/Os. Consequently, low-cost FPGA devices are well suited to implement the LIN standards, and provide added flexibility in interfacing to the microprocessors or microcontrollers of choice.

## ***Media Oriented System Transport (MOST)***

The MOST technology provides a low overhead, low-cost network interface to the simplest multimedia device. MOST supports devices with low intelligence as well as much more complex, DSP-based devices that require sophisticated control and multimedia capabilities. This design principle maximizes the flexibility of the overall automotive communication system. At a high level, it is a versatile, high-performance and low-cost multimedia fiber-optic network technology based on synchronous data communication. MOST is ideal for multimedia applications such as analog audio gateways, analog video interface, digital video display interface, navigation and communication in automobiles. There are different layers within the MOST standards, such as PHY, transceiver/data link, transport, session, and others, all of which cover a wide range of applications ranging from a few kbps up to 24.8Mbps.

MOST is a synchronous network. A timing master supplies the clock, and all other devices synchronize their operation to this clock. This technology eliminates the need for buffering and sample rate conversion, so very simple and inexpensive devices can be connected. The technology is similar to a switched telephone network. There are data channels and control channels defined. The control channels are used to identify which data channels the sender

and receiver are to use. Once the connection is established, data can flow continuously and no further processing of packet information is required. This is the optimum mechanism for delivering streaming data.

The key benefits of the MOST network include ease of use, low-cost implementation, a wide range of applications, synchronous and asynchronous bandwidth, flexibility and synergy with the consumer and personal computer industries.

## ***Cost Savings***

With the inherent flexibility and reprogrammability of the FPGA, the bridging implementation of various automotive bus standards to a microprocessor or a microcontroller interface can be simplified on a single platform; this enables automotive manufacturers to scale the electronic content and options for each grade of car, from economy to luxury, using the same FPGA ordering part number. The resulting inventory simplification and volume pricing lead to cost savings for development, production, servicing and logistics.

The cost savings realized by using an FPGA continue throughout the life cycle of the automobile as well. Through reprogramming or reconfiguring, the FPGA can accommodate upgrades without incremental non-recurring engineering charges, which would be the case with an ASIC implementation. Further, several FPGA manufacturers offer density migration within the same package footprint: i.e., more logic capacity can be had within the original PCB design, extending the life of the electronic platform as system requirements inexorably change.

Not only do these capabilities and advantages make FPGA devices more attractive to designers, they permit a broad choice of microprocessors and microcontrollers as well. Designers using an FPGA implementation have the option to choose either cost effective microprocessors or microcontrollers, or to choose those with rich feature sets. This flexibility contributes directly to the lower total solutions cost of electronic content in the automobile.

Another cost saving feature, offered only by the new LatticeECP and LatticeEC FPGA devices, is standard SPI memory configuration support. Traditionally, SRAM-based FPGAs have required expensive, proprietary non-volatile boot PROMs, supplied by the FPGA vendor. These PROMs can account for over 35% of the total FPGA solution cost. In contrast, low-cost,

industry standard SPI memories are ideal for high-volume applications. They offer fast configuration times, the lowest cost and a smaller PCB footprint. With its ECP and EC devices, Lattice is the first FPGA vendor to provide standard SPI memory configuration support.

## ***Summary***

With new automotive standards continuing to emerge, implementation of these interfaces with maximum flexibility and adaptability are essential considerations for automotive designers. The LatticeECP and LatticeEC families are designed to provide exceptional functionality, performance and value. Employing an extremely efficient architecture (high-volume, production proven 130nm technology), these low-cost FPGAs deliver performance DSP blocks, sysMEM embedded Ram blocks, distributed memory, sysCLOCK PLLs, DDR memory interface, sysIO buffers and more, making these devices very well suited for automotive applications. Using the LatticeECP and LatticeEC FPGAs, automotive designers will be able to accommodate changing bus standards, adopt with comparative ease new and emerging standards after initial deployment, and realize a lower total cost solution of 30% to 50% when compared with existing FPGA solutions.

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