



DYNAMIC POWER MANAGEMENT IN AN EMBEDDED SYSTEM

A Lattice Semiconductor White Paper

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A Flexible Dynamic Power Management Solution

What is Dynamic Power Management?

A key product differentiator in an embedded system is power efficiency, because lower power results in lower operating costs, lower fan noise, and lower cooling requirements. Designers of modern embedded systems therefore focus on increased system performance while reducing operating power consumption. Increasing the operating frequency, or using more powerful, higher density VLSI ICs -- or both -- achieves increased system performance, but increasing the performance level inevitably increases power consumption. One option to reduce system-level power consumption is to use low static power devices. Power consumption also can be controlled during system operation depending upon the processing load. This latter approach is called Dynamic Power Management.

Methods Used to Control Power Consumption

In digital systems based on CMOS technology, the following equation describes the relationship between power consumption and operating frequency and voltage.

$$\text{System Power Consumption} _ C * V^2 * F$$

Where C is the total capacitance of all the circuits that need to be charged during signal transitions. V is the Voltage applied to the devices and F is the frequency of signal toggle.

As the equation illustrates, reducing the operating voltage or frequency, or both, can result in lowering overall system power consumption, and that is the underlying principle of Dynamic Power Management. Dynamic Power Management identifies low processing requirement periods and reduces operating voltage (voltage scaling) and frequency (frequency scaling), resulting in reduced average operating power consumption. Additionally, during these lean

periods, idle sections of the circuit board also can be turned off to further reduce power consumption.

During system operation, the extent of voltage or frequency reduction from its maximum value is determined on the fly by software. This white paper describes a circuit that operates as a peripheral to this power management software.

Issues with Dynamic Power Management Methods

There are a number of issues of which a designer should be aware when designing a system with dynamic power management capability, including:

1. Operating voltage & frequency scaling latency – Power supplies require a finite amount of time to ramp to the new operating voltage, and this delay is usually a function of load on the power supply bus. But for the Clock generator, the time required to shift between frequencies can be very short. Therefore, the operating system has to monitor the operating voltage and determine when the operating frequency should be changed.

2. Processors may not operate reliably during voltage or frequency transition -- Many CPUs, capable of operating at different voltages and at corresponding frequencies, may not operate reliably when their power supply voltage or input clock frequency is changing. In such cases, it is advisable to halt the CPU during the voltage and frequency transition. This requires external hardware to monitor the voltage and clock frequency and prevent the CPU from execution during transition.

3. CPUs with integrated PLLs usually generate the required frequency for the integrated peripherals and also provide the clock for the external bus interface -- If the CPU clock frequency were changed, the PLL would have to be reprogrammed to maintain operating frequency for the external peripherals, which are not designed to operate at different frequencies. CPUs with on-chip PLL may put the restriction on the range of frequency scaling. An external PLL can easily overcome this restriction and extend the range of power saving while

also meeting the clocking requirements of other peripherals used on the circuit board.

Implementing Dynamic Power Management With ispPAC Power Manager and ispClock

Figure 1 shows the block diagram of a circuit board implementing the power management functions. Together, the power management algorithm implemented in software, and the Voltage Scaling and Frequency Scaling Unit implemented in hardware, control overall board power consumption by:

1. Controlling the operating clock frequency of the CPU and the board circuitry
2. Controlling the core supply voltage to the CPU
3. Turning the circuit on the secondary power plane off during idle periods

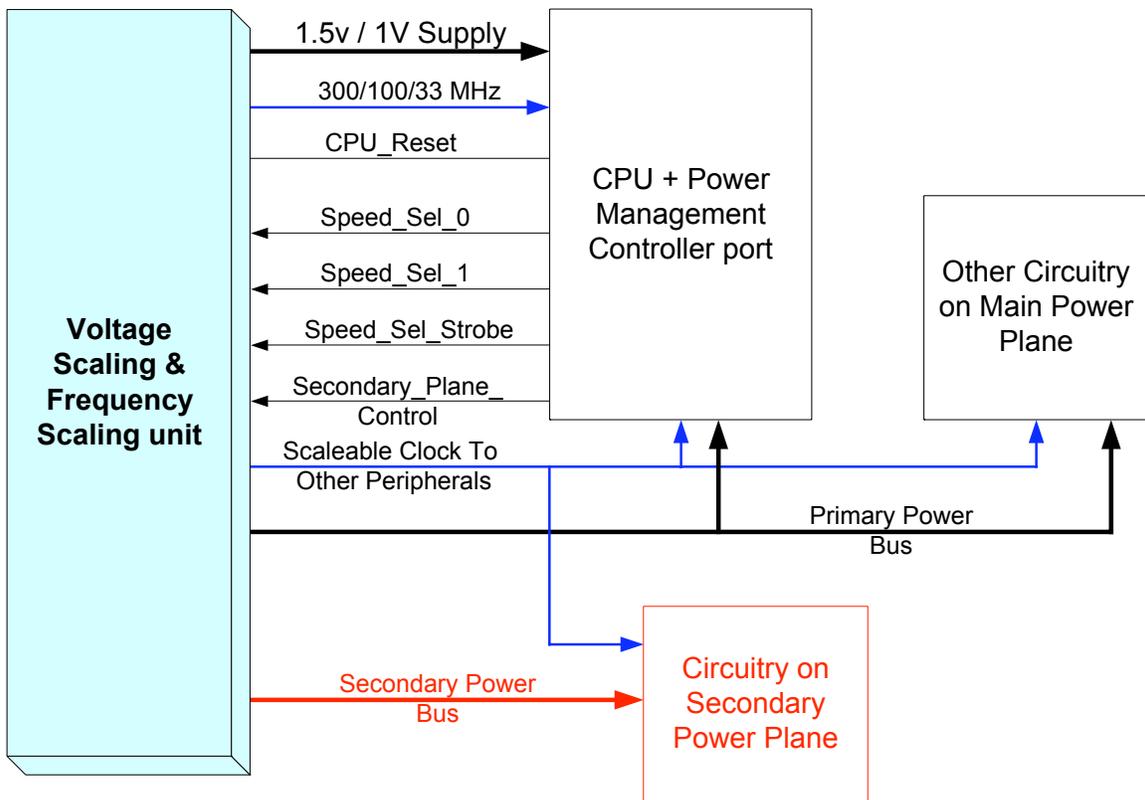


Figure 1 – Block Diagram of Dynamic Power Management Implementation

Block diagram description

From the left, the Voltage Scaling & Frequency Scaling unit block accepts a command from the power management port (at the top middle portion of the block diagram) and generates the required core voltage and CPU clock frequency, and also turns the secondary power bus on/off.

The power management signals are

Speed_Sel_0, Speed_Sel_1 – These are the command signals and are decoded as follows:

00 - Full Power, CPU Voltage = 1.5V, Operating Frequency = 300 MHz

01 - Medium Power, CPU Voltage = 1.0V, Operating Frequency = 100 MHz

10 - Low Power, CPU Voltage = 1.0V, Operating Frequency = 33 MHz

11 - Controls the second power plane using the signal

Secondary_Plane_Control -

0 - Turn secondary plane off and 1 = secondary plane on

Speed_Sel_Strobe - latches the command from the power manager controller port

The remaining circuitry on the board is divided into the primary power plane circuitry and the secondary power plane circuitry.

Together, the Lattice ispPAC Power Manager and ispClock5620 devices provide an extremely convenient mechanism to implement a wide range of Dynamic Power Management functionality. Before discussing the detailed circuit diagram description, the following section provides a brief description of the ispClock device.

Description of ispClock5600 Features

The two members of the ispClock5600 family, the 10-output ispClock5610 and 20-output ispClock5620, combine a high-performance clock generator with a flexible, Universal Fan-out Buffer. The on-chip clock generator can provide up to 5 clock frequencies, ranging from 10MHz to 320MHz, using a high-performance PLL and clock multiply and divide facilities. The Universal Fan-out Buffer can

drive up to 20 clock nets using either single-ended or differential signaling, with individual output control for improved signal and timing integrity. The devices provide an unprecedented level of performance and flexibility in support of high-performance clock network designs on electronic circuit boards.

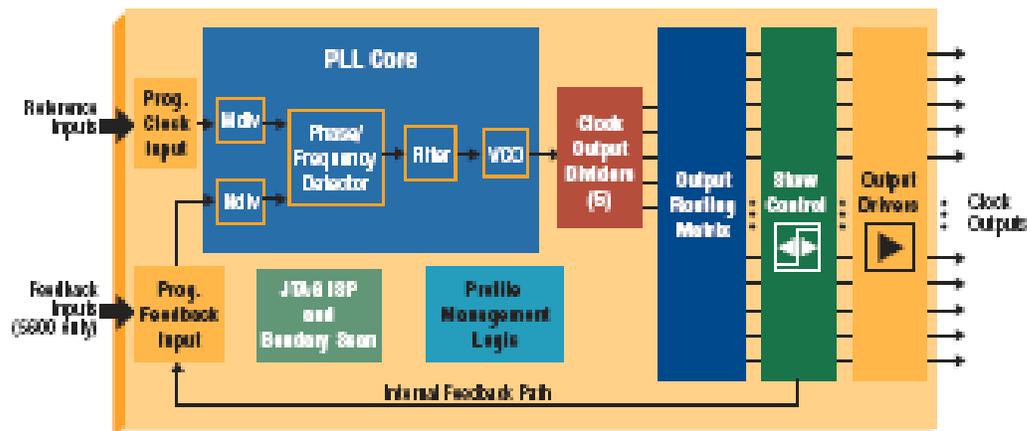


Figure 2 – Block diagram of ispClock5620

Programmable I/O section - The input section consists of two hardware selectable multiplexed clock inputs. The output section consists of up to 20 low-skew clock outputs. Both the reference clock input and the clock outputs can be individually programmed to interface to single ended logic (LVTTTL, LVCMOS, SSTL, HSTL) and differential logic (LVDS, LVPECL, Differential HSTL, Differential SSTL) types. Input and output termination resistance can be programmed between 40 to 70 ohms in 5-ohm steps. The output skew of each clock output can be individually set to one of 16 steps, with resolution to 195ps. The skew step size is derived from the PLL frequency and therefore is very precise. The frequency synthesis unit is able to generate up to 5 clock frequencies. The non-blocking output switch matrix can switch any frequency to any output. The input frequency range is from 10MHz to 320MHz, and the output frequency range is from 5MHz to 320 MHz.

PLL Core - The heart of the device is the high performance PLL core, consisting of a Phase Frequency Detector (PFD), Programmable on-chip filter, and VCO.

The PLL core is able to lock to inputs ranging from 10 MHz to 320 MHz, while the output frequency range is between 320 to 640 MHz. Output jitter is < 100ps.

Frequency Synthesis Dividers - The device has seven 5-bit counters: M, N, and five V Counters. The M, N, and one V counter provide 5-bit resolution to set the operating frequency of the PLL. The output of the PLL then drives the remaining V-dividers, resulting in the synthesis of five independent frequencies related only by the PLL operating frequency.

JTAG Programming and Boundary Scan Interface - While the device can be fully programmed using the JTAG interface, it also can be used for testing circuit board interconnection using standard in-circuit testers.

Profile Management - The device can store up to four independent configurations – (M, N, and V counters, Skew) enabling the selection of four sets of independent clock frequencies.

The frequency scaling functionality of the circuit makes use of the profile management feature of the ispClock to provide three clock frequencies, 300MHz, 100 MHz and 33 MHz to the CPU. However, the remaining outputs can be programmed to provide four sets of three clock frequencies, different from that of the CPU clock, using the remaining V counters, all controlled by the same profile select pins. Additionally the design uses the synchronous gating (Sync_gate) signal of the ispClock to prevent runt clock cycles.

The following table lists various configuration values under different profiles:

Profile	Input Clock	M Divider	N Divider	Vdivider in Feedback	PLL Operating Frequency	Output V-Divider	Output Frequency
00	100 MHz	1	3	2	600 MHz	2	300 MHz
01	100 MHz	1	3	2	600 MHz	6	100 MHz
10	100 MHz	1	3	2	600 MHz	18	33.33 MHz

Detailed Voltage and Frequency Scaling Circuit Description

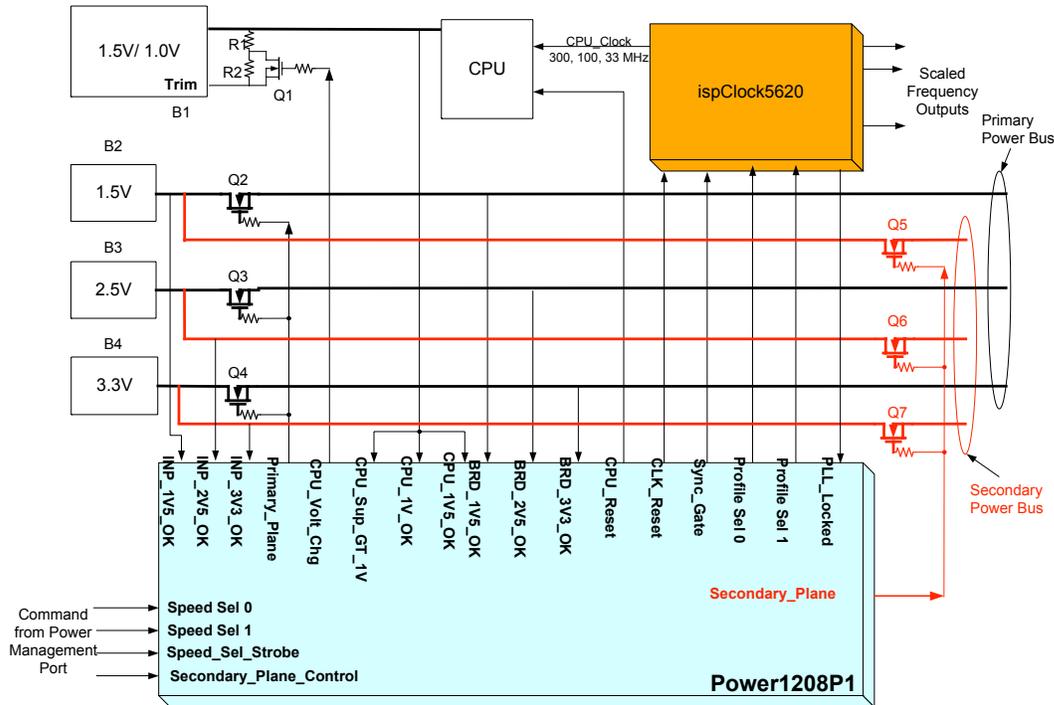


Figure 3 - Voltage Scaling and Frequency Scaling Unit

Figure 3 shows the Power1208P1 (ispPAC-POWR1208P1) device, which provides all the logic for voltage and frequency scaling functions. It also drives the ispClock5620 device, taking Voltage transition and Frequency transition latencies into consideration, and independently controls the secondary power supply plane following the command from the Power Management port. The ispClock5620 device generates the various clock frequencies required for frequency scaling. In total there are 20 clock outputs, which can be programmed to generate different clock frequencies for different sections of the circuit board.

The functions of the Power1208P1 are:

Register and execute Commands from the Power management Control port

Control Switching B1 supply Voltage between 1.0V and 1.5V

Monitor all Power Supply Voltages

Generate Control signals for ispClock to Switch between output frequencies

- Profile select
- Reset the ispClock device after Profile switch
- Control Clock gating during Power Supply voltage variation and clock

frequency switch over

Turn on primary power bus with tracking

Secondary power bus control with tracking

Pulse-stretch the CPU_Reset Signal during power on, and activate CPU_reset in case of power supply fault.

Functions of ispClock5620

Only three of the four profiles of ispClock are configured to generate different clock frequencies. While this white paper discusses only the change in frequency for the CPU, the same mechanism can also be applied to all the remaining clock outputs.

Circuit operation of power supply B1 - The output voltage of the power supply brick B1 on the top left side of Figure 3 can be set to 1.5 Volts by connecting resistor R1 + R2 between the trim pin and the output voltage pin. If only R1 is connected between the output and trim inputs, the output voltage will be at 1.0V. The MOSFET Q1, when turned on, shorts the resistor R2. This results in output voltage of B1 to transition to 1.0V. However, when the Q1 is turned off, the output voltage of the brick will transition to 1.5V. Controlling the ramp rate of HVOUT pin driving the MOSFET Q1 can limit the current inrush during the voltage transition from 1V to 1.5V, and vice versa.

The following table lists all the pins of Power1208P1 and their functions:

Power1208P1 Input Pin Name	Function Performed
Voltage Monitoring Inputs	
Inp_1V5_OK	Indicates that input power supply voltage of the 1.5V brick above the lower limit of 1.5V
Inp_2V5_OK	Indicates that input power supply voltage of the 2.5V brick above the lower limit of 2.5V
Inp_3V3_OK	Indicates that input power supply voltage of the 3.3V brick above the lower limit of 3.3V
CPU_1V5_OK	Indicates that CPU's voltage is above lower limit of 1.5V Range
CPU_Sup_GT_1V	Indicates to the logic that CPU voltage is greater than 1V and hence is beyond the limit of 1V operating Spec of CPU
CPU_1V_OK	Indicates that CPU's voltage is above lower limit of 1V Range
Brd_1V5_OK	Indicates that the power supply voltage of the 1.5V bus above the lower limit of 1.5V
Brd_2V5_OK	Indicates that the power supply voltage of the 2.5V bus above the lower limit of 2.5V
Brd_3V3_OK	Indicates that the power supply voltage of the 3.3V bus above the lower limit of 3.3V
Logic Inputs	
Speed_sel_0	Command input bit 0 from the Power Management Port
Speed_sel_1	Command input bit 1 from the Power Management Port
Speed_Sel_Strobe	Strobe signal from Power Management port to latch the command in the Power Manager device
Secondary_Plane Control	This input turns the secondary plane on/off when the power management port command is 11.
PLL_Locked	Signal from the ispClock5620 that the PLL has locked to new operating frequency

Power1208P1 Output Pin Name	Function Performed
MOSFET Drive Outputs	
Primary_Plane	Drives 3 MOSFET outputs together so that the primary power supplies 3.3V, 2.5V & 1.5V track
Secondary_Plane	Drives 3 MOSFET outputs together so that the secondary power supplies 3.3V, 2.5V & 1.5V track. This is controlled by the Power Management port
CPU_Volt_Change	Drives the MOSFET that shorts the resistor R2 controlling the output voltage of the CPU power supply to toggle between 1.5V & 1V
Logic Outputs	
CPU_Reset	Drives the Reset of the CPU and is active for 100 ms after the supplies are turned on and this signal is activated when there is a power supply fault
CLK_Reset	Resets the clock chip when the output clock frequency is changed
Sync_Gate	Synchronously stops the output clock during voltage transition or frequency transition
Profile_Sel_0	Selects the ispClock5620 output frequency
Profile_Sel_1	Selects the ispClock5620 output frequency

Timing Diagrams

The timing diagram in figure 4 shows the operation of the circuit above. The top section is the command from the Power Management Control Port. The Power1208P1 and the ispClock5620 devices execute the commands and the steady state is reached safely after the power supply voltage and the clock frequencies reach the steady state.

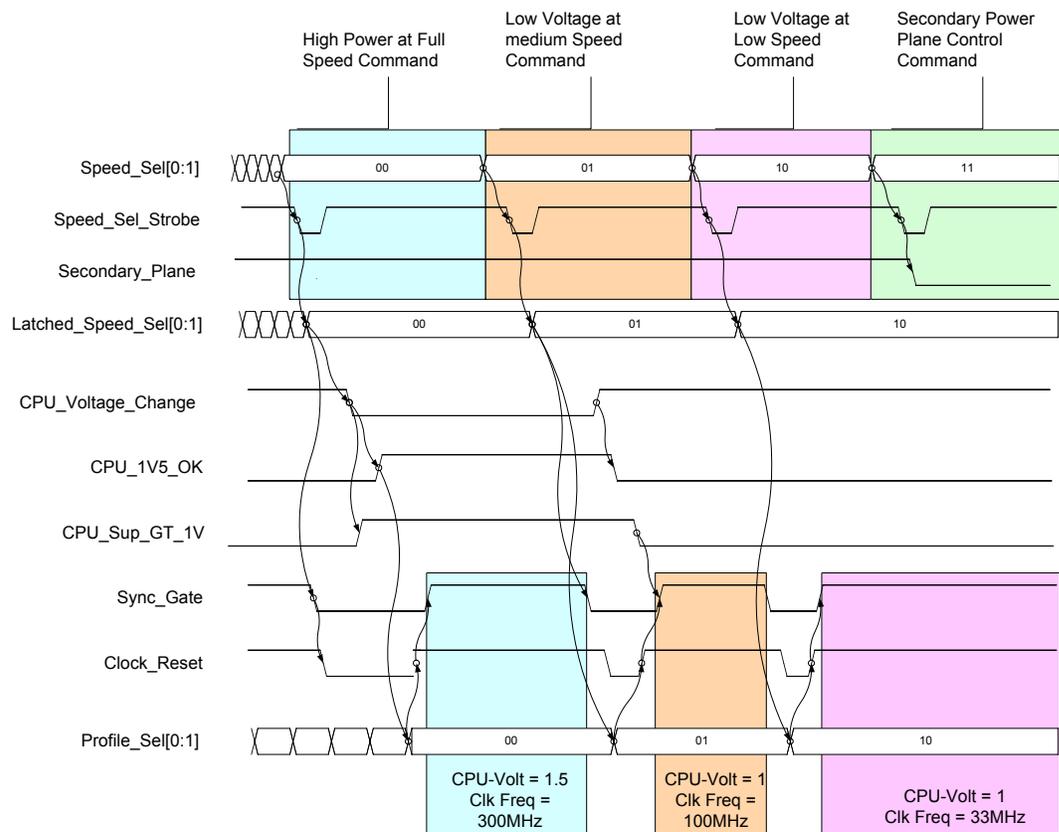


Figure 4 – Circuit Timing Diagrams

Conclusion

The design described above provides the most flexibility in the smallest circuit board area. This design can be adapted across a wide variety of designs.

The ispClock5620 device is ideally suited for the clock frequency scaling function, because it is able to replace four independent clock generator devices and the associated, expensive logic circuit required to multiplex various clock buffer, to a single clock net. The resulting solution is flexible and high performance.

The Power1208P1 device used in this design combines the ability to monitor logic signals as well as power supply voltages. The logic section of this device is able to conveniently integrate all the logic functions required to switch reliably between different operating speeds, while controlling power supply voltages as well as monitoring the CPU voltage rail. The resulting design switches between configurations safely.

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