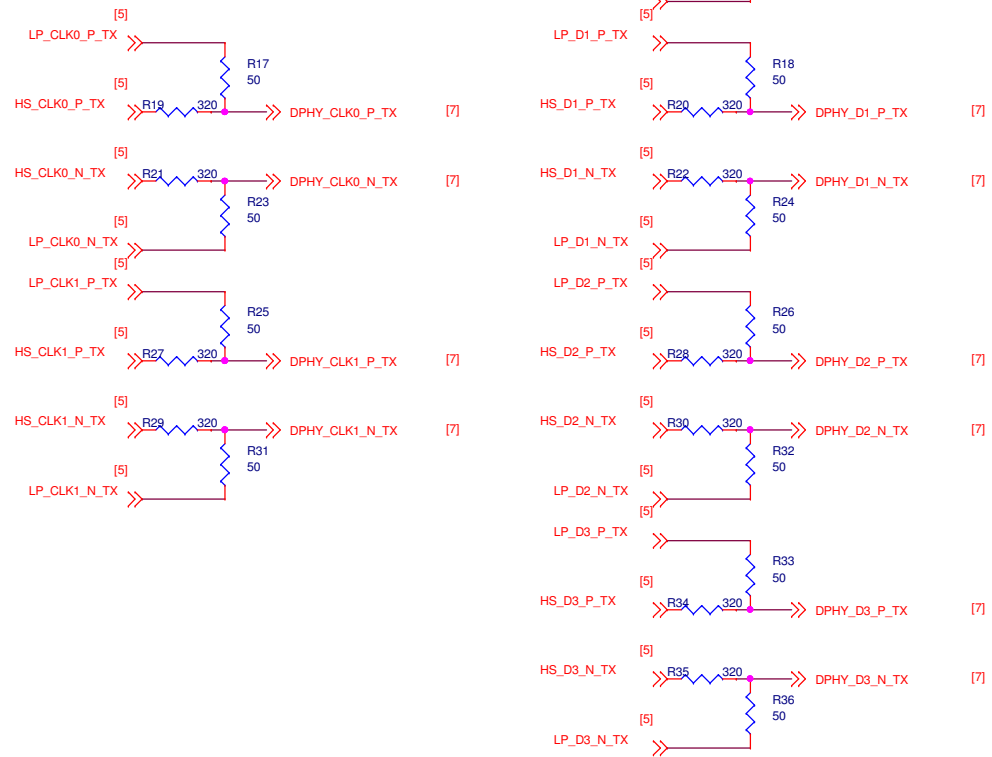


Place resistor networks as close to Bank 0 pins as possible and trace match all diff signals between P and N as well as between pairs

LP_* Signals are only needed if you intend on monitoring LP signals from within the FPGA. If monitoring LP signals from within the FPGA is not needed 100 ohm parallel termination can be used in place of the resistor network for those pairs. It is recommended to use the 50 ohm resistor network on at least the clock lanes and data lane 0 for DSI. For CSI-2 100ohm termination is sufficient for all data and clock lanes in most cases.

XO2 DPHY RX Resistor Networks

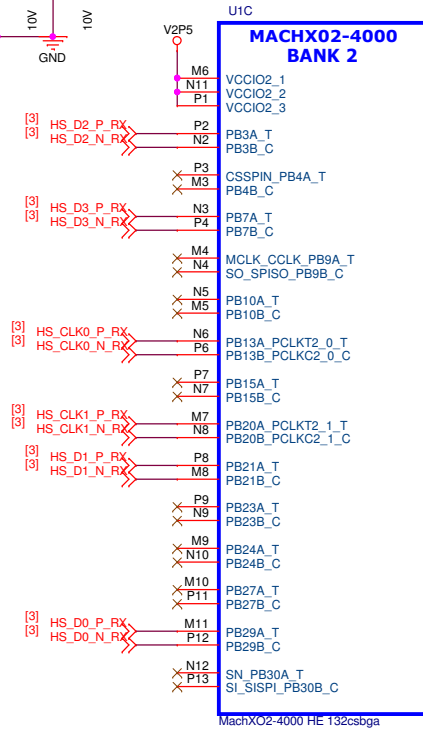
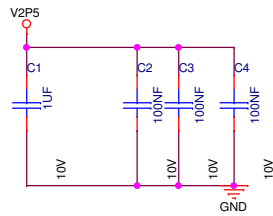
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Place resistor networks as close to Bank 0 pins as possible and trace match all diff signals between P and N as well as between pairs
 If LP mode is not needed the LP_* signals can be removed with the 50ohm resistors connected to ground

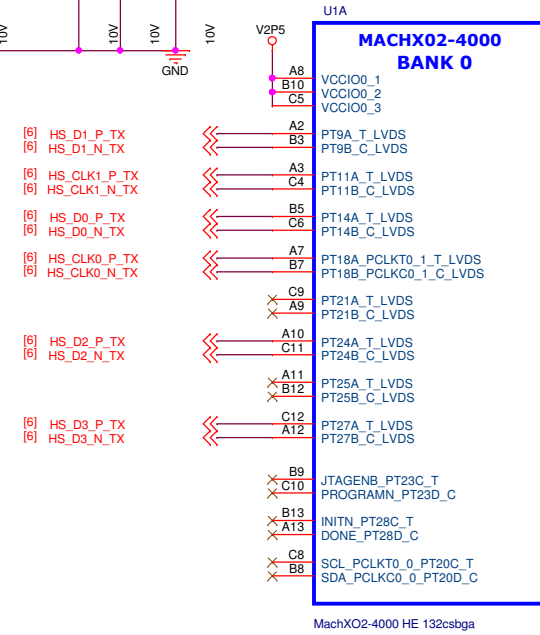
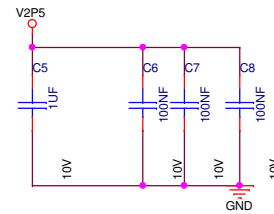
X02 DSI TX Resistor Networks

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HS_* signals must be trace length matched between P and N of a pair as well as between the individual pairs

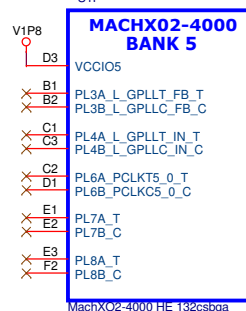
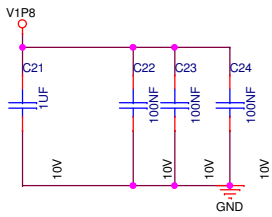
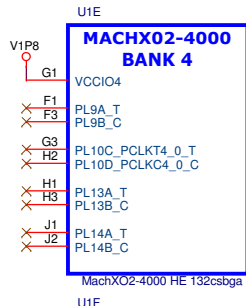
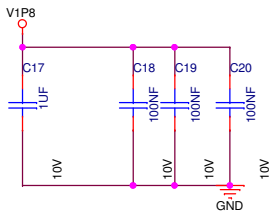
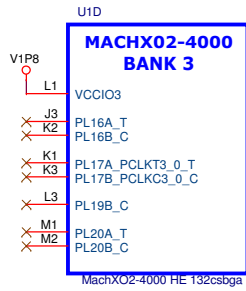
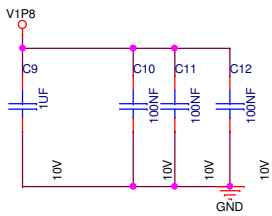
XO2 MIPI HS RX Signals



HS_* signals must be trace length matched between P and N of a pair as well as between the individual pairs

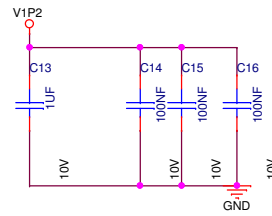
XO2 MIPI HS TX Signals

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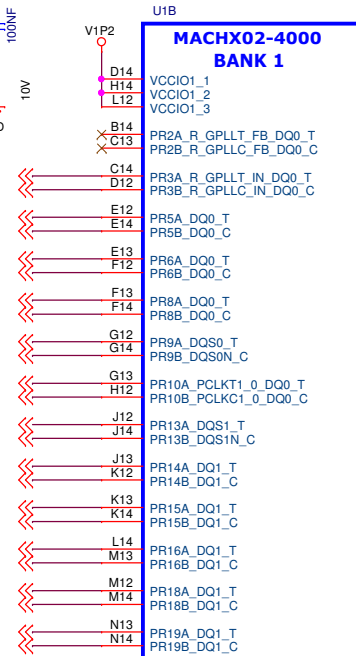


For XO2-1200 compatibility, VCCIO3 = VCCIO4 = VCCIO5

Extra Banks

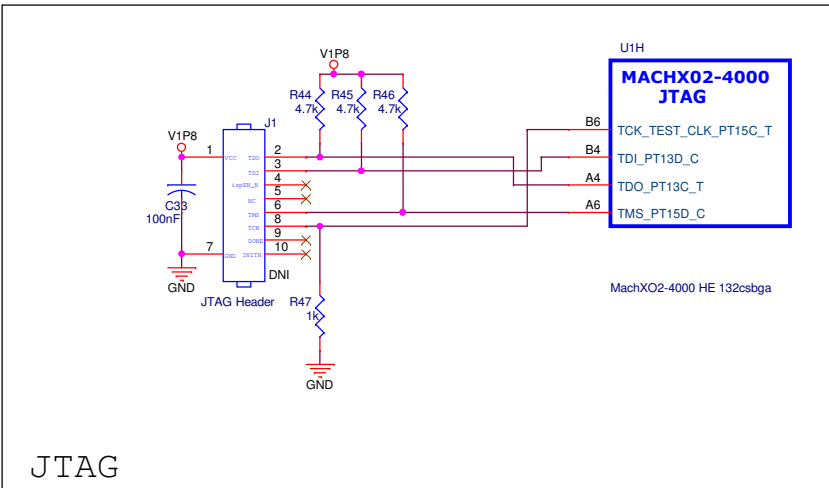
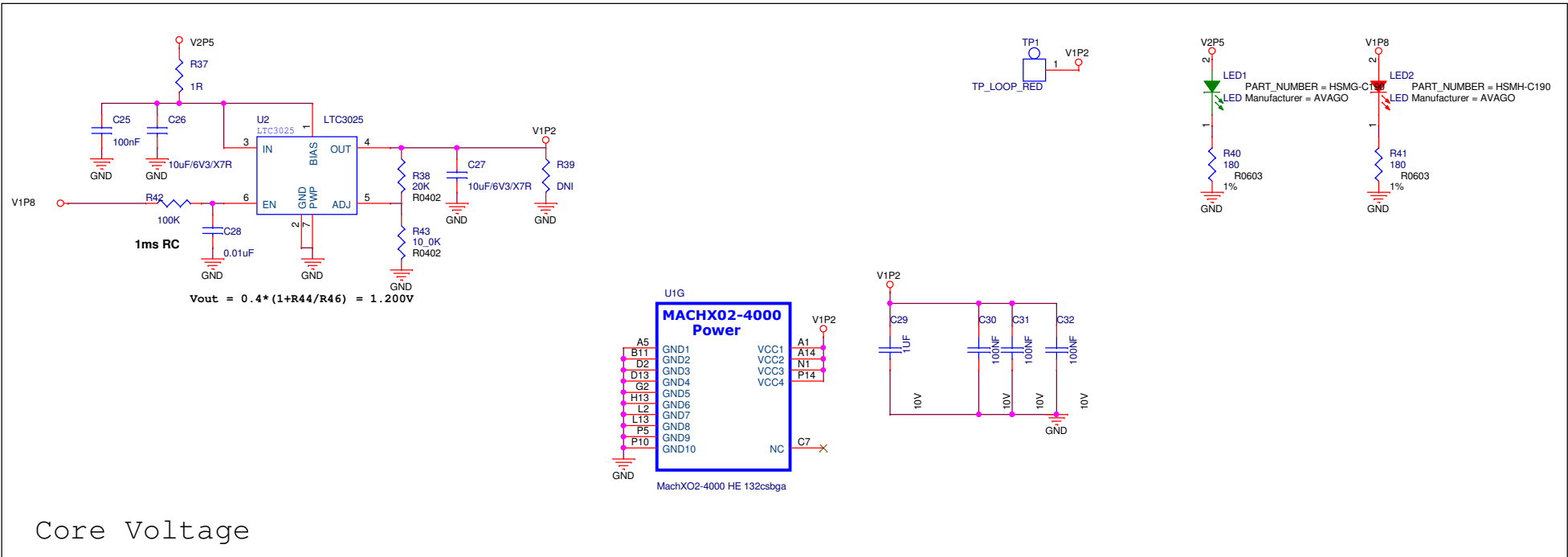


- [6] LP_CLK1_P_TX
- [6] LP_CLK1_N_TX
- [6] LP_CLK0_P_TX
- [6] LP_CLK0_N_TX
- [6] LP_D0_P_TX
- [6] LP_D0_N_TX
- [6] LP_D1_P_TX
- [6] LP_D1_N_TX
- [6] LP_D2_P_TX
- [6] LP_D2_N_TX
- [6] LP_D3_P_TX
- [6] LP_D3_N_TX
- [3] LP_CLK1_P_RX
- [3] LP_CLK1_N_RX
- [3] LP_CLK0_P_RX
- [3] LP_CLK0_N_RX
- [3] LP_D0_P_RX
- [3] LP_D0_N_RX
- [3] LP_D1_P_RX
- [3] LP_D1_N_RX
- [3] LP_D2_P_RX
- [3] LP_D2_N_RX
- [3] LP_D3_P_RX
- [3] LP_D3_N_RX



XO2 MIPI LP RX and TX Signals

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