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## Revision History

<table>
<thead>
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<th>Version</th>
<th>Changes</th>
</tr>
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<tbody>
<tr>
<td>2.0</td>
<td>Added Version Number to document. Added sections on Default Signal Values for unconnected ports.</td>
</tr>
<tr>
<td>2.1</td>
<td>Added PLL primitives</td>
</tr>
<tr>
<td>2.2</td>
<td>Corrected SB_CARRY connections to LUT inputs</td>
</tr>
<tr>
<td>2.3</td>
<td>Added iCE40 RAM, PLL primitives.</td>
</tr>
<tr>
<td>2.4</td>
<td>Added PLL_DS, SB_MIPI_RX_2LANE, SB_TMDS_deserializer primitives.</td>
</tr>
<tr>
<td>2.5</td>
<td>Added SB_MAC16 Primitive details.</td>
</tr>
<tr>
<td>2.6</td>
<td>Added iCE40LM Hard Macro details. Removed PLL_DS, SB_MIPI, SB_TMDS, SB_MAC16 primitive details.</td>
</tr>
<tr>
<td>2.7</td>
<td>Added iCE5LP (iCE40 Ultra) primitive details.</td>
</tr>
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Register Primitives

SB_DFF
D Flip-Flop

Data: D is loaded into the flip-flop during a rising clock edge transition.

<table>
<thead>
<tr>
<th>Inputs</th>
<th>Output</th>
</tr>
</thead>
<tbody>
<tr>
<td>D</td>
<td>C</td>
</tr>
<tr>
<td>0</td>
<td></td>
</tr>
<tr>
<td>1</td>
<td></td>
</tr>
</tbody>
</table>

Power on State

X   X   0

Key

- Rising Edge
- 1 High logic level
- 0 Low logic level
- X Don't care
- ? Unknown

HDL use

This register is inferred during synthesis and can also be explicitly instantiated.

Verilog Instantiation

// SB_DFF - D Flip-Flop.
SB_DFF SB_DFF_inst (  
  .Q(Q),       // Registered Output
  .C(C),       // Clock
  .D(D),       // Data
);

// End of SB_DFF instantiation
VHDL Instantiation

-- SB_DFF - D Flip-Flop.

SB_DFF_inst: SB_DFF
  port map (
    Q => Q, -- Registered Output
    C => C, -- Clock
    D => D, -- Data
  );

-- End of SB_DFF instantiation
**SB_DFFE**
D Flip-Flop with Clock Enable

Data D is loaded into the flip-flop when Clock Enable E is high, during a rising clock edge transition.

<table>
<thead>
<tr>
<th>Inputs</th>
<th>Output</th>
</tr>
</thead>
<tbody>
<tr>
<td>E</td>
<td>D</td>
</tr>
<tr>
<td>0</td>
<td>X</td>
</tr>
<tr>
<td>1</td>
<td>0</td>
</tr>
<tr>
<td>1</td>
<td>1</td>
</tr>
<tr>
<td>Power on State</td>
<td>X</td>
</tr>
</tbody>
</table>

**Key**
- ⬤ Rising Edge
- 1 High logic level
- 0 Low logic level
- X Don’t care
- ? Unknown

**HDL Usage**
This register is inferred during synthesis and can also be explicitly instantiated.

**Default Signal Values**
The iCEcube2 software assigns the following signal values to unconnected input ports:

- Input D: Logic ‘0’
- Input C: Logic ‘0’
- Input E: Logic ‘1’

Note that explicitly connecting a logic ‘1’ value to port E will result in a non-optimal implementation, since an extra LUT will be used to generate the logic ‘1’. It is recommended that the user leave the port E unconnected, or use the corresponding flip-flop without Enable functionality i.e. the DFF primitive.

**Verilog Instantiation**

```verilog
// SB_DFFE - D Flip-Flop with Clock Enable.
`SB_DFFE  SB_DFFE_inst (  
  .Q(Q),     // Registered Output
  .C(C),     // Clock
  .D(D),     // Data
  .E(E),     // Clock Enable
);
```
VHDL Instantiation

-- SB_DFFE - D Flip-Flop with Clock Enable.

SB_DFFE_inst: SB_DFFE
  port map (
    Q => Q, -- Registered Output
    C => C, -- Clock
    D => D, -- Data
    E => E, -- Clock Enable
  );

-- End of SB_DFFE instantiation
**SB_DFFSR**

D Flip-Flop with Synchronous Reset

Data: D is loaded into the flip-flop when Reset R is low during a rising clock edge transition.

Reset: R input is active high, overrides all other inputs and resets the Q output during a rising clock edge.

<table>
<thead>
<tr>
<th>Inputs</th>
<th>Output</th>
</tr>
</thead>
<tbody>
<tr>
<td>R</td>
<td>D</td>
</tr>
<tr>
<td>1</td>
<td>X</td>
</tr>
<tr>
<td>X</td>
<td>X</td>
</tr>
<tr>
<td>0</td>
<td>0</td>
</tr>
<tr>
<td>0</td>
<td>1</td>
</tr>
<tr>
<td>Power on State</td>
<td>X</td>
</tr>
</tbody>
</table>

Key

- ⬆ Rising Edge
- 1 High logic level
- 0 Low logic level
- X Don't care
- ? Unknown

HDL Usage

This register is inferred during synthesis and can also be explicitly instantiated.

Default Signal Values

The iCECube2 software assigns the following signal values to unconnected input ports:

Input D: Logic ‘0’
Input C: Logic ‘0’
Input R: Logic ‘0’

Verilog Instantiation

```verilog
// SB_DFFSR - D Flip-Flop, Reset is synchronous with the rising clock edge
SB_DFFSR SB_DFFSR_inst (  
  .Q(Q), // Registered Output  
  .C(C), // Clock  
  .D(D), // Data  
  .R(R)  // Synchronous Reset
);
```

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VHDL Instantiation

-- SB_DFFSR - D Flip-Flop, Reset is synchronous with the rising clock edge

SB_DFFSR_inst : SB_DFFSR
    port map (  
        Q => Q,       -- Registered Output  
        C => C,       -- Clock  
        D => D,       -- Data  
        R => R       -- Synchronous Reset  
    );

-- End of SB_DFFSR instantiation
**SB_DFFR**

D Flip-Flop with Asynchronous Reset

Data: D is loaded into the flip-flop when R is low during a rising clock edge transition.

Reset: R input is active high, overrides all other inputs and asynchronously resets the Q output.

<table>
<thead>
<tr>
<th>Inputs</th>
<th>Output</th>
</tr>
</thead>
<tbody>
<tr>
<td>R</td>
<td>D</td>
</tr>
<tr>
<td>1</td>
<td>X</td>
</tr>
<tr>
<td>0</td>
<td>0</td>
</tr>
<tr>
<td>0</td>
<td>1</td>
</tr>
<tr>
<td>Power on State</td>
<td>X</td>
</tr>
</tbody>
</table>

Key

- Rising Edge
- 1 High logic level
- 0 Low logic level
- X Don’t care
- ? Unknown

**HDL Usage**

This register is inferred during synthesis and can also be explicitly instantiated.

**Default Signal Values**

The iCEcube2 software assigns the following signal values to unconnected input ports:

- Input D: Logic ‘0’
- Input C: Logic ‘0’
- Input R: Logic ‘0’

**Verilog Instantiation**

```verilog
// SB_DFFR - D Flip-Flop, Reset is asynchronous to the clock.
SB_DFFR   SB_DFFR_inst (  
   .Q(Q),  // Registered Output
   .C(C),  // Clock
   .D(D),  // Data
   .R(R)   // Asynchronous Reset
);```
// End of SB_DFFR instantiation

VHDL Instantiation

-- SB_DFFR - D Flip-Flop, Reset is asynchronous to the clock.

SB_DFFR_inst: SB_DFFR
  port map (  
    Q => Q,        -- Registered Output  
    C => C,        -- Clock          
    D => D,        -- Data          
    R => R         -- Asynchronous Reset  
  );

-- End of SB_DFFR instantiation
**SB_DFFSS**

D Flip-Flop with Synchronous Set

Data: D is loaded into the flip-flop when the Synchronous Set S is low during a rising clock edge transition.

Set: S input is active high, overrides all other inputs and synchronously sets the Q output.

### Inputs

<table>
<thead>
<tr>
<th>Inputs</th>
<th>Output</th>
</tr>
</thead>
<tbody>
<tr>
<td>S</td>
<td>D</td>
</tr>
<tr>
<td>1</td>
<td>X</td>
</tr>
<tr>
<td>0</td>
<td>0</td>
</tr>
<tr>
<td>0</td>
<td>1</td>
</tr>
<tr>
<td>Power on State</td>
<td>X</td>
</tr>
</tbody>
</table>

**Key**

- Rising Edge
- X Don't care
- ? Unknown

### HDL Usage

This register is inferred during synthesis and can also be explicitly instantiated.

### Default Signal Values

The iCEcube2 software assigns the following signal values to unconnected input ports:

- Input D: Logic ‘0’
- Input C: Logic ‘0’
- Input S: Logic ‘0’

### Verilog Instantiation

```verilog
// SB_DFFSS - D Flip-Flop, Set is synchronous with the rising clock edge,
SB_DFFSS SB_DFFSS_inst (  
  .Q(Q), // Registered Output
  .C(C), // Clock
  .D(D), // Data
  .S(S), // Synchronous Set
);
```

// End of SB_DFFSS instantiation
VHDL Instantiation

-- SB_DFFSS - D Flip-Flop, Set is synchronous with the rising clock edge

SB_DFFSS_inst  SB_DFFSS
           port map ( 
            Q => Q, -- Registered Output
            C => C, -- Clock
            D => D, -- Data
            S => S, -- Synchronous Set
        );

-- End of SB_DFFSS instantiation
**SB_DFFS**
D Flip-Flop with Asynchronous Set

Data: D is loaded into the flip-flop when S is low during a rising clock edge transition.

Set: S input is active high, and it overrides all other inputs and asynchronously sets the Q output.

<table>
<thead>
<tr>
<th>Inputs</th>
<th>Output</th>
</tr>
</thead>
<tbody>
<tr>
<td>S</td>
<td>D</td>
</tr>
<tr>
<td>1</td>
<td>X</td>
</tr>
<tr>
<td>0</td>
<td>0</td>
</tr>
<tr>
<td>Power on State</td>
<td>X</td>
</tr>
</tbody>
</table>

**HDL Usage**
This register is inferred during synthesis and can also be explicitly instantiated.

**Default Signal Values**
The iCEcube2 software assigns the following signal values to unconnected input ports:

Input D: Logic ‘0’
Input C: Logic ‘0’
Input S: Logic ‘0’

**Verilog Instantiation**

```verilog
// SB_DFFS - D Flip-Flop, Set is asynchronous to the rising clock edge
SB_DFFS   SB_DFFS_inst (   // Registered Output
   .Q(Q),                      // Clock
   .C(C),                      // Data
   .D(D),                      // Asynchronous Set
   .S(S)                       // End of SB_DFFS instantiation
);
```
VHDL Instantiation

-- SB_DFFS - D Flip-Flop, Set is asynchronous to the rising clock edge

SB_DFFS_inst: SB_DFFS
  port map (  
    Q => Q,    -- Registered Output  
    C => C,    -- Clock  
    D => D,    -- Data  
    S => S     -- Asynchronous Set  
  );

-- End of SB_DFFS instantiation
**SB_DFFESR**

D Flip-Flop with Clock Enable and Synchronous Reset

Data: D is loaded into the flip-flop when Reset R is low and Clock Enable E is high during a rising clock edge transition.

Reset: R, when asserted with Clock Enable E high, synchronously resets the Q output during a rising clock edge.

<table>
<thead>
<tr>
<th>Inputs</th>
<th>Output</th>
</tr>
</thead>
<tbody>
<tr>
<td>R</td>
<td>E</td>
</tr>
<tr>
<td>1</td>
<td>1</td>
</tr>
<tr>
<td>X</td>
<td>0</td>
</tr>
<tr>
<td>0</td>
<td>1</td>
</tr>
<tr>
<td>0</td>
<td>1</td>
</tr>
<tr>
<td>Power on State</td>
<td>X</td>
</tr>
</tbody>
</table>

**Key**

- Rising Edge
- 1 High logic level
- 0 Low logic level
- X Don’t care
- ? Unknown

**HDL Usage**

This register is inferred during synthesis and can also be explicitly instantiated.

**Default Signal Values**

The iCEcube2 software assigns the following signal values to unconnected input ports:

- Input D: Logic ‘0’
- Input C: Logic ‘0’
- Input R: Logic ‘0’
- Input E: Logic ‘1’

Note that explicitly connecting a Logic ‘1’ value to port E will result in a non-optimal implementation, since an extra LUT will be used to generate the Logic ‘1’. If the user’s intention is to keep the FF always enabled, it is recommended that either port E be left unconnected, or the corresponding FF without a Clock Enable port be used.
Verilog Instantiation

// SB_DFFESR - D Flip-Flop, Reset is synchronous with rising clock edge
// Clock Enable.

SB_DFFESR_SB_DFFESR_inst (  
  .Q(Q), // Registered Output  
  .C(C), // Clock  
  .E(E), // Clock Enable  
  .D(D), // Data  
  .R(R) // Synchronous Reset
);

// End of SB_DFFESR instantiation

VHDL Instantiation

-- SB_DFFESR - D Flip-Flop, Reset is synchronous with rising clock edge
-- Clock Enable.

SB_DFFESR_inst: SB_DFFESR
  port map (  
    Q => Q, -- Registered Output  
    C => C, -- Clock  
    E => E, -- Clock Enable  
    D => D, -- Data  
    R => R -- Synchronous Reset
  );

-- End of SB_DFFESR instantiation
**SB_DFFER**

**D Flip-Flop with Clock Enable and Asynchronous Reset**

Data: D is loaded into the flip-flop when Reset R is low and Clock Enable E is high during a rising clock edge transition.

Reset: R input is active high, overrides all other inputs and asynchronously resets the Q output.

![D Flip-Flop with Clock Enable and Asynchronous Reset](image)

<table>
<thead>
<tr>
<th>Inputs</th>
<th>Output</th>
</tr>
</thead>
<tbody>
<tr>
<td>R</td>
<td>E</td>
</tr>
<tr>
<td>1</td>
<td>X</td>
</tr>
<tr>
<td>0</td>
<td>0</td>
</tr>
<tr>
<td>0</td>
<td>1</td>
</tr>
<tr>
<td>0</td>
<td>1</td>
</tr>
<tr>
<td>Power on State</td>
<td>X</td>
</tr>
</tbody>
</table>

**Key**

- Rising Edge
- 1 High logic level
- 0 Low logic level
- X Don’t care
- ? Unknown

**HDL Usage**

This register is inferred during synthesis and can also be explicitly instantiated.

**Default Signal Values**

The iCEcube2 software assigns the following signal values to unconnected input ports:

- Input D: Logic ‘0’
- Input C: Logic ‘0’
- Input R: Logic ‘0’
- Input E: Logic ‘1’

Note that explicitly connecting a Logic ‘1’ value to port E will result in a non-optimal implementation, since an extra LUT will be used to generate the Logic ‘1’. If the user’s intention is to keep the FF always enabled, it is recommended that either port E be left unconnected, or the corresponding FF primitive without a Clock Enable port be used.
Verilog Instantiation

// SB_DFFER - D Flip-Flop, Reset is asynchronously on rising clock edge with Clock Enable.

SB_DFFER SB_DFFER_inst (
    .Q(Q), // Registered Output
    .C(C), // Clock
    .E(E), // Clock Enable
    .D(D), // Data
    .R(R) // Asynchronously Reset
);

// End of SB_DFFER instantiation

VHDL Instantiation

-- SB_DFFER - D Flip-Flop, Reset is asynchronously on rising clock edge with Clock Enable.

SB_DFFER_inst : SB_DFFER
    port map (    
        Q => Q, -- Registered Output
        C => C, -- Clock
        E => E, -- Clock Enable
        D => D, -- Data
        R => R -- Asynchronously Reset
    )

-- End of SB_DFFER instantiation
**SB_DFFESS**

D Flip-Flop with Clock Enable and Synchronous Set

Data: D is loaded into the flip-flop when S is low and E is high during a rising clock edge transition.

Set: Asserting S when Clock Enable E is high, synchronously sets the Q output.

![Diagram of SB_DFFESS](image)

<table>
<thead>
<tr>
<th>Inputs</th>
<th>Output</th>
</tr>
</thead>
<tbody>
<tr>
<td>S</td>
<td>E</td>
</tr>
<tr>
<td>1</td>
<td>1</td>
</tr>
<tr>
<td>0</td>
<td>0</td>
</tr>
<tr>
<td>0</td>
<td>1</td>
</tr>
<tr>
<td>0</td>
<td>1</td>
</tr>
<tr>
<td>Power on State</td>
<td>X</td>
</tr>
</tbody>
</table>

**HDL Usage**

This register is inferred during synthesis and can also be explicitly instantiated.

**Default Signal Values**

The iCEcube2 software assigns the following signal values to unconnected input ports:

- Input D: Logic '0'
- Input C: Logic '0'
- Input R: Logic '0'
- Input S: Logic '0'

**Verilog Instantiation**

// SB_DFFESS - D Flip-Flop, Set is synchronous with rising clock edge and Clock Enable.

```verilog
SB_DFFESS  SB_DFFESS_inst (  
    .Q(Q), // Registered Output  
    .C(C), // Clock  
    .E(E), // Clock Enable  
    .D(D), // Data  
    .S(S)  // Synchronously Set
);
```
VHDL Instantiation

-- SB_DFFESS - D Flip-Flop, Set is synchronous with rising clock edge and Clock Enable.

SB_DFFESS_inst : SB_DFFESS
  port map (  
    Q => Q, -- Registered Output
    C => C, -- Clock
    E => E, -- Clock Enable
    D => D, -- Data
    S => S -- Synchronously Set
  );

-- End of SB_DFFESS instantiation
**SB_DFFES**

D Flip-Flop with Clock Enable and Asynchronous Set

Data: D is loaded into the flip-flop when S is low and E is high during a rising clock edge transition.

Set: S input is active high, overrides all other inputs and asynchronously sets the Q output.

![SB_DFFES Diagram]

<table>
<thead>
<tr>
<th>Inputs</th>
<th>Output</th>
</tr>
</thead>
<tbody>
<tr>
<td>S</td>
<td>E</td>
</tr>
<tr>
<td>1</td>
<td>X</td>
</tr>
<tr>
<td>0</td>
<td>0</td>
</tr>
<tr>
<td>0</td>
<td>1</td>
</tr>
<tr>
<td>0</td>
<td>1</td>
</tr>
<tr>
<td>Power on State</td>
<td>X</td>
</tr>
</tbody>
</table>

**Key**

- Rising Edge
  - 1 High logic level
  - 0 Low logic level
  - X Don’t care
  - ? Unknown

**HDL Usage**

This register is inferred during synthesis and can also be explicitly instantiated.

**Default Signal Values**

The iCEcube2 software assigns the following signal values to unconnected input ports:

- Input D: Logic ‘0’
- Input C: Logic ‘0’
- Input S: Logic ‘0’
- Input E: Logic ‘1’

**Verilog Instantiation**

// SB_DFFES - D Flip-Flop, Set is asynchronous on rising clock edge with Clock Enable.

```verilog
SB_DFFES   SB_DFFES_inst (   .Q(Q),   // Registered Output   .C(C),   // Clock   .E(E),   // Clock Enable   .D(D),   // Data   .S(S)    // Asynchronously Set   );
```
VHDL Instantiation

-- SB_DFFES - D Flip-Flop, Set is asynchronous on rising clock edge with Clock Enable.

SB_DFFES_inst : SB_DFFES
  port map (  
    Q => Q,                      -- Registered Output  
    C => C,                      -- Clock  
    E => E,                      -- Clock Enable  
    D => D,                      -- Data  
    S => S                       -- Asynchronously Set  
  );

-- End of SB_DFFES instantiation
**SB_DFFN**

D Flip-Flop – Negative Edge Clock

Data: D is loaded into the flip-flop during the falling clock edge transition.

![SB_DFFN diagram](image)

<table>
<thead>
<tr>
<th>Inputs</th>
<th>Output</th>
</tr>
</thead>
<tbody>
<tr>
<td>D</td>
<td>C</td>
</tr>
<tr>
<td>0</td>
<td></td>
</tr>
<tr>
<td>1</td>
<td></td>
</tr>
</tbody>
</table>

**Power on State**

<table>
<thead>
<tr>
<th>Key</th>
<th>Value</th>
</tr>
</thead>
<tbody>
<tr>
<td>Falling Edge</td>
<td></td>
</tr>
<tr>
<td>1</td>
<td>High logic level</td>
</tr>
<tr>
<td>0</td>
<td>Low logic level</td>
</tr>
<tr>
<td>X</td>
<td>Don’t care</td>
</tr>
<tr>
<td>?</td>
<td>Unknown</td>
</tr>
</tbody>
</table>

**HDL Usage**

This register is inferred during synthesis and can also be explicitly instantiated.

**Default Signal Values**

The iCEcube2 software assigns the following signal values to unconnected input ports:

Input D: Logic ‘0’
Input C: Logic ‘0’

**Verilog Instantiation**

```verilog
// SB_DFFN - D Flip-Flop – Negative Edge Clock.
SB_DFFN SB_DFFN_inst (
    .Q(Q),  // Registered Output
    .C(C),  // Clock
    .D(D),  // Data
);
// End of SB_DFFN instantiation
```
VHDL Instantiation

-- SB_DFFN - D Flip-Flop – Negative Edge Clock.

SB_DFFN_inst : SB_DFFN
  port map (  
    Q => Q,       -- Registered Output  
    C => C,       -- Clock  
    D => D,       -- Data  
  );

-- End of SB_DFFN instantiation
**SB_DFFNE**

D Flip-Flop – Negative Edge Clock and Clock Enable

Data: D is loaded into the flip-flop when E is high, during the falling clock edge transition.

<table>
<thead>
<tr>
<th>Inputs</th>
<th>Output</th>
</tr>
</thead>
<tbody>
<tr>
<td>E</td>
<td>D</td>
</tr>
<tr>
<td>0</td>
<td>X</td>
</tr>
<tr>
<td>1</td>
<td>0</td>
</tr>
<tr>
<td>1</td>
<td>1</td>
</tr>
</tbody>
</table>

Power on State: X | X | 0

Key
- Falling Edge
- 1: High logic level
- 0: Low logic level
- X: Don't care
- ?: Unknown

**HDL Usage**

This register is inferred during synthesis and can also be explicitly instantiated.

**Default Signal Values**

The iCEcube2 software assigns the following signal values to unconnected input ports:

Input D: Logic ‘0’
Input C: Logic ‘0’
Input E: Logic ‘1’

Note that explicitly connecting a Logic ‘1’ value to port E will result in a non-optimal implementation, since an extra LUT will be used to generate the Logic ‘1’. If the user’s intention is to keep the FF always enabled, it is recommended that either port E be left unconnected, or the corresponding FF without a Clock Enable port be used.

**Verilog Instantiation**

```verilog
// SB_DFFNE - D Flip-Flop – Negative Edge Clock and Clock Enable.

SB_DFFNE  SB_DFFNE_inst (  
    .Q(Q),         // Registered Output  
    .C(C),         // Clock  
    .D(D),         // Data  
```

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VHDL Instantiation

-- SB_DFFNE - D Flip-Flop – Negative Edge Clock and Clock Enable.

SB_DFFNE_inst : SB_DFFNE
  port map (
    Q => Q,         -- Registered Output
    C => C,        -- Clock
    D => D,        -- Data
    E => E,        -- Clock Enable
  );

-- End of SB_DFFNE instantiation
**SB_DFFNSR**

D Flip-Flop – Negative Edge Clock with Synchronous Reset

Data: D is loaded into the flip-flop when R is low during the falling clock edge transition.

Reset: R input is active high, overrides all other inputs and resets the Q output during the falling clock edge transition.

<table>
<thead>
<tr>
<th>Inputs</th>
<th>Output</th>
</tr>
</thead>
<tbody>
<tr>
<td>R</td>
<td>D</td>
</tr>
<tr>
<td>1</td>
<td>X</td>
</tr>
<tr>
<td>X</td>
<td>X</td>
</tr>
<tr>
<td>0</td>
<td>0</td>
</tr>
<tr>
<td>0</td>
<td>1</td>
</tr>
<tr>
<td>Power on State</td>
<td>X</td>
</tr>
</tbody>
</table>

**Key**

- Falling Edge
- 1: High logic level
- 0: Low logic level
- X: Don’t care
- ?: Unknown

**HDL Usage**

This register is inferred during synthesis and can also be explicitly instantiated.

**Default Signal Values**

The iCEcube2 software assigns the following signal values to unconnected input ports:

- Input D: Logic ‘0’
- Input C: Logic ‘0’
- Input R: Logic ‘0’

**Verilog Instantiation**

// SB_DFFNSR - D Flip-Flop – Negative Edge Clock, Reset is synchronous with the falling clock edge

```verilog
SB_DFFNSR   SB_DFFNSR_inst (    .Q(Q),    // Registered Output    .C(C),    // Clock    .D(D),    // Data    .R(R)    // Synchronous Reset );
```
// End of SB_DFFNSR instantiation

VHDL Instantiation

-- SB_DFFNSR - D Flip-Flop – Negative Edge Clock, Reset is synchronous with the falling clock edge

SB_DFFNSR_inst: SB_DFFNSR
    port map (  
        Q => Q,               -- Registered Output  
        C => C,               -- Clock  
        D => D,               -- Data  
        R => R                -- Synchronous Reset  
    );

-- End of SB_DFFNSR instantiation
**SB_DFFNR**

D Flip-Flop – Negative Edge Clock with Asynchronous Reset

Data: D is loaded into the flip-flop when R is low during the falling clock edge transition.

Reset: R input is active high, overrides all other inputs and asynchronously resets the Q output.

![SB_DFFNR Diagram]

<table>
<thead>
<tr>
<th>Inputs</th>
<th>Output</th>
</tr>
</thead>
<tbody>
<tr>
<td>R</td>
<td>D</td>
</tr>
<tr>
<td>1</td>
<td>X</td>
</tr>
<tr>
<td>0</td>
<td>0</td>
</tr>
<tr>
<td>0</td>
<td>1</td>
</tr>
<tr>
<td>Power on State</td>
<td>X</td>
</tr>
</tbody>
</table>

**HDL Usage**

This register is inferred during synthesis and can also be explicitly instantiated.

**Default Signal Values**

The iCEcube2 software assigns the following signal values to unconnected input ports:

Input D: Logic '0'
Input C: Logic '0'
Input R: Logic '0'

**Verilog Instantiation**

// SB_DFFNR - D Flip-Flop – Negative Edge Clock, Reset is asynchronous to the clock.

```
SB_DFFNR SB_DFFNR_inst (  
    .Q(Q),    // Registered Output  
    .C(C),    // Clock  
    .D(D),    // Data  
    .R(R)     // Asynchronously Reset  
);  
```

// End of SB_DFFNR instantiation
VHDL Instantiation

-- SB_DFFNR - D Flip-Flop – Negative Edge Clock, Reset is asynchronous to the clock.

SB_DFFNR_inst : SB_DFFNR
port map (  
  Q => Q,          -- Registered Output  
  C => C,          -- Clock  
  D => D,          -- Data  
  R => R           -- Asynchronously Reset  
);

-- End of SB_DFFNR instantiation
**SB_DFFNSS**

D Flip-Flop – Negative Edge Clock with Synchronous Set

Data: D is loaded into the flip-flop when S is low during the falling clock edge transition.

Set: S input is active high, overrides all other inputs and synchronously sets the Q output.

![SB_DFFNSS symbol](image)

<table>
<thead>
<tr>
<th>Inputs</th>
<th>Output</th>
</tr>
</thead>
<tbody>
<tr>
<td>S</td>
<td>D</td>
</tr>
<tr>
<td>1</td>
<td>X</td>
</tr>
<tr>
<td>0</td>
<td>0</td>
</tr>
<tr>
<td>0</td>
<td>1</td>
</tr>
<tr>
<td>Power on State</td>
<td>X</td>
</tr>
</tbody>
</table>

**Key**
- Falling Edge
- 1 High logic level
- 0 Low logic level
- X Don’t care
- ? Unknown

**HDL Usage**
This register is inferred during synthesis and can also be explicitly instantiated.

**Default Signal Values**
The iCEcube2 software assigns the following signal values to unconnected input ports:

- Input D: Logic '0'
- Input C: Logic '0'
- Input S: Logic '0'

**Verilog Instantiation**

// SB_DFFNSS - D Flip-Flop – Negative Edge Clock, Set is synchronous with the falling clock edge,

```verilog
SB_DFFNSS SB_DFFNSS_inst (
  .Q(Q), // Registered Output
  .C(C), // Clock
  .D(D), // Data
  .S(S)  // Synchronous Set
);
```

// End of SB_DFFNSS instantiation
**VHDL Instantiation**

-- SB_DFFNSS - D Flip-Flop – Negative Edge Clock, Set is synchronous with the falling clock edge, 
-- with .

```
SB_DFFNSS_inst : SB_DFFNSS
   port map (  
    Q => Q,    -- Registered Output  
    C => C,    -- Clock  
    D => D,    -- Data  
    S => S    -- Synchronous Set  
   );
```

-- End of SB_DFFNSS instantiation
**SB_DFFNS**

D Flip-Flop – Negative Edge Clock with Asynchronous Set

Data: D is loaded into the flip-flop when S is low during the falling clock edge transition.

Set: S input is active high, overrides all other inputs and asynchronously sets the Q output.

<table>
<thead>
<tr>
<th>Inputs</th>
<th>Output</th>
</tr>
</thead>
<tbody>
<tr>
<td>S</td>
<td>D</td>
</tr>
<tr>
<td>1</td>
<td>X</td>
</tr>
<tr>
<td>0</td>
<td>0</td>
</tr>
<tr>
<td>0</td>
<td>1</td>
</tr>
<tr>
<td>Power on State</td>
<td>X</td>
</tr>
</tbody>
</table>

**HDL Usage**

This register is inferred during synthesis and can also be explicitly instantiated.

**Default Signal Values**

The iCEcube2 software assigns the following signal values to unconnected input ports:

- Input D: Logic '0'
- Input C: Logic '0'
- Input S: Logic '0'

**Verilog Instantiation**

```
// SB_DFFNS - D Flip-Flop – Negative Edge Clock, Set is asynchronous to the falling clock edge,
SB_DFFNS     SB_DFFNS_inst (  
  .Q(Q),  // Registered Output  
  .C(C),  // Clock  
  .D(D),  // Data  
  .S(S)   // Asynchronous Set  
);
// End of SB_DFFNS instantiation
```
VHDL Instantiation

-- SB_DFFNS - D Flip-Flop – Negative Edge Clock, Set is asynchronous to the falling clock edge

SB_DFFNS_inst : SB_DFFNS
  port map (  
    Q  => Q,  
    C  => C,  
    D  => D,  
    S  => S  
  );

-- End of SB_DFFNS instantiation
**SB_DFFNESR**

**D Flip-Flop – Negative Edge Clock, Enable and Synchronous Reset**

Data: D is loaded into the flip-flop when R is low and E is high during the falling clock edge transition.

Reset: Asserting R when the Clock Enable E is high, synchronously resets the Q output during the falling clock edge.

<table>
<thead>
<tr>
<th>Inputs</th>
<th>Output</th>
</tr>
</thead>
<tbody>
<tr>
<td>R</td>
<td>E</td>
</tr>
<tr>
<td>1</td>
<td>1</td>
</tr>
<tr>
<td>X</td>
<td>0</td>
</tr>
<tr>
<td>0</td>
<td>1</td>
</tr>
<tr>
<td>0</td>
<td>1</td>
</tr>
<tr>
<td>Power on State</td>
<td>X</td>
</tr>
</tbody>
</table>

**HDL Usage**

This register is inferred during synthesis and can also be explicitly instantiated.

**Default Signal Values**

The iCEcube2 software assigns the following signal values to unconnected input ports:

- Input D: Logic ‘0’
- Input C: Logic ‘0’
- Input R: Logic ‘0’
- Input E: Logic ‘1’

Note that explicitly connecting a Logic ‘1’ value to port E will result in a non-optimal implementation, since an extra LUT will be used to generate the Logic ‘1’. If the user’s intention is to keep the FF always enabled, it is recommended that either port E be left unconnected, or the corresponding FF without a Clock Enable port be used.

**Verilog Instantiation**

```verilog
// SB_DFFNESR - D Flip-Flop – Negative Edge Clock, Reset is synchronous with falling clock edge Clock Enable.
```
SB_DFFNESR   SB_DFFNESR_inst (  
   .Q(Q),       // Registered Output  
   .C(C),       // Clock  
   .E(E),       // Clock Enable  
   .D(D),       // Data  
   .R(R)        // Synchronous Reset  
);

// End of SB_DFFNESR instantiation

VHDL Instantiation

-- SB_DFFNESR - D Flip-Flop – Negative Edge Clock, Reset is synchronous with falling clock edge Clock Enable.

SB_DFFNESR_inst : SB_DFFNESR  
   port map (  
      Q => Q,     -- Registered Output  
      C => C,     -- Clock  
      E => E,     -- Clock Enable  
      D => D,     -- Data  
      R => R      -- Synchronous Reset  
);  

-- End of SB_DFFNESR instantiation
**SB_DFFNER**

**D Flip-Flop – Negative Edge Clock, Enable and Asynchronous Reset**

Data: D is loaded into the flip-flop when R is low and E is high during the falling clock edge transition.

Reset: R input is active high, and it overrides all other inputs and asynchronously resets the Q output.

<table>
<thead>
<tr>
<th>Inputs</th>
<th>Output</th>
</tr>
</thead>
<tbody>
<tr>
<td>R</td>
<td>E</td>
</tr>
<tr>
<td>1</td>
<td>X</td>
</tr>
<tr>
<td>0</td>
<td>0</td>
</tr>
<tr>
<td>0</td>
<td>1</td>
</tr>
<tr>
<td>0</td>
<td>1</td>
</tr>
<tr>
<td>Power on State</td>
<td>X</td>
</tr>
</tbody>
</table>

**Key**

- Falling Edge
- 1 High logic level
- 0 Low logic level
- X Don’t care
- ? Unknown

**HDL Usage**

This register is inferred during synthesis and can also be explicitly instantiated.

**Default Signal Values**

The iCEcube2 software assigns the following signal values to unconnected input ports:

Input D: Logic ‘0’
Input C: Logic ‘0’
Input R: Logic ‘0’
Input E: Logic ‘1’

Note that explicitly connecting a Logic ‘1’ value to port E will result in a non-optimal implementation, since an extra LUT will be used to generate the Logic ‘1’. If the user’s intention is to keep the FF always enabled, it is recommended that either port E be left unconnected, or the corresponding FF without a Clock Enable port be used.
Verilog Instantiation

// SB_DFFNER - D Flip-Flop – Negative Edge Clock, Reset is asynchronously
// on falling clock edge and Clock Enable.
SB_DFFNER   SB_DFFNER_inst(  
    .Q(Q),         // Registered Output
    .C(C),         // Clock
    .E(E),         // Clock Enable
    .D(D),         // Data
    .R(R)          // Asynchronously Reset
    );

// End of SB_DFFNER instantiation

VHDL Instantiation

-- SB_DFFNER - D Flip-Flop – Negative Edge Clock, Reset is asynchronously
-- on falling clock edge and Clock Enable.
SB_DFFNER_inst:  SB_DFFNER  
    port map (  
    Q => Q,           -- Registered Output
    C => C,           -- Clock
    E => E,           -- Clock Enable
    D => D,           -- Data
    R => R            -- Asynchronously Reset
    );

-- End of SB_DFFNER instantiation
**SB_DFFNESS**

D Flip-Flop – Negative Edge Clock, Enable and Synchronous Set

Data: D is loaded into the flip-flop when S is low and E is high during the falling clock edge transition.

Set: S and E inputs high, synchronously sets the Q output on the falling clock edge transition.

<table>
<thead>
<tr>
<th>Inputs</th>
<th>Output</th>
</tr>
</thead>
<tbody>
<tr>
<td>S</td>
<td>E</td>
</tr>
<tr>
<td>1</td>
<td>1</td>
</tr>
<tr>
<td>X</td>
<td>0</td>
</tr>
<tr>
<td>0</td>
<td>1</td>
</tr>
<tr>
<td>0</td>
<td>1</td>
</tr>
<tr>
<td>Power on State</td>
<td>X</td>
</tr>
</tbody>
</table>

**Key**
- Falling Edge
  - 1 High logic level
  - 0 Low logic level
  - X Don't care
  - ? Unknown

**HDL Usage**
This register is inferred during synthesis and can also be explicitly instantiated.

**Default Signal Values**
The iCEcube2 software assigns the following signal values to unconnected input ports:

- Input D: Logic ‘0’
- Input C: Logic ‘0’
- Input S: Logic ‘0’
- Input E: Logic ‘1’

Note that explicitly connecting a Logic ‘1’ value to port E will result in a non-optimal implementation, since an extra LUT will be used to generate the Logic ‘1’. If the user’s intention is to keep the FF always enabled, it is recommended that either port E be left unconnected, or the corresponding FF without a Clock Enable port be used.
Verilog Instantiation

// SB_DFFNESS - D Flip-Flop – Negative Edge Clock, Set is synchronous with falling clock edge, // and Clock Enable.

SB_DFFNESS   SB_DFFNESS_inst (  
   .Q(Q),       // Registered Output  
   .C(C),       // Clock  
   .E(E),       // Clock Enable  
   .D(D),       // Data  
   .S(S)        // Synchronously Set
);

// End of SB_DFFNESS instantiation

VHDL Instantiation

-- SB_DFFNESS - D Flip-Flop – Negative Edge Clock, Set is synchronous with falling clock edge, -- and Clock Enable.

SB_DFFNESS_inst : SB_DFFNESS
   port map (  
      Q => Q,       -- Registered Output  
      C => C,       -- Clock  
      E => E,       -- Clock Enable  
      D => D,       -- Data  
      S => S        -- Synchronously Set
);

-- End of SB_DFFNESS instantiation
**SB_DFFNES**

D Flip-Flop – Negative Edge Clock, Enable and Asynchronous Set

Data: D is loaded into the flip-flop when S is low and E is high during the falling clock edge transition.

Set: S input is active high, and it overrides all other inputs and asynchronously sets the Q output.

```
<table>
<thead>
<tr>
<th>Inputs</th>
<th>Output</th>
</tr>
</thead>
<tbody>
<tr>
<td>S</td>
<td>E</td>
</tr>
<tr>
<td>1</td>
<td>X</td>
</tr>
<tr>
<td>0</td>
<td>0</td>
</tr>
<tr>
<td>0</td>
<td>1</td>
</tr>
<tr>
<td>0</td>
<td>1</td>
</tr>
<tr>
<td>Power on State</td>
<td>X</td>
</tr>
</tbody>
</table>
```

**HDL Usage**

This register is inferred during synthesis and can also be explicitly instantiated.

**Default Signal Values**

The iCEcube2 software assigns the following signal values to unconnected input ports:

- Input D: Logic ‘0’
- Input C: Logic ‘0’
- Input S: Logic ‘0’
- Input E: Logic ‘1’

Note that explicitly connecting a Logic ‘1’ value to port E will result in a non-optimal implementation, since an extra LUT will be used to generate the Logic ‘1’. If the user’s intention is to keep the FF always enabled, it is recommended that either port E be left unconnected, or the corresponding FF without a Clock Enable port be used.
Verilog Instantiation

// SB_DFFNES - D Flip-Flop – Negative Edge Clock, Set is asynchronous on falling clock edge with clock Enable.

SB_DFFNES SB_DFFNES_inst (  
  .Q(Q), // Registered Output  
  .C(C), // Clock  
  .E(E), // Clock Enable  
  .D(D), // Data  
  .S(S) // Asynchronously Set  
);

// End of SB_DFFNES instantiation

VHDL Instantiation

-- SB_DFFNES - D Flip-Flop – Negative Edge Clock, Set is asynchronous on falling clock edge and Clock Enable.

SB_DFFNES_inst: SB_DFFNES  
  port map (  
    Q => Q, -- Registered Output  
    C => C, -- Clock  
    E => E, -- Clock Enable  
    D => D, -- Data  
    S => S -- Asynchronously Set  
);

-- End of SB_DFFNES instantiation
Combinational Logic Primitives

**SB_LUT4**

The LUT unit is a simple ROM 4 input look-up function table.

```
  I0  I1  I2  I3  O
  0   0   0   0  LUT_INIT[0]
  0   0   0   1  LUT_INIT[1]
  0   0   1   0  LUT_INIT[2]
  0   0   1   1  LUT_INIT[3]
  0   1   0   0  LUT_INIT[4]
  0   1   0   1  LUT_INIT[5]
  0   1   1   0  LUT_INIT[6]
  0   1   1   1  LUT_INIT[7]
  1   0   0   0  LUT_INIT[8]
  1   0   0   1  LUT_INIT[9]
  1   0   1   0  LUT_INIT[10]
  1   0   1   1  LUT_INIT[11]
  1   1   0   0  LUT_INIT[12]
  1   1   0   1  LUT_INIT[13]
  1   1   1   0  LUT_INIT[14]
  1   1   1   1  LUT_INIT[15]
```

**Initialization values**

LUT state initialization parameter LUT_INIT = 16'hxxxx;

**HDL Usage**

This primitive is inferred during synthesis and can also be explicitly instantiated.

**Default Signal Values**

The iCEcube2 software assigns logic value ‘0’ to unconnected input ports.
Verilog Instantiation

// SB_LUT4 : 4-input Look-Up Table
SB_LUT4    SB_LUT4_inst (  
    .O (O),                // output  
    .I0 (I0),              // data input 0  
    .I1 (I1),              // data input 1  
    .I2 (I2),              // data input 2  
    .I3 (I3)               // data input 3  
  );
defparam SB_LUT4_inst.LUT_INIT=16'hxxxx;
  //LUT state initialization parameter, 16 bits.
//End of SB_LUT4 instantiation

VHDL Instantiation

-- SB_LUT4 : 4-input Look-Up Table
SB_LUT4_inst: SB_LUT4
  generic map(    
    LUT_INIT => X"0001"    -- LUT state initialization parameter, 16 bits
  )
  port map (    
    I0 => I0,    
    I1 => I1,    
    I2 => I2,    
    I3 => I3,    
    O => 0  
  );
**SB_CARRY**

**Carry Logic**

The dedicated Carry Logic within each Logic Cell primarily accelerates and improves the efficiency of arithmetic logic such as adders, accumulators, subtracters, incrementers, decrementers, counters, ALUs, and comparators. The Carry Logic also supports a limited number of wide combinational logic functions.

The figure below illustrates the Carry Logic structure within a Logic Cell. The Carry Logic shares inputs with the associated Look-Up Table (LUT). The I1 and I2 inputs of the LUT directly feed the Carry Logic. The carry input from the previous adjacent Logic Cell optionally provides an alternate input to the LUT4 function, supplanting the I3 input.

**Carry Logic Structure within a Logic Cell**

![Carry Logic Structure](image)

<table>
<thead>
<tr>
<th>Inputs</th>
<th>Output</th>
</tr>
</thead>
<tbody>
<tr>
<td>I0</td>
<td>I1</td>
</tr>
<tr>
<td>0</td>
<td>0</td>
</tr>
<tr>
<td>0</td>
<td>X</td>
</tr>
<tr>
<td>X</td>
<td>1</td>
</tr>
<tr>
<td>X</td>
<td>0</td>
</tr>
<tr>
<td>1</td>
<td>X</td>
</tr>
<tr>
<td>1</td>
<td>1</td>
</tr>
</tbody>
</table>

**HDL Usage**

This primitive is inferred during synthesis and can also be explicitly instantiated.

**Default Signal Values**

The iCEcube2 software assigns logic value ‘0’ to unconnected input ports.
Verilog Instantiation

SB_CARRY my_carry_inst (  
  .CO(CO),  
  .I0(I0),  
  .I1(I1),  
  .CI(CI));

VHDL Instantiation

my_carry_inst : SB_CARRY  
  port map (  
    CO => CO,  
    CI => CI,  
    I0 => I0,  
    I1 => I1  
  );
Block RAM Primitives

The iCE architecture supports dual ported synchronous RAM, with 4096 bits, and a fixed 16 bit data-width. The block is arranged as 256 x 16 bit words. The RAM block may be configured to be used as a RAM with data between 1-16 bits.

**iCE65 Block RAM**

Each iCE65 device includes multiple high-speed synchronous RAM blocks (RAM4K), each 4Kbit in size. A RAM4K block has separate write and read ports, each with independent control signals. Additionally, the write port has an Active-Low bit-line write-enable control; each write-port data bit has an individual write-enable control. By default, input and output data is 16 bits wide, although the data width is configurable using programmable logic and, if needed, multiple RAM4K blocks. The data contents of the RAM4K block are optionally pre-loaded during ICE device configuration.

**RAM4K Naming Convention Rules**

The SiliconBlue Technologies convention for the RAM4K primitives with negedge Read or Write clock is that the base primitive name is post fixed with N and R or W according to the clock that is affected, as displayed in the table below.

<table>
<thead>
<tr>
<th>RAM Primitive Name</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>SB_RAM4K</td>
<td>Posedge Read clock, Posedge Write clock</td>
</tr>
<tr>
<td>SB_RAM4KNR</td>
<td>Negedge Read clock, Posedge Write clock</td>
</tr>
<tr>
<td>SB_RAM4KNW</td>
<td>Posedge Read clock, Negedge Write clock</td>
</tr>
<tr>
<td>SB_RAM4KNRNW</td>
<td>Negedge Read clock, Negedge Write clock</td>
</tr>
</tbody>
</table>

RAM4K blocks have separate write and read ports, each with independent control signals.

The data contents of the RAM4K block are optionally pre-loaded during ICE device configuration. If the RAM4K blocks are not pre-loaded during configuration, then the resulting configuration bitstream image is smaller.
If an unitialized RAM4K block is used in the application, then the application must initialize the RAM contents to guarantee the data value.

The following table lists the signals for both ports. Additionally, the write port has an active-Low bit-line write-enable control:

<table>
<thead>
<tr>
<th>Signal Name</th>
<th>Direction</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>WDATA[15:0]</td>
<td>Input</td>
<td>Write Data input</td>
</tr>
<tr>
<td>MASK[15:0]</td>
<td>Input</td>
<td>Bit-line Write Enable input, active low</td>
</tr>
<tr>
<td>WADDR[7:0]</td>
<td>Input</td>
<td>Write Address input. Selects up to 256 possible locations</td>
</tr>
<tr>
<td>WE</td>
<td>Input</td>
<td>Write Enable input, active high</td>
</tr>
<tr>
<td>WCLK</td>
<td>Input</td>
<td>Write Clock input, rising-edge active</td>
</tr>
<tr>
<td>WCLKE</td>
<td>Input</td>
<td>Write Clock Enable input</td>
</tr>
<tr>
<td>RDATA[15:0]</td>
<td>Output</td>
<td>Read Data output</td>
</tr>
<tr>
<td>RADDR[7:0]</td>
<td>Input</td>
<td>Read Address input. Selects one of 256 possible locations</td>
</tr>
<tr>
<td>RE</td>
<td>Input</td>
<td>Read Enable input, active high</td>
</tr>
<tr>
<td>RCLK</td>
<td>Input</td>
<td>Read Clock input, rising-edge active</td>
</tr>
<tr>
<td>RCLKE</td>
<td>Input</td>
<td>Read Clock Enable input</td>
</tr>
<tr>
<td>INIT_0, … ,INIT_F</td>
<td>Verilog parameter</td>
<td>RAM Initialization Data. Passed using 16 parameter strings, each comprising 256 bits. (16x256=4096 total bits)</td>
</tr>
</tbody>
</table>
Write Operation

1. Supply a valid address on the WADDR[7:0] address input port

2. Supply valid data on the WDATA[15:0] data input port

To write or mask selected data bits, set the associated bit write MASK accordingly. For example, write operations on data bit Data[i] is controlled by the associated MASK[i] input: MASK[i] = 0: Enable write operations for data line Data[i]

- MASK[i] = 1: Mask write operations for data line Data[i]
- Enable the RAM4K write port (WE = 1)

3. Apply a rising clock edge on WCLK

<table>
<thead>
<tr>
<th>Operation</th>
<th>WDATA[15:0] Data</th>
<th>MASK[15:0] Bit Enable</th>
<th>WADDR[7:0] Address</th>
<th>WE Enable</th>
<th>WCLK Clock</th>
<th>RAM Location</th>
</tr>
</thead>
<tbody>
<tr>
<td>Disabled</td>
<td>X</td>
<td>X</td>
<td>X</td>
<td>X</td>
<td>0</td>
<td>No Change</td>
</tr>
<tr>
<td>Disabled</td>
<td>X</td>
<td>X</td>
<td>X</td>
<td></td>
<td></td>
<td>No Change</td>
</tr>
<tr>
<td>Write Data</td>
<td>D[i]</td>
<td>MASK[i]=0</td>
<td>WADDR</td>
<td>1</td>
<td>†</td>
<td>RAM[WADDR[i]] = D[i]</td>
</tr>
<tr>
<td>Masked Write</td>
<td>X</td>
<td>MASK[i]=1</td>
<td>WADDR</td>
<td>1</td>
<td>†</td>
<td>RAM[WADDR[i]] = No Change</td>
</tr>
</tbody>
</table>

Read Operation

The following table describes various read operations for a RAM4K block. All RAM4K read operations are synchronized to the rising edge of RCLK.

<table>
<thead>
<tr>
<th>Operation</th>
<th>RADDR[7:0] Address</th>
<th>RE Enable</th>
<th>RCLK Clock</th>
<th>RDATA[15:0]</th>
</tr>
</thead>
<tbody>
<tr>
<td>After configuration, before first valid Read Data operation</td>
<td>X</td>
<td>X</td>
<td>X</td>
<td>Undefined</td>
</tr>
<tr>
<td>Disabled</td>
<td>X</td>
<td>0</td>
<td>X</td>
<td>No Change</td>
</tr>
<tr>
<td>Read Data</td>
<td>RA</td>
<td>1</td>
<td>†</td>
<td>RAM[RADDR]</td>
</tr>
</tbody>
</table>

To read data from the RAM4K block

1. Supply a valid address on the RADDR[7:0] address input port

2. Enable the RAM4K read port (RE = 1)

3. Apply a rising clock edge on RCLK

Default Signal Values

The iCEcube2 software assigns logic value ‘0’ to all unconnected input ports, with the exception of the RCLKE and WCLKE ports.
The RCLKE and WCLKE ports are always enabled by default i.e. if left unconnected the software will automatically assign a logic value ‘1’ to these ports. Note that explicitly connecting a logic ‘1’ value to ports RCLKE and WCLKE will result in a non-optimal implementation, since an extra LUT will be used to generate the logic ‘1’. If the user’s intention is to always maintain the clocks in an enabled state, it is recommended that these ports be left unconnected.

Note that the Read Enable (RE) and Write Enable (WE) ports are always disabled by default, since they are tied-off to logic ‘0’ by the software, unless explicitly enabled by the user.

**Verilog Instantiation**

The following instantiation is for the base SB_RAM4K, all other RAM4K based primitives share the same format with the only difference being the port name changes. All primitives share the same parameter for data initialization after power on reset.

```verilog
// SB_RAM4K with data initialization after power on reset
SB_RAM4K SB_RAM4K_with_INIT (.RDATA(RDATA), .RCLK(RCLK), .RCLKE(RCLKE), .RE(RE), .RADDR(RADDR), .WCLK(WCLK), .WCLKE(WCLKE), .WE(WE), .WADDR(WADDR), .MASK(MASK), .WDATA(WDATA));
```

defparam SB_RAM4K_with_INIT.INIT_0 = 256'h0000000000000000000000000000000000000000000000000000000000000000;
defparam SB_RAM4K_with_INIT.INIT_1 = 256'h0000000000000000000000000000000000000000000000000000000000000000;
defparam SB_RAM4K_with_INIT.INIT_2 = 256'h0000000000000000000000000000000000000000000000000000000000000000;
defparam SB_RAM4K_with_INIT.INIT_3 = 256'h0000000000000000000000000000000000000000000000000000000000000000;
defparam SB_RAM4K_with_INIT.INIT_4 = 256'h0000000000000000000000000000000000000000000000000000000000000000;
defparam SB_RAM4K_with_INIT.INIT_5 = 256'h0000000000000000000000000000000000000000000000000000000000000000;
defparam SB_RAM4K_with_INIT.INIT_6 = 256'h0000000000000000000000000000000000000000000000000000000000000000;
defparam SB_RAM4K_with_INIT.INIT_7 = 256'h0000000000000000000000000000000000000000000000000000000000000000;
defparam SB_RAM4K_with_INIT.INIT_8 = 256'h0000000000000000000000000000000000000000000000000000000000000000;
defparam SB_RAM4K_with_INIT.INIT_9 = 256'h0000000000000000000000000000000000000000000000000000000000000000;
defparam SB_RAM4K_with_INIT.INIT_A = 256'h0000000000000000000000000000000000000000000000000000000000000000;
defparam SB_RAM4K_with_INIT.INIT_B = 256'h0000000000000000000000000000000000000000000000000000000000000000;
defparam SB_RAM4K_with_INIT.INIT_C = 256'h0000000000000000000000000000000000000000000000000000000000000000;
defparam SB_RAM4K_with_INIT.INIT_D = 256'h0000000000000000000000000000000000000000000000000000000000000000;
defparam SB_RAM4K_with_INIT.INIT_E = 256'h0000000000000000000000000000000000000000000000000000000000000000;
defparam SB_RAM4K_with_INIT.INIT_F = 256'h0000000000000000000000000000000000000000000000000000000000000000;
```

**VHDL Instantiation**

```vhdl
-- SB_RAM4K with data initialization after power on reset
SB_RAM4K_with_INIT : SB_RAM4K
```

ICE Technology Library  
Lattice Semiconductor Corporation Confidential
generic map (  
INIT_0 =>  x"0000000000000000000000000000000000000000000000000000000000000000",  
INIT_1 =>  x"0000000000000000000000000000000000000000000000000000000000000000",  
INIT_2 =>  x"0000000000000000000000000000000000000000000000000000000000000000",  
INIT_3 =>  x"0000000000000000000000000000000000000000000000000000000000000000",  
INIT_4 =>  x"0000000000000000000000000000000000000000000000000000000000000000",  
INIT_5 =>  x"0000000000000000000000000000000000000000000000000000000000000000",  
INIT_6 =>  x"0000000000000000000000000000000000000000000000000000000000000000",  
INIT_7 =>  x"0000000000000000000000000000000000000000000000000000000000000000",  
INIT_8 =>  x"0000000000000000000000000000000000000000000000000000000000000000",  
INIT_9 =>  x"0000000000000000000000000000000000000000000000000000000000000000",  
INIT_A =>  x"0000000000000000000000000000000000000000000000000000000000000000",  
INIT_B =>  x"0000000000000000000000000000000000000000000000000000000000000000",  
INIT_C =>  x"0000000000000000000000000000000000000000000000000000000000000000",  
INIT_D =>  x"0000000000000000000000000000000000000000000000000000000000000000",  
INIT_E =>  x"0000000000000000000000000000000000000000000000000000000000000000",  
INIT_F =>  x"0000000000000000000000000000000000000000000000000000000000000000"
)

port map (  
RDATA => RDATA,  
RADDR => RADDR,  
RCLK => RCLK,  
RCLKE => RCLKE,  
RE => RE,  
WADDR => WADDR,  
WCLK => WCLK,  
WCLKE => WCLKE,  
WDATA => WDATA,  
MASK => MASK,  
WE => WE  
);
The following are the complete list of RAM4K based primitives

**SB_RAM4K**

```plaintext
SB_RAM4K // Posedge clock RCLK WCLK
(RDATA, RCLK, RCLKE, RE, RADDR, WCLK, WCLKE, WE, WADDR, MASK, WDATA);
```

**SB_RAM4KNR**

```plaintext
SB_RAM4KNR // Negative edged Read Clock – i.e. RCLKN
(RDATA, RCLKN, RCLKE, RE, RADDR, WCLK, WCLKE, WE, WADDR, MASK, WDATA);
```

**SB_RAM4KNW**

```plaintext
SB_RAM4KNW // Negative edged Write Clock – i.e. WCLKN
(RDATA, RCLK, RCLKE, RE, RADDR, WCLKN, WCLKE, WE, WADDR, MASK, WDATA);
```

**SB_RAM4KNRW**

```plaintext
SB_RAM4KNRNW // Negative edged Read and Write – i.e. RCLKN WRCKLN
(RDATA, RCLKN, RCLKE, RE, RADDR, WCLKN, WCLKE, WE, WADDR, MASK, WDATA);
```
**iCE40 Block RAM**

Each iCE40 device includes multiple high-speed synchronous RAM blocks, each 4Kbit in size. The RAM block has separate write and read ports, each with independent control signals. Each RAM block can be configured into a RAM block of size 256x16, 512x8, 1024x4 or 2048x2. The data contents of the RAM block are optionally pre-loaded during ICE device configuration.

The following table lists the supported dual port synchronous RAM configurations, each of 4Kbits in size. The RAM blocks can be directly instantiated in the top module and taken through iCube2 flow.

<table>
<thead>
<tr>
<th>Block RAM Configuration</th>
<th>Block RAM Size</th>
<th>WADDR Port Size (Bits)</th>
<th>WDATA Port Size (Bits)</th>
<th>RADDR Port Size (Bits)</th>
<th>RDATA Port Size (Bits)</th>
<th>MASK Port Size (Bits)</th>
</tr>
</thead>
<tbody>
<tr>
<td>SB_RAM256x16</td>
<td>256x16 (4K)</td>
<td>8 [7:0]</td>
<td>16 [15:0]</td>
<td>8 [7:0]</td>
<td>16 [15:0]</td>
<td></td>
</tr>
<tr>
<td>SB_RAM256x16NR</td>
<td>256x16 (4K)</td>
<td>8 [7:0]</td>
<td>16 [15:0]</td>
<td>8 [7:0]</td>
<td>16 [15:0]</td>
<td></td>
</tr>
<tr>
<td>SB_RAM256x16NW</td>
<td>256x16 (4K)</td>
<td>8 [7:0]</td>
<td>16 [15:0]</td>
<td>8 [7:0]</td>
<td>16 [15:0]</td>
<td></td>
</tr>
<tr>
<td>SB_RAM256x16NRNW</td>
<td>256x16 (4K)</td>
<td>8 [7:0]</td>
<td>16 [15:0]</td>
<td>8 [7:0]</td>
<td>16 [15:0]</td>
<td></td>
</tr>
<tr>
<td>SB_RAM512x8</td>
<td>512x8 (4K)</td>
<td>9 [8:0]</td>
<td>8 [7:0]</td>
<td>8 [7:0]</td>
<td>No Mask Port</td>
<td></td>
</tr>
<tr>
<td>SB_RAM512x8NR</td>
<td>512x8 (4K)</td>
<td>9 [8:0]</td>
<td>8 [7:0]</td>
<td>8 [7:0]</td>
<td>No Mask Port</td>
<td></td>
</tr>
<tr>
<td>SB_RAM512x8NW</td>
<td>512x8 (4K)</td>
<td>9 [8:0]</td>
<td>8 [7:0]</td>
<td>8 [7:0]</td>
<td>No Mask Port</td>
<td></td>
</tr>
<tr>
<td>SB_RAM512x8NRNW</td>
<td>512x8 (4K)</td>
<td>9 [8:0]</td>
<td>8 [7:0]</td>
<td>8 [7:0]</td>
<td>No Mask Port</td>
<td></td>
</tr>
<tr>
<td>SB_RAM2048x2</td>
<td>2048x2 (4K)</td>
<td>11 [10:0]</td>
<td>2 [1:0]</td>
<td>10 [9:0]</td>
<td>2 [1:0]</td>
<td>No Mask Port</td>
</tr>
<tr>
<td>SB_RAM2048x2NR</td>
<td>2048x2 (4K)</td>
<td>11 [10:0]</td>
<td>2 [1:0]</td>
<td>10 [9:0]</td>
<td>2 [1:0]</td>
<td>No Mask Port</td>
</tr>
<tr>
<td>SB_RAM2048x2NW</td>
<td>2048x2 (4K)</td>
<td>11 [10:0]</td>
<td>2 [1:0]</td>
<td>10 [9:0]</td>
<td>2 [1:0]</td>
<td>No Mask Port</td>
</tr>
<tr>
<td>SB_RAM2048x2NRNW</td>
<td>2048x2 (4K)</td>
<td>11 [10:0]</td>
<td>2 [1:0]</td>
<td>10 [9:0]</td>
<td>2 [1:0]</td>
<td>No Mask Port</td>
</tr>
</tbody>
</table>

The SiliconBlue Technologies convention for the iCE40 RAM primitives with negedge Read or Write clock is that the base primitive name is post fixed with N and R or W according to the clock that is affected, as displayed in the table below for 256x16 RAM block configuration.

<table>
<thead>
<tr>
<th>RAM Primitive Name</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>SB_RAM256x16</td>
<td>Posedge Read clock, Posedge Write clock</td>
</tr>
<tr>
<td>SB_RAM4256x16NR</td>
<td>Negedge Read clock, Posedge Write clock</td>
</tr>
<tr>
<td>SB_RAM256x16NW</td>
<td>Posedge Read clock, Negedge Write clock</td>
</tr>
<tr>
<td>SB_RAM256x16NRNW</td>
<td>Negedge Read clock, Negedge Write clock</td>
</tr>
</tbody>
</table>
The following modules are the complete list of SB_RAM256x16 based primitives

**SB_RAM256x16**

(sbdata, rclk, rclke, re, raddr, wclk, wclke, we, waddr, mask, wdata);

Verilog Instantiation:

```verilog
SB_RAM256x16   ram256x16_inst (  
   .RDATA(RDATA_c[15:0]),
   .RADDR(RADDR_c[7:0]),
   .RCLK(RCLK_c),
   .RCLKE(RCLKE_c),
   .RE(RE_c),
   .WADDR(WADDR_c[7:0]),
   .WCLK(WCLK_c),
   .WCLKE(WCLKE_c),
   .WDATA(WDATA_c[15:0]),
   .WE(WE_c),
   .MASK(MASK_c[15:0])
);

defparam ram256x16_inst.INIT_0 = 256'h0000000000000000000000000000000000000000000000000000000000000000;
defparam ram256x16_inst.INIT_1 = 256'h0000000000000000000000000000000000000000000000000000000000000000;
defparam ram256x16_inst.INIT_2 = 256'h0000000000000000000000000000000000000000000000000000000000000000;
defparam ram256x16_inst.INIT_3 = 256'h0000000000000000000000000000000000000000000000000000000000000000;
defparam ram256x16_inst.INIT_4 = 256'h0000000000000000000000000000000000000000000000000000000000000000;
defparam ram256x16_inst.INIT_5 = 256'h0000000000000000000000000000000000000000000000000000000000000000;
```
VHDL Instantiation:

```vhdl
ram256x16_inst : SB_RAM256x16
generic map (    INIT_0 =>    X"0000000000000000000000000000000000000000000000000000000000000000",
                INIT_1 =>    X"0000000000000000000000000000000000000000000000000000000000000000",
                INIT_2 =>    X"0000000000000000000000000000000000000000000000000000000000000000",
                INIT_3 =>    X"0000000000000000000000000000000000000000000000000000000000000000",
                INIT_4 =>    X"0000000000000000000000000000000000000000000000000000000000000000",
                INIT_5 =>    X"0000000000000000000000000000000000000000000000000000000000000000",
                INIT_6 =>    X"0000000000000000000000000000000000000000000000000000000000000000",
                INIT_7 =>    X"0000000000000000000000000000000000000000000000000000000000000000",
                INIT_8 =>    X"0000000000000000000000000000000000000000000000000000000000000000",
                INIT_9 =>    X"0000000000000000000000000000000000000000000000000000000000000000",
                INIT_A =>    X"0000000000000000000000000000000000000000000000000000000000000000",
                INIT_B =>    X"0000000000000000000000000000000000000000000000000000000000000000",
                INIT_C =>    X"0000000000000000000000000000000000000000000000000000000000000000",
                INIT_D =>    X"0000000000000000000000000000000000000000000000000000000000000000",
                INIT_E =>    X"0000000000000000000000000000000000000000000000000000000000000000",
                INIT_F =>    X"0000000000000000000000000000000000000000000000000000000000000000"
            )
port map (    RDATA => RDATA_c,
                RADDR => RADDR_c,
                RCLK => RCLK_c,
                RCLKE => RCLKE_c,
                RE => RE_c,
```

WADDR => WADDR_c,  
WCLK => WCLK_c,  
WCLKE => WCLKE_c,  
WDATA => WDATA_c,  
MASK => MASK_c,  
WE => WE_c)

SB_RAM256x16NR

SB_RAM256x16NR  // Negative edged Read Clock – i.e. RCLKN
(RDATA, RCLKN, RCLKE, RE, RADDR, WCLK, WCLKE, WE, WADDR, MASK, WDATA);

Verilog Instantiation:

SB_RAM256x16NR   ram256x16NR_inst (  
    .RDATA(RDATA_c[15:0]),  
    .RADDR(RADDR_c[7:0]),  
    .RCLKN(RCLKN_c),  
    .RCLKE(RCLKE_c),  
    .RE(RE_c),  
    .WADDR(WADDR_c[7:0]),  
    .WCLK(WCLK_c),  
    .WCLKE(WCLKE_c),  
    .WDATA(WDATA_c[15:0]),  
    .WE(WE_c),  
    .MASK(MASK_c[15:0])  
);  
defparam ram256x16nr_inst.INIT_0 =  
256'h0000000000000000000000000000000000000000000000000000000000000000;  
defparam ram256x16nr_inst.INIT_1 =  
256'h0000000000000000000000000000000000000000000000000000000000000000;  
defparam ram256x16nr_inst.INIT_2 =  
256'h0000000000000000000000000000000000000000000000000000000000000000;  
defparam ram256x16nr_inst.INIT_3 =  
256'h0000000000000000000000000000000000000000000000000000000000000000;  
defparam ram256x16nr_inst.INIT_4 =  
256'h0000000000000000000000000000000000000000000000000000000000000000;  
defparam ram256x16nr_inst.INIT_5 =  
256'h0000000000000000000000000000000000000000000000000000000000000000;  
defparam ram256x16nr_inst.INIT_6 =  
256'h0000000000000000000000000000000000000000000000000000000000000000;  
defparam ram256x16nr_inst.INIT_7 =  
256'h0000000000000000000000000000000000000000000000000000000000000000;  
defparam ram256x16nr_inst.INIT_8 =  
256'h0000000000000000000000000000000000000000000000000000000000000000;  
defparam ram256x16nr_inst.INIT_9 =  
256'h0000000000000000000000000000000000000000000000000000000000000000;  
defparam ram256x16nr_inst.INIT_A =  
256'h0000000000000000000000000000000000000000000000000000000000000000;  
defparam ram256x16nr_inst.INIT_B =  
256'h0000000000000000000000000000000000000000000000000000000000000000;  
defparam ram256x16nr_inst.INIT_C =  
256'h0000000000000000000000000000000000000000000000000000000000000000;  
defparam ram256x16nr_inst.INIT_D =  
256'h0000000000000000000000000000000000000000000000000000000000000000;  
defparam ram256x16nr_inst.INIT_E =  
256'h0000000000000000000000000000000000000000000000000000000000000000;  
defparam ram256x16nr_inst.INIT_F =  
256'h0000000000000000000000000000000000000000000000000000000000000000;
VHDL Instantiation:

```vhdl
ram256x16nr_inst : SB_RAM256x16NR
generic map (  
    INIT_0 =>
        X"0000000000000000000000000000000000000000000000000000000000000000",
    INIT_1 =>
        X"0000000000000000000000000000000000000000000000000000000000000000",
    INIT_2 =>
        X"0000000000000000000000000000000000000000000000000000000000000000",
    INIT_3 =>
        X"0000000000000000000000000000000000000000000000000000000000000000",
    INIT_4 =>
        X"0000000000000000000000000000000000000000000000000000000000000000",
    INIT_5 =>
        X"0000000000000000000000000000000000000000000000000000000000000000",
    INIT_6 =>
        X"0000000000000000000000000000000000000000000000000000000000000000",
    INIT_7 =>
        X"0000000000000000000000000000000000000000000000000000000000000000",
    INIT_8 =>
        X"0000000000000000000000000000000000000000000000000000000000000000",
    INIT_9 =>
        X"0000000000000000000000000000000000000000000000000000000000000000",
    INIT_A =>
        X"0000000000000000000000000000000000000000000000000000000000000000",
    INIT_B =>
        X"0000000000000000000000000000000000000000000000000000000000000000",
    INIT_C =>
        X"0000000000000000000000000000000000000000000000000000000000000000",
    INIT_D =>
        X"0000000000000000000000000000000000000000000000000000000000000000",
    INIT_E =>
        X"0000000000000000000000000000000000000000000000000000000000000000",
    INIT_F =>
        X"0000000000000000000000000000000000000000000000000000000000000000"
        )
port map (  
    RDATA => RDATA_c,
    RADDR => RADDR_c,
    RCLKN => RCLKN_c,
    RCLKE => RCLKE_c,
    RE => RE_c,
    WADDR => WADDR_c,
    WCLK => WCLK_c,
    WCLKE => WCLKE_c,
    WDATA => WDATA_c,
    MASK => MASK_c,
    WE => WE_c
    );
```

**SB_RAM256x16NW**

SB_RAM256x16NW // Negative edged Write Clock – i.e. WCLKN
(RDATA, RCLK, RCLKE, RE, RADDR, WCLKN, WCLKE, WE, WADDR, MASK, WDATA);
Verilog Instantiation:

SB_RAM256x16NW ram256x16nw_inst (  
  .RDATA(RDATA_c[15:0]),
  .RADDR(RADDR_c[7:0]),
  .RCLK(RCLK_c),
  .RCLKE(RCLKE_c),
  .RE(RE_c),
  .WADDR(WADDR_c[7:0]),
  .WCLK(NW(WCLK_c)),
  .WCLKE(WCLKE_c),
  .WDATA(WDATA_c[15:0]),
  .WE(WE_c),
  .MASK(MASK_c[15:0])
);
defparam ram256x16nw_inst.INIT_0 = 256'h0000000000000000000000000000000000000000000000000000000000000000;
defparam ram256x16nw_inst.INIT_1 = 256'h0000000000000000000000000000000000000000000000000000000000000000;
defparam ram256x16nw_inst.INIT_2 = 256'h0000000000000000000000000000000000000000000000000000000000000000;
defparam ram256x16nw_inst.INIT_3 = 256'h0000000000000000000000000000000000000000000000000000000000000000;
defparam ram256x16nw_inst.INIT_4 = 256'h0000000000000000000000000000000000000000000000000000000000000000;
defparam ram256x16nw_inst.INIT_5 = 256'h0000000000000000000000000000000000000000000000000000000000000000;
defparam ram256x16nw_inst.INIT_6 = 256'h0000000000000000000000000000000000000000000000000000000000000000;
defparam ram256x16nw_inst.INIT_7 = 256'h0000000000000000000000000000000000000000000000000000000000000000;
defparam ram256x16nw_inst.INIT_8 = 256'h0000000000000000000000000000000000000000000000000000000000000000;
defparam ram256x16nw_inst.INIT_9 = 256'h0000000000000000000000000000000000000000000000000000000000000000;
defparam ram256x16nw_inst.INIT_A = 256'h0000000000000000000000000000000000000000000000000000000000000000;
defparam ram256x16nw_inst.INIT_B = 256'h0000000000000000000000000000000000000000000000000000000000000000;
defparam ram256x16nw_inst.INIT_C = 256'h0000000000000000000000000000000000000000000000000000000000000000;
defparam ram256x16nw_inst.INIT_D = 256'h0000000000000000000000000000000000000000000000000000000000000000;
defparam ram256x16nw_inst.INIT_E = 256'h0000000000000000000000000000000000000000000000000000000000000000;
defparam ram256x16nw_inst.INIT_F = 256'h0000000000000000000000000000000000000000000000000000000000000000;

VHDL Instantiation:

ram256x16nw_inst : SB_RAM256x16NW
generic map (  
  INIT_0 =>  
  X"0000000000000000000000000000000000000000000000000000000000000000",
  INIT_1 =>  
  X"0000000000000000000000000000000000000000000000000000000000000000",
  INIT_2 =>  
  X"0000000000000000000000000000000000000000000000000000000000000000",
  INIT_3 =>  
  X"0000000000000000000000000000000000000000000000000000000000000000",
  INIT_4 =>  
  X"0000000000000000000000000000000000000000000000000000000000000000",
  INIT_5 =>  
  X"0000000000000000000000000000000000000000000000000000000000000000",
  INIT_6 =>  
  X"0000000000000000000000000000000000000000000000000000000000000000",
  INIT_7 =>  
  X"0000000000000000000000000000000000000000000000000000000000000000",
  INIT_8 =>  
  X"0000000000000000000000000000000000000000000000000000000000000000",
  INIT_9 =>  
  X"0000000000000000000000000000000000000000000000000000000000000000",
  INIT_A =>  
  X"0000000000000000000000000000000000000000000000000000000000000000",
  INIT_B =>  
  X"0000000000000000000000000000000000000000000000000000000000000000",
  INIT_C =>  
  X"0000000000000000000000000000000000000000000000000000000000000000",
  INIT_D =>  
  X"0000000000000000000000000000000000000000000000000000000000000000",
  INIT_E =>  
  X"0000000000000000000000000000000000000000000000000000000000000000",
  INIT_F =>  
  X"0000000000000000000000000000000000000000000000000000000000000000"
INIT_5 => X"0000000000000000000000000000000000000000000000000000000000000000",
INIT_6 => X"0000000000000000000000000000000000000000000000000000000000000000",
INIT_7 => X"0000000000000000000000000000000000000000000000000000000000000000",
INIT_8 => X"0000000000000000000000000000000000000000000000000000000000000000",
INIT_9 => X"0000000000000000000000000000000000000000000000000000000000000000",
INIT_A => X"0000000000000000000000000000000000000000000000000000000000000000",
INIT_B => X"0000000000000000000000000000000000000000000000000000000000000000",
INIT_C => X"0000000000000000000000000000000000000000000000000000000000000000",
INIT_D => X"0000000000000000000000000000000000000000000000000000000000000000",
INIT_E => X"0000000000000000000000000000000000000000000000000000000000000000",
INIT_F => X"0000000000000000000000000000000000000000000000000000000000000000"
);

port map (
    RDATA => RDATA_c,
    RADDR => RADDR_c,
    RCLK => RCLK_c,
    RCLKE => RCLKE_c,
    RE => RE_c,
    WADDR => WADDR_c,
    WCLK => WCLK_c,
    WCLKE => WCLKE_c,
    WDATA => WDATA_c,
    WE => WE_c,
    MASK => MASK_c,
);

SB_RAM256x16NRNW

SB_RAM256x16NRNW  // Negative edged Read and Write – i.e. RCLKN WRCKLN
(RDATA, RCLKN, RCLKE, RE, RADDR, WCLKN, WCLKE, WE, WADDR, MASK, WDATA);

Verilog Instantiation:

SB_RAM256x16NRNW  ram256x16nrnw_inst (
    .RDATA(RDATA_c[15:0]),
    .RADDR(RADDR_c[7:0]),
    .RCLKN(RCLKN_c),
    .RCLKE(RCLKE_c),
    .RE(RE_c),
    .WADDR(WADDR_c[7:0]),
    .WCLKN(WCLKN_c),
    .WCLKE(WCLKE_c),
    .WDATA(WDATA_c[15:0]),
    .WE(WE_c),
    .MASK(MASK_c[15:0])
);
defparam ram256x16nrnw_inst.INIT_0 = 256'h0000000000000000000000000000000000000000000000000000000000000000;
defparam ram256x16nrnw_inst.INIT_1 = 256'h0000000000000000000000000000000000000000000000000000000000000000;
VHDL Instantiation:

```vhdl
ram256x16nrnw_inst : SB_RAM256x16NRNW
generic map(
  INIT_0 =>
    x"0000000000000000000000000000000000000000000000000000000000000000",
  INIT_1 =>
    x"0000000000000000000000000000000000000000000000000000000000000000",
  INIT_2 =>
    x"0000000000000000000000000000000000000000000000000000000000000000",
  INIT_3 =>
    x"0000000000000000000000000000000000000000000000000000000000000000",
  INIT_4 =>
    x"0000000000000000000000000000000000000000000000000000000000000000",
  INIT_5 =>
    x"0000000000000000000000000000000000000000000000000000000000000000",
  INIT_6 =>
    x"0000000000000000000000000000000000000000000000000000000000000000",
  INIT_7 =>
    x"0000000000000000000000000000000000000000000000000000000000000000",
  INIT_8 =>
    x"0000000000000000000000000000000000000000000000000000000000000000",
  INIT_9 =>
    x"0000000000000000000000000000000000000000000000000000000000000000",
  INIT_A =>
    x"0000000000000000000000000000000000000000000000000000000000000000",
  INIT_B =>
    x"0000000000000000000000000000000000000000000000000000000000000000",
  INIT_C =>
    x"0000000000000000000000000000000000000000000000000000000000000000",
  INIT_D =>
    x"0000000000000000000000000000000000000000000000000000000000000000",
  INIT_E =>
    x"0000000000000000000000000000000000000000000000000000000000000000",
  INIT_F =>
    x"0000000000000000000000000000000000000000000000000000000000000000",
)
end ram256x16nrnw_inst;
```
INIT_F => x"0000000000000000000000000000000000000000000000000000000000000000"
)
port map (  
  RDATA => RDATA_c,  
  RADDR => RADDR_c,  
  RCLKN => RCLKN_c,  
  RCLKE => RCLKE_c,  
  RE => RE_c,  
  WADDR => WADDR_c,  
  WCLKN=> WCLKN_c,  
  WCLKE => WCLKE_c,  
  WDATA => WDATA_c,  
  MASK => MASK_c,  
  WE => WE_c  
);

The following modules are the complete list of SB_RAM512x8 based primitives

```
SB_RAM512x8 //Posedge clock RCLK WCLK
(RDATA, RCLK, RCLKE, RE, RADDR, WCLK, WCLKE, WE, WADDR, MASK, WDATA);
```

Verilog Instantiation:

```
SB_RAM512x8   ram512x8_inst (  
    .RDATA(RDATA_c[7:0]),
    .RADDR(RADDR_c[8:0]),
    .RCLK(RCLK_c),
    .RCLKE(RCLKE_c),
    .RE(RE_c),
    .WADDR(WADDR_c[8:0]),
    .WCLK(WCLK_c),
    .WCLKE(WCLKE_c),
    .WDATA(WDATA_c[7:0]),
    .WE(WE_c)
);
```

defparam ram512x8_inst.INIT_0 =
256'h0000000000000000000000000000000000000000000000000000000000000000;

defparam ram512x8_inst.INIT_1 =
256'h0000000000000000000000000000000000000000000000000000000000000000;

defparam ram512x8_inst.INIT_2 =
256'h0000000000000000000000000000000000000000000000000000000000000000;

defparam ram512x8_inst.INIT_3 =
256'h0000000000000000000000000000000000000000000000000000000000000000;

defparam ram512x8_inst.INIT_4 =
256'h0000000000000000000000000000000000000000000000000000000000000000;

defparam ram512x8_inst.INIT_5 =
256'h0000000000000000000000000000000000000000000000000000000000000000;
defparam ram512x8_inst.INIT_6 = 256'h0000000000000000000000000000000000000000000000000000000000000000;
defparam ram512x8_inst.INIT_7 = 256'h0000000000000000000000000000000000000000000000000000000000000000;
defparam ram512x8_inst.INIT_8 = 256'h0000000000000000000000000000000000000000000000000000000000000000;
defparam ram512x8_inst.INIT_9 = 256'h0000000000000000000000000000000000000000000000000000000000000000;
defparam ram512x8_inst.INIT_A = 256'h0000000000000000000000000000000000000000000000000000000000000000;
defparam ram512x8_inst.INIT_B = 256'h0000000000000000000000000000000000000000000000000000000000000000;
defparam ram512x8_inst.INIT_C = 256'h0000000000000000000000000000000000000000000000000000000000000000;
defparam ram512x8_inst.INIT_D = 256'h0000000000000000000000000000000000000000000000000000000000000000;
defparam ram512x8_inst.INIT_E = 256'h0000000000000000000000000000000000000000000000000000000000000000;
defparam ram512x8_inst.INIT_F = 256'h0000000000000000000000000000000000000000000000000000000000000000;

VHDL Instantiation:

ram512x8_inst : SB_RAM512x8
genéric map (  
INIT_0 =>
X"0000000000000000000000000000000000000000000000000000000000000000",
INIT_1 =>
X"0000000000000000000000000000000000000000000000000000000000000000",
INIT_2 =>
X"0000000000000000000000000000000000000000000000000000000000000000",
INIT_3 =>
X"0000000000000000000000000000000000000000000000000000000000000000",
INIT_4 =>
X"0000000000000000000000000000000000000000000000000000000000000000",
INIT_5 =>
X"0000000000000000000000000000000000000000000000000000000000000000",
INIT_6 =>
X"0000000000000000000000000000000000000000000000000000000000000000",
INIT_7 =>
X"0000000000000000000000000000000000000000000000000000000000000000",
INIT_8 =>
X"0000000000000000000000000000000000000000000000000000000000000000",
INIT_9 =>
X"0000000000000000000000000000000000000000000000000000000000000000",
INIT_A =>
X"0000000000000000000000000000000000000000000000000000000000000000",
INIT_B =>
X"0000000000000000000000000000000000000000000000000000000000000000",
INIT_C =>
X"0000000000000000000000000000000000000000000000000000000000000000",
INIT_D =>
X"0000000000000000000000000000000000000000000000000000000000000000",
INIT_E =>
X"0000000000000000000000000000000000000000000000000000000000000000",
INIT_F =>
X"0000000000000000000000000000000000000000000000000000000000000000"
  );
port map (  
  RDATA => RDATA_c,  
  RADDR => RADDR_c,  
  RCLK => RCLK_c,  
  RCLKE => RCLKE_c,  
  RE => RE_c,
WADDR => WADDR_c,  
WCLK=> WCLK_c,  
WCLKE => WCLKE_c,  
WDATA => WDATA_c,  
WE => WE_c  
);

SB_RAM512x8NR

SB_RAM512x8NR // Negative edged Read Clock – i.e. RCLKN  
(RDATA, RCLKN, RCLKE, RE, RADDR, WCLK, WCLKE, WE, WADDR, MASK, WDATA);

Verilog Instantiation:

SB_RAM512x8NR ram512x8nr_inst (  
   .RDATA(RDATA_c[7:0]),  
   .RADDR(RADDR_c[8:0]),  
   .RCLKN(RCLKN_c),  
   .RCLKE(RCLKE_c),  
   .RE(RE_c),  
   .WADDR(WADDR_c[8:0]),  
   .WCLK(WCLK_c),  
   .WCLKE(WCLKE_c),  
   .WDATA(WDATA_c[7:0]),  
   .WE(WE_c)  
);

defparam ram512x8nr_inst.INIT_0 = 256'h0000000000000000000000000000000000000000000000000000000000000000;  
defparam ram512x8nr_inst.INIT_1 = 256'h0000000000000000000000000000000000000000000000000000000000000000;  
defparam ram512x8nr_inst.INIT_2 = 256'h0000000000000000000000000000000000000000000000000000000000000000;  
defparam ram512x8nr_inst.INIT_3 = 256'h0000000000000000000000000000000000000000000000000000000000000000;  
defparam ram512x8nr_inst.INIT_4 = 256'h0000000000000000000000000000000000000000000000000000000000000000;  
defparam ram512x8nr_inst.INIT_5 = 256'h0000000000000000000000000000000000000000000000000000000000000000;  
defparam ram512x8nr_inst.INIT_6 = 256'h0000000000000000000000000000000000000000000000000000000000000000;  
defparam ram512x8nr_inst.INIT_7 = 256'h0000000000000000000000000000000000000000000000000000000000000000;  
defparam ram512x8nr_inst.INIT_8 = 256'h0000000000000000000000000000000000000000000000000000000000000000;  
defparam ram512x8nr_inst.INIT_9 = 256'h0000000000000000000000000000000000000000000000000000000000000000;  
defparam ram512x8nr_inst.INIT_A = 256'h0000000000000000000000000000000000000000000000000000000000000000;  
defparam ram512x8nr_inst.INIT_B = 256'h0000000000000000000000000000000000000000000000000000000000000000;  
defparam ram512x8nr_inst.INIT_C = 256'h0000000000000000000000000000000000000000000000000000000000000000;  
defparam ram512x8nr_inst.INIT_D = 256'h0000000000000000000000000000000000000000000000000000000000000000;  
defparam ram512x8nr_inst.INIT_E = 256'h0000000000000000000000000000000000000000000000000000000000000000;  
defparam ram512x8nr_inst.INIT_F = 256'h0000000000000000000000000000000000000000000000000000000000000000;
VHDL Instantiation:

```vhdl
ram512x8nr_inst: SB_RAM512x8NR
generic map (  
  INIT_0 =>
  x"0000000000000000000000000000000000000000000000000000000000000000",
  INIT_1 =>
  x"0000000000000000000000000000000000000000000000000000000000000000",
  INIT_2 =>
  x"0000000000000000000000000000000000000000000000000000000000000000",
  INIT_3 =>
  x"0000000000000000000000000000000000000000000000000000000000000000",
  INIT_4 =>
  x"0000000000000000000000000000000000000000000000000000000000000000",
  INIT_5 =>
  x"0000000000000000000000000000000000000000000000000000000000000000",
  INIT_6 =>
  x"0000000000000000000000000000000000000000000000000000000000000000",
  INIT_7 =>
  x"0000000000000000000000000000000000000000000000000000000000000000",
  INIT_8 =>
  x"0000000000000000000000000000000000000000000000000000000000000000",
  INIT_9 =>
  x"0000000000000000000000000000000000000000000000000000000000000000",
  INIT_A =>
  x"0000000000000000000000000000000000000000000000000000000000000000",
  INIT_B =>
  x"0000000000000000000000000000000000000000000000000000000000000000",
  INIT_C =>
  x"0000000000000000000000000000000000000000000000000000000000000000",
  INIT_D =>
  x"0000000000000000000000000000000000000000000000000000000000000000",
  INIT_E =>
  x"0000000000000000000000000000000000000000000000000000000000000000",
  INIT_F =>
  x"0000000000000000000000000000000000000000000000000000000000000000"
)  
port map (  
  RDATA => RDATA_c,  
  RADDR => RADDR_c,  
  RCLK => RCLK_N_c,  
  RCLKE => RCLKE_c,  
  RE => RE_c,  
  WADDR => WADDR_c,  
  WCLK => WCLK_c,  
  WCLKE => WCLKE_c,  
  WDATA => WDATA_c,  
  WE => WE_c  
);  
```

**SB_RAM512x8NW**

`SB_RAM512x8NW`  // Negative edged Write Clock – i.e. WCLKN
(RDATA, RCLK, RCLKE, RE, RADDR, WCLKN, WCLKE, WE, WADDR, MASK, WDATA);

Verilog Instantiation:

```verilog
SB_RAM512x8NW  ram512x8nw_inst (  
  .RDAT(A(RDATA_c[7:0]),  
  .RADDR(RADDR_c[8:0]),
```
.RCLK(RCLK_c),
.RCLKE(RCLKE_c),
.RE(RE_c),
.WADDR(WADDR_c[8:0]),
.WCLKN(WCLKN_c),
.WCLKE(WCLKE_c),
.WDATA(WDATA_c[7:0]),
.WE(WE_c);

defparam ram512x8nw_inst.INIT_0 = 256'h0000000000000000000000000000000000000000000000000000000000000000;
defparam ram512x8nw_inst.INIT_1 = 256'h0000000000000000000000000000000000000000000000000000000000000000;
defparam ram512x8nw_inst.INIT_2 = 256'h0000000000000000000000000000000000000000000000000000000000000000;
defparam ram512x8nw_inst.INIT_3 = 256'h0000000000000000000000000000000000000000000000000000000000000000;
defparam ram512x8nw_inst.INIT_4 = 256'h0000000000000000000000000000000000000000000000000000000000000000;
defparam ram512x8nw_inst.INIT_5 = 256'h0000000000000000000000000000000000000000000000000000000000000000;
defparam ram512x8nw_inst.INIT_6 = 256'h0000000000000000000000000000000000000000000000000000000000000000;
defparam ram512x8nw_inst.INIT_7 = 256'h0000000000000000000000000000000000000000000000000000000000000000;
defparam ram512x8nw_inst.INIT_8 = 256'h0000000000000000000000000000000000000000000000000000000000000000;
defparam ram512x8nw_inst.INIT_9 = 256'h0000000000000000000000000000000000000000000000000000000000000000;
defparam ram512x8nw_inst.INIT_A = 256'h0000000000000000000000000000000000000000000000000000000000000000;
defparam ram512x8nw_inst.INIT_B = 256'h0000000000000000000000000000000000000000000000000000000000000000;
defparam ram512x8nw_inst.INIT_C = 256'h0000000000000000000000000000000000000000000000000000000000000000;
defparam ram512x8nw_inst.INIT_D = 256'h0000000000000000000000000000000000000000000000000000000000000000;
defparam ram512x8nw_inst.INIT_E = 256'h0000000000000000000000000000000000000000000000000000000000000000;
defparam ram512x8nw_inst.INIT_F = 256'h0000000000000000000000000000000000000000000000000000000000000000;

VHDL Instantiation:

ram512x8nw_inst: SB_RAM512x8NW
generic map (
  INIT_0 => x"0000000000000000000000000000000000000000000000000000000000000000",
  INIT_1 => x"0000000000000000000000000000000000000000000000000000000000000000",
  INIT_2 => x"0000000000000000000000000000000000000000000000000000000000000000",
  INIT_3 => x"0000000000000000000000000000000000000000000000000000000000000000",
  INIT_4 => x"0000000000000000000000000000000000000000000000000000000000000000",
  INIT_5 => x"0000000000000000000000000000000000000000000000000000000000000000",
  INIT_6 => x"0000000000000000000000000000000000000000000000000000000000000000",
  INIT_7 => x"0000000000000000000000000000000000000000000000000000000000000000",
  INIT_8 => x"0000000000000000000000000000000000000000000000000000000000000000",
  INIT_9 => x"0000000000000000000000000000000000000000000000000000000000000000",
  INIT_A => x"0000000000000000000000000000000000000000000000000000000000000000",
  INIT_B => x"0000000000000000000000000000000000000000000000000000000000000000",
  INIT_C => x"0000000000000000000000000000000000000000000000000000000000000000",
  INIT_D => x"0000000000000000000000000000000000000000000000000000000000000000",
  INIT_E => x"0000000000000000000000000000000000000000000000000000000000000000",
  INIT_F => x"0000000000000000000000000000000000000000000000000000000000000000"
);
INIT_8 => x"0000000000000000000000000000000000000000000000000000000000000000",
INIT_9 => x"0000000000000000000000000000000000000000000000000000000000000000",
INIT_A => x"0000000000000000000000000000000000000000000000000000000000000000",
INIT_B => x"0000000000000000000000000000000000000000000000000000000000000000",
INIT_C => x"0000000000000000000000000000000000000000000000000000000000000000",
INIT_D => x"0000000000000000000000000000000000000000000000000000000000000000",
INIT_E => x"0000000000000000000000000000000000000000000000000000000000000000",
INIT_F => x"0000000000000000000000000000000000000000000000000000000000000000"
)
port map (  
  RDATA => RDATA_C,  
  RADDR => RADDR_C,  
  RCLK => RCLK_C,  
  RCLKE => RCLKE_C,  
  RE => RE_C,  
  WADDR => WADDR_C,  
  WCLKN=> WCLKN_C,  
  WCLKE => WCLKE_C,  
  WDATA => WDATA_C,  
  WE => WE_C  
);

\textbf{SB\_RAM512x8NRNW}

\textbf{SB\_RAM512x8NRNW} // Negative edged Read and Write – i.e. RCLKN WRCKLN
(RDATA, RCLKN, RCLKE, RE, RADDR, WCLKN, WCLKE, WE, WADDR, MASK, WDATA); Verilog Instantiation:

SB\_RAM512x8NRNW \quad \text{ram512x8nrnw\_inst (  
  .RDATA(RDATA_c[7:0]),  
  .RADDR(RADDR_c[8:0]),  
  .RCLKN(RCLK_c),  
  .RCLKE(RCLKE_c),  
  .RE(RE_C),  
  .WADDR(WADDR_c[8:0]),  
  .WCLKN(WCLK_c),  
  .WCLKE(WCLKE_c),  
  .WDATA(WDATA_c[7:0]),  
  .WE(WE_C)  
)}

defparam ram512x8nrnw\_inst.INIT_0 = 256'h0000000000000000000000000000000000000000000000000000000000000000;
defparam ram512x8nrnw\_inst.INIT_1 = 256'h0000000000000000000000000000000000000000000000000000000000000000;
defparam ram512x8nrnw\_inst.INIT_2 = 256'h0000000000000000000000000000000000000000000000000000000000000000;
defparam ram512x8nrnw\_inst.INIT_3 = 256'h0000000000000000000000000000000000000000000000000000000000000000;
defparam ram512x8nrnw\_inst.INIT_4 = 256'h0000000000000000000000000000000000000000000000000000000000000000;

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defparam ram512x8nrnw_inst.INIT_5 = 256'h0000000000000000000000000000000000000000000000000000000000000000;
defparam ram512x8nrnw_inst.INIT_6 = 256'h0000000000000000000000000000000000000000000000000000000000000000;
defparam ram512x8nrnw_inst.INIT_7 = 256'h0000000000000000000000000000000000000000000000000000000000000000;
defparam ram512x8nrnw_inst.INIT_8 = 256'h0000000000000000000000000000000000000000000000000000000000000000;
defparam ram512x8nrnw_inst.INIT_9 = 256'h0000000000000000000000000000000000000000000000000000000000000000;
defparam ram512x8nrnw_inst.INIT_A = 256'h0000000000000000000000000000000000000000000000000000000000000000;
defparam ram512x8nrnw_inst.INIT_B = 256'h0000000000000000000000000000000000000000000000000000000000000000;
defparam ram512x8nrnw_inst.INIT_C = 256'h0000000000000000000000000000000000000000000000000000000000000000;
defparam ram512x8nrnw_inst.INIT_D = 256'h0000000000000000000000000000000000000000000000000000000000000000;
defparam ram512x8nrnw_inst.INIT_E = 256'h0000000000000000000000000000000000000000000000000000000000000000;
defparam ram512x8nrnw_inst.INIT_F = 256'h0000000000000000000000000000000000000000000000000000000000000000;

VHDL Instantiation:

ram512x8nrnw_inst: SB_RAM512x8NRNW
            generic map (   
                INIT_0 => x"0000000000000000000000000000000000000000000000000000000000000000",
                INIT_1 => x"0000000000000000000000000000000000000000000000000000000000000000",
                INIT_2 => x"0000000000000000000000000000000000000000000000000000000000000000",
                INIT_3 => x"0000000000000000000000000000000000000000000000000000000000000000",
                INIT_4 => x"0000000000000000000000000000000000000000000000000000000000000000",
                INIT_5 => x"0000000000000000000000000000000000000000000000000000000000000000",
                INIT_6 => x"0000000000000000000000000000000000000000000000000000000000000000",
                INIT_7 => x"0000000000000000000000000000000000000000000000000000000000000000",
                INIT_8 => x"0000000000000000000000000000000000000000000000000000000000000000",
                INIT_9 => x"0000000000000000000000000000000000000000000000000000000000000000",
                INIT_A => x"0000000000000000000000000000000000000000000000000000000000000000",
                INIT_B => x"0000000000000000000000000000000000000000000000000000000000000000",
                INIT_C => x"0000000000000000000000000000000000000000000000000000000000000000",
                INIT_D => x"0000000000000000000000000000000000000000000000000000000000000000",
                INIT_E => x"0000000000000000000000000000000000000000000000000000000000000000",
                INIT_F => x"0000000000000000000000000000000000000000000000000000000000000000"
            )
            port map (   
                RDATA => RDATA_c,
                RADDR => RADDR_c,
                RCLKN => RCLKN_c,
RCLKE => RCLKE_c,
RE => RE_c,
WADDR => WADDR_c,
WCLKN => WCLKN_c,
WCLKE => WCLKE_c,
WDATA => WDATA_c,
WE => WE_c
);
The following modules are the complete list of SB_RAM1024x4 based primitives

**SB_RAM1024x4**

**SB_RAM1024x4**  //Posedge clock RCLK WCLK  
(RDATA, RCLK, RCLKE, RE, RADDR, WCLK, WCLKE, WE, WADDR, MASK, WDATA);

Verilog Instantiation:

```verilog
SB_RAM1024x4   ram1024x4_inst (  
   .RDATA(RDATA_c[3:0]),  
   .RADDR(RADDR_c[9:0]),  
   .RCLK(RCLK_c),  
   .RCLKE(RCLKE_c),  
   .RE(RE_c),  
   .WADDR(WADDR_c[3:0]),  
   .WCLK(WCLK_c),  
   .WCLKE(WCLKE_c),  
   .WDATA(WDATA_c[9:0]),  
   .WE(WE_c)  
);

defparam ram1024x4_inst.INIT_0 = 256'h0000000000000000000000000000000000000000000000000000000000000000;
defparam ram1024x4_inst.INIT_1 = 256'h0000000000000000000000000000000000000000000000000000000000000000;
defparam ram1024x4_inst.INIT_2 = 256'h0000000000000000000000000000000000000000000000000000000000000000;
defparam ram1024x4_inst.INIT_3 = 256'h0000000000000000000000000000000000000000000000000000000000000000;
defparam ram1024x4_inst.INIT_4 = 256'h0000000000000000000000000000000000000000000000000000000000000000;
```

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defparam ram1024x4_inst.INIT_5 =
256'h0000000000000000000000000000000000000000000000000000000000000000;
defparam ram1024x4_inst.INIT_6 =
256'h0000000000000000000000000000000000000000000000000000000000000000;
defparam ram1024x4_inst.INIT_7 =
256'h0000000000000000000000000000000000000000000000000000000000000000;
defparam ram1024x4_inst.INIT_8 =
256'h0000000000000000000000000000000000000000000000000000000000000000;
defparam ram1024x4_inst.INIT_9 =
256'h0000000000000000000000000000000000000000000000000000000000000000;
defparam ram1024x4_inst.INIT_A =
256'h0000000000000000000000000000000000000000000000000000000000000000;
defparam ram1024x4_inst.INIT_B =
256'h0000000000000000000000000000000000000000000000000000000000000000;
defparam ram1024x4_inst.INIT_C =
256'h0000000000000000000000000000000000000000000000000000000000000000;
defparam ram1024x4_inst.INIT_D =
256'h0000000000000000000000000000000000000000000000000000000000000000;
defparam ram1024x4_inst.INIT_E =
256'h0000000000000000000000000000000000000000000000000000000000000000;
defparam ram1024x4_inst.INIT_F =
256'h0000000000000000000000000000000000000000000000000000000000000000;

VHDL Instantiation:

Ram1024x4_inst: SB_RAM1024x4
generic map (
  INIT_0 =>
    x"0000000000000000000000000000000000000000000000000000000000000000",
  INIT_1 =>
    x"0000000000000000000000000000000000000000000000000000000000000000",
  INIT_2 =>
    x"0000000000000000000000000000000000000000000000000000000000000000",
  INIT_3 =>
    x"0000000000000000000000000000000000000000000000000000000000000000",
  INIT_4 =>
    x"0000000000000000000000000000000000000000000000000000000000000000",
  INIT_5 =>
    x"0000000000000000000000000000000000000000000000000000000000000000",
  INIT_6 =>
    x"0000000000000000000000000000000000000000000000000000000000000000",
  INIT_7 =>
    x"0000000000000000000000000000000000000000000000000000000000000000",
  INIT_8 =>
    x"0000000000000000000000000000000000000000000000000000000000000000",
  INIT_9 =>
    x"0000000000000000000000000000000000000000000000000000000000000000",
  INIT_A =>
    x"0000000000000000000000000000000000000000000000000000000000000000",
  INIT_B =>
    x"0000000000000000000000000000000000000000000000000000000000000000",
  INIT_C =>
    x"0000000000000000000000000000000000000000000000000000000000000000",
  INIT_D =>
    x"0000000000000000000000000000000000000000000000000000000000000000",
  INIT_E =>
    x"0000000000000000000000000000000000000000000000000000000000000000",
  INIT_F =>
    x"0000000000000000000000000000000000000000000000000000000000000000"
)  
port map (  
  RDATA => RDATA_c,
  RADDR => RADDR_c,
  RCLK => RCLK_c,
RCLKE => RCLKE_c,  
RE => RE_c,  
WADDR => WADDR_c,  
WCLK => WCLK_c,  
WCLKE => WCLKE_c,  
WDATA => WDATA_c,  
WE => WE_c  
);

SB_RAM1024x4NR

SB_RAM1024x4NR // Negative edged Read Clock – i.e. RCLKN  
(RDATA, RCLKN, RCLKE, RE, RADDR, WCLK, WCLKE, WE, WADDR, MASK, WDATA);

Verilog Instantiation:

SB_RAM1024x4NR ram1024x4nr_inst (  
   .RDATA(RDATA_c[3:0]),  
   .RADDR(RADDR_c[9:0]),  
   .RCLKN(RCLKN_c),  
   .RCLKE(RCLKE_c),  
   .RE(RE_c),  
   .WADDR(WADDR_c[3:0]),  
   .WCLK(wCLK_c),  
   .WCLKE(WCLKE_c),  
   .WDATA(WDATA_c[9:0]),  
   .WE(WE_c)  
);

defparam ram1024x4nr_inst.INIT_0 =  
256'h0000000000000000000000000000000000000000000000000000000000000000;

defparam ram1024x4nr_inst.INIT_1 =  
256'h0000000000000000000000000000000000000000000000000000000000000000;

defparam ram1024x4nr_inst.INIT_2 =  
256'h0000000000000000000000000000000000000000000000000000000000000000;

defparam ram1024x4nr_inst.INIT_3 =  
256'h0000000000000000000000000000000000000000000000000000000000000000;

defparam ram1024x4nr_inst.INIT_4 =  
256'h0000000000000000000000000000000000000000000000000000000000000000;

defparam ram1024x4nr_inst.INIT_5 =  
256'h0000000000000000000000000000000000000000000000000000000000000000;

defparam ram1024x4nr_inst.INIT_6 =  
256'h0000000000000000000000000000000000000000000000000000000000000000;

defparam ram1024x4nr_inst.INIT_7 =  
256'h0000000000000000000000000000000000000000000000000000000000000000;

defparam ram1024x4nr_inst.INIT_8 =  
256'h0000000000000000000000000000000000000000000000000000000000000000;

defparam ram1024x4nr_inst.INIT_9 =  
256'h0000000000000000000000000000000000000000000000000000000000000000;

defparam ram1024x4nr_inst.INIT_A =  
256'h0000000000000000000000000000000000000000000000000000000000000000;

defparam ram1024x4nr_inst.INIT_B =  
256'h0000000000000000000000000000000000000000000000000000000000000000;

defparam ram1024x4nr_inst.INIT_C =  
256'h0000000000000000000000000000000000000000000000000000000000000000;

defparam ram1024x4nr_inst.INIT_D =  
256'h0000000000000000000000000000000000000000000000000000000000000000;

defparam ram1024x4nr_inst.INIT_E =  
256'h0000000000000000000000000000000000000000000000000000000000000000;

defparam ram1024x4nr_inst.INIT_F =  
256'h0000000000000000000000000000000000000000000000000000000000000000;
VHDL Instantiation:

```vhdl
ram1024x4nr_inst: SB_RAM1024x4NR
  generic map (  
    INIT_0 =>  
      x"0000000000000000000000000000000000000000000000000000000000000000",  
    INIT_1 =>  
      x"0000000000000000000000000000000000000000000000000000000000000000",  
    INIT_2 =>  
      x"0000000000000000000000000000000000000000000000000000000000000000",  
    INIT_3 =>  
      x"0000000000000000000000000000000000000000000000000000000000000000",  
    INIT_4 =>  
      x"0000000000000000000000000000000000000000000000000000000000000000",  
    INIT_5 =>  
      x"0000000000000000000000000000000000000000000000000000000000000000",  
    INIT_6 =>  
      x"0000000000000000000000000000000000000000000000000000000000000000",  
    INIT_7 =>  
      x"0000000000000000000000000000000000000000000000000000000000000000",  
    INIT_8 =>  
      x"0000000000000000000000000000000000000000000000000000000000000000",  
    INIT_9 =>  
      x"0000000000000000000000000000000000000000000000000000000000000000",  
    INIT_A =>  
      x"0000000000000000000000000000000000000000000000000000000000000000",  
    INIT_B =>  
      x"0000000000000000000000000000000000000000000000000000000000000000",  
    INIT_C =>  
      x"0000000000000000000000000000000000000000000000000000000000000000",  
    INIT_D =>  
      x"0000000000000000000000000000000000000000000000000000000000000000",  
    INIT_E =>  
      x"0000000000000000000000000000000000000000000000000000000000000000",  
    INIT_F =>  
      x"0000000000000000000000000000000000000000000000000000000000000000"
  )
  port map (  
    RDATA => RDATA_c,  
    RADDR => RADDR_c,  
    RCLKN => RCLKN_c,  
    RCLK => RCLK_c,  
    RCLKE => RCLKE_c,  
    RE => RE_c,  
    WADDR => WADDR_c,  
    WCLK => WCLK_c,  
    WCLKE => WCLKE_c,  
    WDATA => WDATA_c,  
    WE => WE_c  
  );

SB_RAM1024x4NW

SB_RAM1024x4NW  // Negative edged Write Clock – i.e. WCLKN
(RDATA, RCLK, RCLKE, RE, RADDR, WCLK, WCLKE, WE, WADDR, MASK, WDATA);
```
Verilog Instantiation:

```verilog
SB_RAM1024x4NW  ram1024x4nw_inst (  
    .RDATA(RDATA_c[3:0]),  
    .RADDR(RADDR_c[9:0]),  
    .RCLK(RCLK_c),  
    .RCLKE(RCLKE_c),  
    .RE(RE_c),  
    .WADDR(WADDR_c[3:0]),  
    .WCLKN(WCLKN_c),  
    .WCLKE(WCLKE_c),  
    .WDATA(WDATA_c[9:0]),  
    .WE(WE_c)
);
```

defparam ram1024x4_inst.INIT_0 = 256'h0000000000000000000000000000000000000000000000000000000000000000;
defparam ram1024x4_inst.INIT_1 = 256'h0000000000000000000000000000000000000000000000000000000000000000;
defparam ram1024x4_inst.INIT_2 = 256'h0000000000000000000000000000000000000000000000000000000000000000;
defparam ram1024x4_inst.INIT_3 = 256'h0000000000000000000000000000000000000000000000000000000000000000;
defparam ram1024x4_inst.INIT_4 = 256'h0000000000000000000000000000000000000000000000000000000000000000;
defparam ram1024x4_inst.INIT_5 = 256'h0000000000000000000000000000000000000000000000000000000000000000;
defparam ram1024x4_inst.INIT_6 = 256'h0000000000000000000000000000000000000000000000000000000000000000;
defparam ram1024x4_inst.INIT_7 = 256'h0000000000000000000000000000000000000000000000000000000000000000;
defparam ram1024x4_inst.INIT_8 = 256'h0000000000000000000000000000000000000000000000000000000000000000;
defparam ram1024x4_inst.INIT_9 = 256'h0000000000000000000000000000000000000000000000000000000000000000;
defparam ram1024x4_inst.INIT_A = 256'h0000000000000000000000000000000000000000000000000000000000000000;
defparam ram1024x4_inst.INIT_B = 256'h0000000000000000000000000000000000000000000000000000000000000000;
defparam ram1024x4_inst.INIT_C = 256'h0000000000000000000000000000000000000000000000000000000000000000;
defparam ram1024x4_inst.INIT_D = 256'h0000000000000000000000000000000000000000000000000000000000000000;
defparam ram1024x4_inst.INIT_E = 256'h0000000000000000000000000000000000000000000000000000000000000000;
defparam ram1024x4_inst.INIT_F = 256'h0000000000000000000000000000000000000000000000000000000000000000;

VHDL Instantiation:

```
ram1024x4nw_inst : SB_RAM1024x4NW
generic map (  
    INIT_0 => x"0000000000000000000000000000000000000000000000000000000000000000",  
    INIT_1 => x"0000000000000000000000000000000000000000000000000000000000000000",  
    INIT_2 => x"0000000000000000000000000000000000000000000000000000000000000000",  
    INIT_3 => x"0000000000000000000000000000000000000000000000000000000000000000",  
    INIT_4 => x"0000000000000000000000000000000000000000000000000000000000000000",  
    INIT_5 => x"0000000000000000000000000000000000000000000000000000000000000000",  
    INIT_6 => x"0000000000000000000000000000000000000000000000000000000000000000",  
    INIT_7 => x"0000000000000000000000000000000000000000000000000000000000000000",  
    INIT_8 => x"0000000000000000000000000000000000000000000000000000000000000000",  
    INIT_9 => x"0000000000000000000000000000000000000000000000000000000000000000",  
    INIT_A => x"0000000000000000000000000000000000000000000000000000000000000000",  
    INIT_B => x"0000000000000000000000000000000000000000000000000000000000000000",  
    INIT_C => x"0000000000000000000000000000000000000000000000000000000000000000",  
    INIT_D => x"0000000000000000000000000000000000000000000000000000000000000000",  
    INIT_E => x"0000000000000000000000000000000000000000000000000000000000000000",  
    INIT_F => x"0000000000000000000000000000000000000000000000000000000000000000"
);
```
INIT_5 =>
x"0000000000000000000000000000000000000000000000000000000000000000",
INIT_6 =>
x"0000000000000000000000000000000000000000000000000000000000000000",
INIT_7 =>
x"0000000000000000000000000000000000000000000000000000000000000000",
INIT_8 =>
x"0000000000000000000000000000000000000000000000000000000000000000",
INIT_9 =>
x"0000000000000000000000000000000000000000000000000000000000000000",
INIT_A =>
x"0000000000000000000000000000000000000000000000000000000000000000",
INIT_B =>
x"0000000000000000000000000000000000000000000000000000000000000000",
INIT_C =>
x"0000000000000000000000000000000000000000000000000000000000000000",
INIT_D =>
x"0000000000000000000000000000000000000000000000000000000000000000",
INIT_E =>
x"0000000000000000000000000000000000000000000000000000000000000000",
INIT_F => x"0000000000000000000000000000000000000000000000000000000000000000"
)
port map (
  RDATA => RDATA_c,
  RADDR => RADDR_c,
  RCLK => RCLK_c,
  RCLKE => RCLKE_c,
  RE => RE_c,
  WADDR => WADDR_c,
  WCLKN => WCLKN_c,
  WCLKE => WCLKE_c,
  WDATA => WDATA_c,
  WE => WE_c
);

**SB_RAM1024x4NRNW**

**SB_RAM1024x4NRNW**  // Negative edged Read and Write – i.e. RCLKN WRCLKLN
(RDATA, RCLKN, RCLKE, RE, RADDR, WCLKN, WCLKE, WE, WADDR, MASK, WDATA);

Verilog Instantiation:

SB_RAM1024x4NRNW _ ram1024x4nrnw_inst (  
  .RDATA(RDATA_c[3:0]),
  .RADDR(RADDR_c[9:0]),
  .RCLKN(RCLK_c),
  .RCLKE(RCLKE_c),
  .RE(RE_c),
  .WADDR(WADDR_c[3:0]),
  .WCLKN(WCLKN_c),
  .WCLKE(WCLKE_c),
  .WDATA(WDATA_c[9:0]),
  .WE(WE_c)
);
defparam ram1024x4nrnw_inst.INIT_0 = 256'h0000000000000000000000000000000000000000000000000000000000000000;
defparam ram1024x4nrnw_inst.INIT_1 = 256'h0000000000000000000000000000000000000000000000000000000000000000;
defparam ram1024x4nrnw_inst.INIT_2 = 256'h0000000000000000000000000000000000000000000000000000000000000000;
defparam ram1024x4nrnw_inst.INIT_3 =
256'h0000000000000000000000000000000000000000000000000000000000000000;
defparam ram1024x4nrnw_inst.INIT_4 =
256'h0000000000000000000000000000000000000000000000000000000000000000;
defparam ram1024x4nrnw_inst.INIT_5 =
256'h0000000000000000000000000000000000000000000000000000000000000000;
defparam ram1024x4nrnw_inst.INIT_6 =
256'h0000000000000000000000000000000000000000000000000000000000000000;
defparam ram1024x4nrnw_inst.INIT_7 =
256'h0000000000000000000000000000000000000000000000000000000000000000;
defparam ram1024x4nrnw_inst.INIT_8 =
256'h0000000000000000000000000000000000000000000000000000000000000000;
defparam ram1024x4nrnw_inst.INIT_9 =
256'h0000000000000000000000000000000000000000000000000000000000000000;
defparam ram1024x4nrnw_inst.INIT_A =
256'h0000000000000000000000000000000000000000000000000000000000000000;
defparam ram1024x4nrnw_inst.INIT_B =
256'h0000000000000000000000000000000000000000000000000000000000000000;
defparam ram1024x4nrnw_inst.INIT_C =
256'h0000000000000000000000000000000000000000000000000000000000000000;
defparam ram1024x4nrnw_inst.INIT_D =
256'h0000000000000000000000000000000000000000000000000000000000000000;
defparam ram1024x4nrnw_inst.INIT_E =
256'h0000000000000000000000000000000000000000000000000000000000000000;
defparam ram1024x4nrnw_inst.INIT_F =
256'h0000000000000000000000000000000000000000000000000000000000000000;

VHDL Instantiation:

ram1024x4nrnw_inst : SB_RAM1024x4NRNW
generic map (  
  INIT_0 => X"0000000000000000000000000000000000000000000000000000000000000000",  
  INIT_1 => X"0000000000000000000000000000000000000000000000000000000000000000",  
  INIT_2 => X"0000000000000000000000000000000000000000000000000000000000000000",  
  INIT_3 => X"0000000000000000000000000000000000000000000000000000000000000000",  
  INIT_4 => X"0000000000000000000000000000000000000000000000000000000000000000",  
  INIT_5 => X"0000000000000000000000000000000000000000000000000000000000000000",  
  INIT_6 => X"0000000000000000000000000000000000000000000000000000000000000000",  
  INIT_7 => X"0000000000000000000000000000000000000000000000000000000000000000",  
  INIT_8 => X"0000000000000000000000000000000000000000000000000000000000000000",  
  INIT_9 => X"0000000000000000000000000000000000000000000000000000000000000000",  
  INIT_A => X"0000000000000000000000000000000000000000000000000000000000000000",  
  INIT_B => X"0000000000000000000000000000000000000000000000000000000000000000",  
  INIT_C => X"0000000000000000000000000000000000000000000000000000000000000000",  
  INIT_D => X"0000000000000000000000000000000000000000000000000000000000000000",  
  INIT_E => X"0000000000000000000000000000000000000000000000000000000000000000",  
  INIT_F => X"0000000000000000000000000000000000000000000000000000000000000000"
)
port map (
    RDATA => RDATA_c,
    RADDR => RADDR_c,
    RCLKN => RCLKN_c,
    RCLKE => RCLKE_c,
    RE => RE_c,
    WADDR => WADDR_c,
    WCLKN => WCLKN_c,
    WCLKE => WCLKE_c,
    WDATA => WDATA_c,
    WE => WE_c
);
The following modules are the complete list of SB_RAM2048x2 based primitives

```
SB_RAM2048x2

//Posedge clock RCLK WCLK
(RDATA, RCLK, RCLKE, RE, RADDR, WCLK, WCLKE, WE, WADDR, MASK, WDATA);

Verilog Instantiation:

SB_RAM2048x2   ram2048x2_inst (  
   .RDATA(RDATA_c[2:0]),  
   .RADDR(RADDR_c[10:0]),  
   .RCLK(RCLK_c),  
   .RCLKE(RCLKE_c),  
   .RE(RE_c),  
   .WADDR(WADDR_c[2:0]),  
   .WCLK(WCLK_c),  
   .WCLKE(WCLKE_c),  
   .WDATA(WDATA_c[10:0]),  
   .WE(WE_c)  
);

defparam ram2048x2_inst.INIT_0 = 256'h0000000000000000000000000000000000000000000000000000000000000000;
defparam ram2048x2_inst.INIT_1 = 256'h0000000000000000000000000000000000000000000000000000000000000000;
defparam ram2048x2_inst.INIT_2 = 256'h0000000000000000000000000000000000000000000000000000000000000000;
defparam ram2048x2_inst.INIT_3 = 256'h0000000000000000000000000000000000000000000000000000000000000000;
defparam ram2048x2_inst.INIT_4 = 256'h0000000000000000000000000000000000000000000000000000000000000000;
defparam ram2048x2_inst.INIT_5 = 256'h0000000000000000000000000000000000000000000000000000000000000000;
defparam ram2048x2_inst.INIT_6 = 256'h0000000000000000000000000000000000000000000000000000000000000000;
```

defparam ram2048x2_inst .INIT_7 = 256'h0000000000000000000000000000000000000000000000000000000000000000;
defparam ram2048x2_inst .INIT_8 = 256'h0000000000000000000000000000000000000000000000000000000000000000;
defparam ram2048x2_inst .INIT_9 = 256'h0000000000000000000000000000000000000000000000000000000000000000;
defparam ram2048x2_inst .INIT_A = 256'h0000000000000000000000000000000000000000000000000000000000000000;
defparam ram2048x2_inst .INIT_B = 256'h0000000000000000000000000000000000000000000000000000000000000000;
defparam ram2048x2_inst .INIT_C = 256'h0000000000000000000000000000000000000000000000000000000000000000;
defparam ram2048x2_inst .INIT_D = 256'h0000000000000000000000000000000000000000000000000000000000000000;
defparam ram2048x2_inst .INIT_E = 256'h0000000000000000000000000000000000000000000000000000000000000000;
defparam ram2048x2_inst .INIT_F = 256'h0000000000000000000000000000000000000000000000000000000000000000;

VHDL Instantiation:

Ram2048x2_inst :  SB_RAM2048x2
generic map (  
  INIT_0 =>
    X"0000000000000000000000000000000000000000000000000000000000000000",
  INIT_1 =>
    X"0000000000000000000000000000000000000000000000000000000000000000",
  INIT_2 =>
    X"0000000000000000000000000000000000000000000000000000000000000000",
  INIT_3 =>
    X"0000000000000000000000000000000000000000000000000000000000000000",
  INIT_4 =>
    X"0000000000000000000000000000000000000000000000000000000000000000",
  INIT_5 =>
    X"0000000000000000000000000000000000000000000000000000000000000000",
  INIT_6 =>
    X"0000000000000000000000000000000000000000000000000000000000000000",
  INIT_7 =>
    X"0000000000000000000000000000000000000000000000000000000000000000",
  INIT_8 =>
    X"0000000000000000000000000000000000000000000000000000000000000000",
  INIT_9 =>
    X"0000000000000000000000000000000000000000000000000000000000000000",
  INIT_A =>
    X"0000000000000000000000000000000000000000000000000000000000000000",
  INIT_B =>
    X"0000000000000000000000000000000000000000000000000000000000000000",
  INIT_C =>
    X"0000000000000000000000000000000000000000000000000000000000000000",
  INIT_D =>
    X"0000000000000000000000000000000000000000000000000000000000000000",
  INIT_E =>
    X"0000000000000000000000000000000000000000000000000000000000000000",
  INIT_F => X"0000000000000000000000000000000000000000000000000000000000000000"
)  
port map (  
  RDATA => RDATA_c,  
  RADDR => RADDR_c,  
  RCLK => RCLK_c,  
  RCLKE => RCLKE_c,  
  RE => RE_c,  
  WADDR => WADDR_c,  
  WCLK => WCLK_c,  
  WCLKE => WCLKE_c,  
  WRE => WRE_c,  
  OE => OE_c,  
  E => E_c)

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SB_RAM2048x2NR

SB_RAM2048x2NR // Negative edged Read Clock – i.e. RCLKN
(RDATA, RCLKN, RCLKE, RE, RADDR, WCLK, WCLKE, WE, WADDR, MASK, WDATA);

SB_RAM2048x2NR ram2048x2nr_inst (
  .RDATA(RDATA_c[2:0]),
  .RADDR(RADDR_c[10:0]),
  .RCLKN(RCLKN_c),
  .RCLKE(RCLKE_c),
  .RE(RE_c),
  .WADDR(WADDR_c[2:0]),
  .WCLK(WCLK_c),
  .WCLKE(WCLKE_c),
  .WDATA(WDATA_c[10:0]),
  .WE(WE_c)
);
defparam ram2048x2nr_inst.INIT_0 = 256'h0000000000000000000000000000000000000000000000000000000000000000;
defparam ram2048x2nr_inst.INIT_1 = 256'h0000000000000000000000000000000000000000000000000000000000000000;
defparam ram2048x2nr_inst.INIT_2 = 256'h0000000000000000000000000000000000000000000000000000000000000000;
defparam ram2048x2nr_inst.INIT_3 = 256'h0000000000000000000000000000000000000000000000000000000000000000;
defparam ram2048x2nr_inst.INIT_4 = 256'h0000000000000000000000000000000000000000000000000000000000000000;
defparam ram2048x2nr_inst.INIT_5 = 256'h0000000000000000000000000000000000000000000000000000000000000000;
defparam ram2048x2nr_inst.INIT_6 = 256'h0000000000000000000000000000000000000000000000000000000000000000;
defparam ram2048x2nr_inst.INIT_7 = 256'h0000000000000000000000000000000000000000000000000000000000000000;
defparam ram2048x2nr_inst.INIT_8 = 256'h0000000000000000000000000000000000000000000000000000000000000000;
defparam ram2048x2nr_inst.INIT_9 = 256'h0000000000000000000000000000000000000000000000000000000000000000;
defparam ram2048x2nr_inst.INIT_A = 256'h0000000000000000000000000000000000000000000000000000000000000000;
defparam ram2048x2nr_inst.INIT_B = 256'h0000000000000000000000000000000000000000000000000000000000000000;
defparam ram2048x2nr_inst.INIT_C = 256'h0000000000000000000000000000000000000000000000000000000000000000;
defparam ram2048x2nr_inst.INIT_D = 256'h0000000000000000000000000000000000000000000000000000000000000000;
defparam ram2048x2nr_inst.INIT_E = 256'h0000000000000000000000000000000000000000000000000000000000000000;
defparam ram2048x2nr_inst.INIT_F = 256'h0000000000000000000000000000000000000000000000000000000000000000;

VHDL Instantiation:

ram2048x2nr_inst : SB_RAM2048x2NR
generic map ({}
  INIT_0 => X"0000000000000000000000000000000000000000000000000000000000000000",}
INIT_1 =>
X"0000000000000000000000000000000000000000000000000000000000000000",
INIT_2 =>
X"0000000000000000000000000000000000000000000000000000000000000000",
INIT_3 =>
X"0000000000000000000000000000000000000000000000000000000000000000",
INIT_4 =>
X"0000000000000000000000000000000000000000000000000000000000000000",
INIT_5 =>
X"0000000000000000000000000000000000000000000000000000000000000000",
INIT_6 =>
X"0000000000000000000000000000000000000000000000000000000000000000",
INIT_7 =>
X"0000000000000000000000000000000000000000000000000000000000000000",
INIT_8 =>
X"0000000000000000000000000000000000000000000000000000000000000000",
INIT_9 =>
X"0000000000000000000000000000000000000000000000000000000000000000",
INIT_A =>
X"0000000000000000000000000000000000000000000000000000000000000000",
INIT_B =>
X"0000000000000000000000000000000000000000000000000000000000000000",
INIT_C =>
X"0000000000000000000000000000000000000000000000000000000000000000",
INIT_D =>
X"0000000000000000000000000000000000000000000000000000000000000000",
INIT_E =>
X"0000000000000000000000000000000000000000000000000000000000000000",
INIT_F => X"0000000000000000000000000000000000000000000000000000000000000000"

port map (
RDATA => RDATA_c,
RADDR => RADDR_c,
RCLK => RCLK_c,
RCLKE => RCLKE_c,
RE => RE_c,
WADDR => WADDR_c,
WCLK => WCLK_c,
WCLKE => WCLKE_c,
WDATA => WDATA_c,
WE => WE_c
);

SB_RAM2048x2NW

SB_RAM2048x2NW // Negative edged Write Clock – i.e. WCLKN
(RDATA, RCLK, RCLKE, RE, RADDR, WCLKN, WCLKE, WE, WADDR, MASK, WDATA);

SB_RAM2048x2NW ram2048x2nw_inst (  
.RDATA(RDATA_c[2:0]),
.RADDR(RADDR_c[10:0]),
.RCLK(RCLKE_c),
.RCLKE(RCLKE_c),
.RE(RE_c),
.WADDR(WADDR_c[2:0]),
.WCLKN(WCLKN_c),
.WCLKE(WCLKE_c),
.WDATA(WDATA_c[10:0]),
.WE(WE_c)
);
defparam ram2048x2nw_inst.INIT_0 = 256'h0000000000000000000000000000000000000000000000000000000000000000;
defparam ram2048x2nw_inst .INIT_0 =
256'h0000000000000000000000000000000000000000000000000000000000000000;
defparam ram2048x2nw_inst .INIT_1 =
256'h0000000000000000000000000000000000000000000000000000000000000000;
defparam ram2048x2nw_inst .INIT_2 =
256'h0000000000000000000000000000000000000000000000000000000000000000;
defparam ram2048x2nw_inst .INIT_3 =
256'h0000000000000000000000000000000000000000000000000000000000000000;
defparam ram2048x2nw_inst .INIT_4 =
256'h0000000000000000000000000000000000000000000000000000000000000000;
defparam ram2048x2nw_inst .INIT_5 =
256'h0000000000000000000000000000000000000000000000000000000000000000;
defparam ram2048x2nw_inst .INIT_6 =
256'h0000000000000000000000000000000000000000000000000000000000000000;
defparam ram2048x2nw_inst .INIT_7 =
256'h0000000000000000000000000000000000000000000000000000000000000000;
defparam ram2048x2nw_inst .INIT_8 =
256'h0000000000000000000000000000000000000000000000000000000000000000;
defparam ram2048x2nw_inst .INIT_9 =
256'h0000000000000000000000000000000000000000000000000000000000000000;
defparam ram2048x2nw_inst .INIT_A =
256'h0000000000000000000000000000000000000000000000000000000000000000;
defparam ram2048x2nw_inst .INIT_B =
256'h0000000000000000000000000000000000000000000000000000000000000000;
defparam ram2048x2nw_inst .INIT_C =
256'h0000000000000000000000000000000000000000000000000000000000000000;
defparam ram2048x2nw_inst .INIT_D =
256'h0000000000000000000000000000000000000000000000000000000000000000;
defparam ram2048x2nw_inst .INIT_E =
256'h0000000000000000000000000000000000000000000000000000000000000000;
defparam ram2048x2nw_inst .INIT_F =
256'h0000000000000000000000000000000000000000000000000000000000000000;

VHDL Instantiation:

ram2048x2nw_inst: SB_RAM2048x2NW
generic map ("
  INIT_0 =>
  x"0000000000000000000000000000000000000000000000000000000000000000",
  INIT_1 =>
  x"0000000000000000000000000000000000000000000000000000000000000000",
  INIT_2 =>
  x"0000000000000000000000000000000000000000000000000000000000000000",
  INIT_3 =>
  x"0000000000000000000000000000000000000000000000000000000000000000",
  INIT_4 =>
  x"0000000000000000000000000000000000000000000000000000000000000000",
  INIT_5 =>
  x"0000000000000000000000000000000000000000000000000000000000000000",
  INIT_6 =>
  x"0000000000000000000000000000000000000000000000000000000000000000",
  INIT_7 =>
  x"0000000000000000000000000000000000000000000000000000000000000000",
  INIT_8 =>
  x"0000000000000000000000000000000000000000000000000000000000000000",
  INIT_9 =>
  x"0000000000000000000000000000000000000000000000000000000000000000",
  INIT_A =>
  x"0000000000000000000000000000000000000000000000000000000000000000",
  INIT_B =>
  x"0000000000000000000000000000000000000000000000000000000000000000",
  INIT_C =>
  x"0000000000000000000000000000000000000000000000000000000000000000",
  INIT_D =>
  x"0000000000000000000000000000000000000000000000000000000000000000";"
INIT_E => \x"0000000000000000000000000000000000000000000000000000000000000000",
INIT_F => \x"0000000000000000000000000000000000000000000000000000000000000000"
port map (    RDATA => RDATA_c,
    RADDR => RADDR_c,
    RCLK => RCLK_c,
    RCLKE => RCLKE_c,
    RE => RE_c,
    WADDR => WADDR_c,
    WCLK => WCLK_c,
    WCLKE => WCLKE_c,
    WDATA => WDATA_c,
    WE => WE_c
);

SB_RAM2048x2NRNW

SB_RAM2048x2NRNW // Negative edged Read and Write – i.e. RCLKN WRCKLN
(RDATA, RCLKN, RCLKE, RE, RADDR, WCLKN, WCLKE, WE, WADDR, MASK, WDATA);

SB_RAM2048x2NRNW ram2048x2nrrnw_inst (    .RDATA(RDATA_c[2:0]),
    .RADDR(RADDR_c[10:0]),
    .RCLKN(RCLKN_c),
    .RCLKE(RCLKE_c),
    .RE(RE_c),
    .WADDR(WADDR_c[2:0]),
    .WCLKN(WCLKN_c),
    .WCLKE(WCLKE_c),
    .WDATA(WDATA_c[10:0]),
    .WE(WE_c)
);
defparam ram2048x2nrrnw_inst.INIT_0 = 256'h0000000000000000000000000000000000000000000000000000000000000000;
defparam ram2048x2nrrnw_inst.INIT_1 = 256'h0000000000000000000000000000000000000000000000000000000000000000;
defparam ram2048x2nrrnw_inst.INIT_2 = 256'h0000000000000000000000000000000000000000000000000000000000000000;
defparam ram2048x2nrrnw_inst.INIT_3 = 256'h0000000000000000000000000000000000000000000000000000000000000000;
defparam ram2048x2nrrnw_inst.INIT_4 = 256'h0000000000000000000000000000000000000000000000000000000000000000;
defparam ram2048x2nrrnw_inst.INIT_5 = 256'h0000000000000000000000000000000000000000000000000000000000000000;
defparam ram2048x2nrrnw_inst.INIT_6 = 256'h0000000000000000000000000000000000000000000000000000000000000000;
defparam ram2048x2nrrnw_inst.INIT_7 = 256'h0000000000000000000000000000000000000000000000000000000000000000;
defparam ram2048x2nrrnw_inst.INIT_8 = 256'h0000000000000000000000000000000000000000000000000000000000000000;
defparam ram2048x2nrrnw_inst.INIT_9 = 256'h0000000000000000000000000000000000000000000000000000000000000000;
defparam ram2048x2nrrnw_inst.INIT_A = 256'h0000000000000000000000000000000000000000000000000000000000000000;
defparam ram2048x2nrrnw_inst.INIT_B = 256'h0000000000000000000000000000000000000000000000000000000000000000;
defparam ram2048x2nrrnw_inst.INIT_C = 256'h0000000000000000000000000000000000000000000000000000000000000000;
defparam ram2048x2nrnw_inst .INIT_D = 256'h0000000000000000000000000000000000000000000000000000000000000000;
defparam ram2048x2nrnw_inst .INIT_E = 256'h0000000000000000000000000000000000000000000000000000000000000000;
defparam ram2048x2nrnw_inst .INIT_F = 256'h0000000000000000000000000000000000000000000000000000000000000000;

VHDL Instantiation:

ram2048x2nrnw_inst : SB_RAM2048x2NRNW
generic map (
    INIT_0 => X"0000000000000000000000000000000000000000000000000000000000000000",
    INIT_1 => X"0000000000000000000000000000000000000000000000000000000000000000",
    INIT_2 => X"0000000000000000000000000000000000000000000000000000000000000000",
    INIT_3 => X"0000000000000000000000000000000000000000000000000000000000000000",
    INIT_4 => X"0000000000000000000000000000000000000000000000000000000000000000",
    INIT_5 => X"0000000000000000000000000000000000000000000000000000000000000000",
    INIT_6 => X"0000000000000000000000000000000000000000000000000000000000000000",
    INIT_7 => X"0000000000000000000000000000000000000000000000000000000000000000",
    INIT_8 => X"0000000000000000000000000000000000000000000000000000000000000000",
    INIT_9 => X"0000000000000000000000000000000000000000000000000000000000000000",
    INIT_A => X"0000000000000000000000000000000000000000000000000000000000000000",
    INIT_B => X"0000000000000000000000000000000000000000000000000000000000000000",
    INIT_C => X"0000000000000000000000000000000000000000000000000000000000000000",
    INIT_D => X"0000000000000000000000000000000000000000000000000000000000000000",
    INIT_E => X"0000000000000000000000000000000000000000000000000000000000000000",
    INIT_F => X"0000000000000000000000000000000000000000000000000000000000000000"
)
port map (  RDATAC => RDATA_c,
    RADDR => RADDR_c,
    RCLKN => RCLKN_c,
    RCLKE => RCLKE_c,
    RE => RE_c,
    WADDR => WADDR_c,
    WCLKN => WCLKN_c,
    WCLKE => WCLKE_c,
    WDATA => WDATA_c,
    WE => WE_c
);
**SB_RAM40_4K**

SB_RAM40_4K is the basic physical RAM primitive which can be instantiated and configured to different depth and dataports. The SB_RAM40_4K block has a size of 4K bits with separate write and read ports, each with independent control signals. By default, input and output data is 16 bits wide, although the data width is configurable using the READ_MODE and WRITE_MODE parameters. The data contents of the SB_RAM40_4K block are optionally pre-loaded during ICE device configuration.

**SB_RAM40_4K Naming Convention Rules**

<table>
<thead>
<tr>
<th>RAM Primitive Name</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>SB_RAM40_4K</td>
<td>Posedge Read clock, Posedge Write clock</td>
</tr>
<tr>
<td>SB_RAM40_4KNR</td>
<td>Negedge Read clock, Posedge Write clock</td>
</tr>
<tr>
<td>SB_RAM40_4KNW</td>
<td>Posedge Read clock, Negedge Write clock</td>
</tr>
<tr>
<td>SB_RAM40_4KNRNW</td>
<td>Negedge Read clock, Negedge Write clock</td>
</tr>
</tbody>
</table>

The following table lists the signals for both ports.

<table>
<thead>
<tr>
<th>Signal Name</th>
<th>Direction</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>WDATA[15:0]</td>
<td>Input</td>
<td>Write Data input</td>
</tr>
<tr>
<td>MASK[15:0]</td>
<td>Input</td>
<td>Bit-line Write Enable input, active low. Applicable only when WRITE_MODE parameter is set to 0.</td>
</tr>
<tr>
<td>WADDR[7:0]</td>
<td>Input</td>
<td>Write Address input. Selects up to 256 possible locations</td>
</tr>
<tr>
<td>WE</td>
<td>Input</td>
<td>Write Enable input, active high</td>
</tr>
<tr>
<td>WCLK</td>
<td>Input</td>
<td>Write Clock input, rising-edge active</td>
</tr>
<tr>
<td>WCLKE</td>
<td>Input</td>
<td>Write Clock Enable input</td>
</tr>
<tr>
<td>RDATA[15:0]</td>
<td>Output</td>
<td>Read Data output</td>
</tr>
<tr>
<td>RADDR[7:0]</td>
<td>Input</td>
<td>Read Address input. Selects one of 256 possible locations</td>
</tr>
<tr>
<td>RE</td>
<td>Input</td>
<td>Read Enable input, active high</td>
</tr>
<tr>
<td>RCLK</td>
<td>Input</td>
<td>Read Clock input, rising-edge active</td>
</tr>
<tr>
<td>RCLKE</td>
<td>Input</td>
<td>Read Clock Enable input</td>
</tr>
<tr>
<td>Parameter Name</td>
<td>Description</td>
<td>Parameter Value</td>
</tr>
<tr>
<td>----------------</td>
<td>-------------</td>
<td>-----------------</td>
</tr>
<tr>
<td>INIT_0, ..., INIT_F</td>
<td>RAM Initialization Data. Passed using 16 parameter strings, each comprising 256 bits. (16x256=4096 total bits)</td>
<td>INIT_0 to INIT_F</td>
</tr>
<tr>
<td>WRITE_MODE</td>
<td>Sets the RAM block write port configuration</td>
<td>0</td>
</tr>
<tr>
<td></td>
<td></td>
<td>1</td>
</tr>
<tr>
<td></td>
<td></td>
<td>2</td>
</tr>
<tr>
<td></td>
<td></td>
<td>3</td>
</tr>
<tr>
<td>READ_MODE</td>
<td>Sets the RAM block read port configuration</td>
<td>0</td>
</tr>
<tr>
<td></td>
<td></td>
<td>1</td>
</tr>
<tr>
<td></td>
<td></td>
<td>2</td>
</tr>
<tr>
<td></td>
<td></td>
<td>3</td>
</tr>
</tbody>
</table>

**SB_RAM40_4K**

Verilog Instantiation:

```
// Physical RAM Instance without Pre Initialization

SB_RAM40_4K ram40_4kinst_physical (  
  .RDATA(RDATA),  
  .RADDR(RADDR),  
  .WADDR(WADDR),  
  .MASK(MASK),  
  .WDATA(WDATA),  
  .RCLKE(RCLKE),  
  .RCLK(RCLK),  
  .RE(RE),  
  .WCLKE(WCLKE),  
  .WCLK(wCLK),  
  .WE(WE)
);

defparam ram40_4kinst_physical.READ_MODE=0;
defparam ram40_4kinst_physical.WRITE_MODE=0;
```

VHDL Instantiation:

```
-- Physical RAM Instance without Pre Initialization

ram40_4kinst_physical : SB_RAM40_4K
  generic map (  
    READ_MODE => 0,  
    WRITE_MODE=>0 )
  port map (  
    RDATA=>RDATA,  
    RADDR=>RADDR,  
    WADDR=>WADDR,  
    MASK=>MASK,  
    WDATA=>WDATA,  
    RCLKE=>RCLKE,  
    RCLK=>RCLK,  
    RE=>RE,  
    WCLKE=>WCLKE,  
    WCLK=>wCLK,  
    WE=>WE  
  );
```
**SB_RAM40_4KNR**

Verilog Instantiation:

```verilog
// Physical RAM Instance without Pre Initialization
SB_RAM40_4KNR ram40_4knrivphys (  
 .RDATA(RDATA),  
 .RADDR(RADDR),  
 .WADDR(WADDR),  
 .MASK(MASK),  
 .WDATA(WDATA),  
 .RCLKE(RCLKE),  
 .RCLKN(RCLKN),  
 .RE(RE),  
 .WCLKE(WCLKE),  
 .WCLK(WCLK),  
 .WE(WE)
);
defparam ram40_4knrivphys.READ_MODE=0;
defparam ram40_4knrivphys.WRITE_MODE=0;
```

VHDL Instantiation:

```vhdl
-- Physical RAM Instance without Pre Initialization
ram40_4knrivphys : SB_RAM40_4KNR
generic map (  
 READ_MODE => 0,  
 WRITE_MODE => 0
)
port map (  
 RDATA=>RDATA,  
 RADDR=>RADDR,  
 WADDR=>WADDR,  
 MASK=>MASK,  
 WDATA=>WDATA,  
 RCLKE=>RCLKE,  
 RCLKN=>RCLKN,  
 RE=>RE,  
 WCLKE=>WCLKE,  
 WCLK=>WCLK,  
 WE=>WE
);
```
SB_RAM40_4KNW

Verilog Instantiation:

// Physical RAM Instance without Pre Initialization

SB_RAM40_4KNW ram40_4knwinst_physical (  
  .RDATA(RDATA),  
  .RADDR(RADDR),  
  .WADDR(WADDR),  
  .MASK(MASK),  
  .WDATA(WDATA),  
  .RCLKE(RCLKE),  
  .RCLK(RCLK),  
  .RE(RE),  
  .WCLKE(WCLKE),  
  .WCLKN(WCLKN),  
  .WE(WE)
);

defparam ram40_4knwinst_physical.READ_MODE=0;
defparam ram40_4knwinst_physical.WRITE_MODE=0;

VHDL Instantiation:

-- Physical RAM Instance without Pre Initialization

ram40_4knwinst_physical : SB_RAM40_4KNW
  generic map (  
    READ_MODE => 0,  
    WRITE_MODE= >0
  )
  port map (  
    RDATA=>RDATA,  
    RADDR=>RADDR,  
    WADDR=>WADDR,  
    MASK=>MASK,  
    WDATA=>WDATA,  
    RCLKE=>RCLKE,  
    RCLK=>RCLK,  
    RE=>RE,  
    WCLKE=>WCLKE,  
    WCLKN=>WCLKN,  
    WE=>WE
  );
SB_RAM40_4KNRNW

Verilog Instantiation:

// Physical RAM Instance without Pre Initialization

SB_RAM40_4KNRNW ram40_4knrnwinst_physical (  
  .RDATA(RDATA),  
  .RADDR(RADDR),  
  .WADDR(WADDR),  
  .MASK(MASK),  
  .RCLKE(RCLKE),  
  .RCLKN(RCLKN),  
  .RE(RE),  
  .WCLKE(WCLKE),  
  .WCLKN(WCLKN),  
  .WE(WE)  
);

defparam ram40_4knrnwinst_physical.READ_MODE=0;
defparam ram40_4knrnwinst_physical.WRITE_MODE=0;

VHDL Instantiation:

-- Physical RAM Instance without Pre Initialization

ram40_4knrnwinst_physical : SB_RAM40_4KNRNW  
generic map (  
  READ_MODE => 0,  
  WRITE_MODE => 0  
);  
port map (  
  RDATA=>RDATA,  
  RADDR=>RADDR,  
  WADDR=>WADDR,  
  MASK=>MASK,  
  WDATA=>WDATA,  
  RCLKE=>RCLKE,  
  RCLKN=>RCLKN,  
  RE=>RE,  
  WCLKE=>WCLKE,  
  WCLKN=>WCLKN,  
  WE=>WE  
);
IO Primitives

**SB_IO**
The SB_IO block contains five registers. The following figure and Verilog template illustrate the complete user accessible logic diagram, and its Verilog instantiation.

![IO Primitives Diagram](image)

**Default Signal Values**
The iCEcube2 software assigns the logic '0' value to all unconnected input ports except for CLOCK_ENABLE.

Note that explicitly connecting a logic '1' value to port CLOCK_ENABLE will result in a non-optimal implementation, since an extra LUT will be used to generate the Logic '1'. If the user's intention is to keep the Input and Output registers always enabled, it is recommended that port CLOCK_ENABLE be left unconnected.
Input and Output Pin Function Tables

Input and Output functions are independently selectable via PIN_TYPE [1:0] and PIN_TYPE [5:2] parameter settings respectively. Specific IO functions are defined by the combination of both attributes. This means that the complete number of combinations is 64, although some combinations are not valid and not defined below. Note that the selection of IO Standards such as SSTL and LVCMOS are not defined by these tables.

### Input Pin Function Table

<table>
<thead>
<tr>
<th>#</th>
<th>Pin Function Mnemonic</th>
<th>PIN_TYPE[1:0]</th>
<th>Functional Description of Package Pin Input Operation</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>PIN_INPUT</td>
<td>0 1</td>
<td>Simple input pin (D_IN_0)</td>
</tr>
<tr>
<td>2</td>
<td>PIN_INPUT_LATCH</td>
<td>1 1</td>
<td>Disables internal data changes on the physical input pin by latching the value.</td>
</tr>
<tr>
<td>3</td>
<td>PIN_INPUT_REGISTERED</td>
<td>0 0</td>
<td>Input data is registered in input cell</td>
</tr>
<tr>
<td>4</td>
<td>PIN_INPUT_REGISTERED _LATCH</td>
<td>1 0</td>
<td>Disables internal data changes on the physical input pin by latching the value on the input register</td>
</tr>
<tr>
<td>5</td>
<td>PIN_INPUT_DDR</td>
<td>0 0</td>
<td>Input 'DDR' data is clocked out on rising and falling clock edges. Use the D_IN_0 and D_IN_1 pins for DDR operation.</td>
</tr>
</tbody>
</table>

### Output Pin Function Table

<table>
<thead>
<tr>
<th>#</th>
<th>Pin Function Mnemonic</th>
<th>PIN_TYPE[5:2]</th>
<th>Functional Description of Package Pin Output Operation</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>PIN_NO_OUTPUT</td>
<td>0 0 0 0</td>
<td>Disables the output function</td>
</tr>
<tr>
<td>2</td>
<td>PIN_OUTPUT</td>
<td>0 1 1 0</td>
<td>Simple output pin, (no enable)</td>
</tr>
<tr>
<td>3</td>
<td>PIN_OUTPUT_TRISTATE</td>
<td>1 0 1 0</td>
<td>The output pin may be tristated using the enable</td>
</tr>
<tr>
<td>4</td>
<td>PIN_OUTPUT_ENABLE_REGISTERED</td>
<td>1 1 1 0</td>
<td>The output pin may be tristated using a registered enable signal</td>
</tr>
<tr>
<td>5</td>
<td>PIN_OUTPUT_REGISTERED</td>
<td>0 1 0 1</td>
<td>Output registered, (no enable)</td>
</tr>
<tr>
<td>6</td>
<td>PIN_OUTPUT_REGISTERED_ENABLE</td>
<td>1 0 0 1</td>
<td>Output registered with enable (enable is not registered)</td>
</tr>
<tr>
<td>7</td>
<td>PIN_OUTPUT_REGISTERED_ENABLE _REGISTERED</td>
<td>1 1 0 1</td>
<td>Output registered and enable registered</td>
</tr>
<tr>
<td>8</td>
<td>PIN_OUTPUT_DDR</td>
<td>0 1 0 0</td>
<td>Output 'DDR' data is clocked out on rising and falling clock edges</td>
</tr>
<tr>
<td>9</td>
<td>PIN_OUTPUT_DDR_ENABLE</td>
<td>1 0 0 0</td>
<td>Output data is clocked out on rising and falling clock edges</td>
</tr>
<tr>
<td>10</td>
<td>PIN_OUTPUT_DDR_ENABLE_REGISTERED</td>
<td>1 1 0 0</td>
<td>Output 'DDR' data with registered enable signal</td>
</tr>
<tr>
<td>11</td>
<td>PIN_OUTPUT_REGISTERED_INVERTED</td>
<td>0 1 1 1</td>
<td>Output registered signal is inverted</td>
</tr>
<tr>
<td>12</td>
<td>PIN_OUTPUT_REGISTERED_ENABLE _INVERTED</td>
<td>1 0 1 1</td>
<td>Output signal is registered and inverted, (no enable function)</td>
</tr>
<tr>
<td>13</td>
<td>PIN_OUTPUT_REGISTERED_ENABLE _REGISTERED_INVERTED</td>
<td>1 1 1 1</td>
<td>Output signal is registered and inverted, the enable/tristate control is registered.</td>
</tr>
</tbody>
</table>
Syntax Verilog Use

Output Pin Function is the bit vector associated with PIN_TYPE [5:2] and Input Pin Function is the bit vector associated with PIN_TYPE [1:0], resulting in a 6 bit value PIN_TYPE [5:0]

```
defparam my_generic_IO.PIN_TYPE = 6'b(Output Pin Function, Input Pin Function);
```

DDR IO Configuration

The following setting configures the SB_IO into a DDR IO.

```
defparam my_DDR_IO.PIN_TYPE = 6'b100000;
```

// PIN_TYPE [5:2] = 1000
// PIN_TYPE [1:0] = 00

This creates a DDR IO pin whereby the input data is clocked in on both the rising and falling input clock edges.

The output 'DDR' data is clocked out on rising and falling output clock edges, and the output may be tri-stated, using the output enable port of the SB_IO.

High Drive SB_IO

The iCE40LP1K-SWG16TR and iCE40LP640-SWG16TR device SB_IO’s can be configured with different drive strengths to increase the IO output current. To configure an SB_IO with specific drive value, the user needs specify the "DRIVE_STRENGTH" synthesis attribute on the SB_IO instance and the IO needs to be configured as output-only registered IO. Refer iCEcube2_userguide for more details.

Synthesis Attribute Syntax:

```
/* synthesis DRIVE_STRENGTH = <Drive value> */
```

**Drive Value:**

<table>
<thead>
<tr>
<th>Drive Strength Value</th>
<th>Description.</th>
</tr>
</thead>
<tbody>
<tr>
<td>x1</td>
<td>Default drive strength. No replication of SB_IO.</td>
</tr>
<tr>
<td>x2</td>
<td>Increase default drive strength by 2. SB_IO replicated once.</td>
</tr>
<tr>
<td>x3</td>
<td>Increase default drive strength by 3. SB_IO replicated twice.</td>
</tr>
</tbody>
</table>

Note: High drive SB_IO is available only in iCE40LP1K-SWG16TR and iCE40640-SWG16TR devices.
Verilog Instantiation

```verilog
SB_IO   IO_PIN_INST
()
  .PACKAGE_PIN (Package_Pin), // User's Pin signal name
  .LATCH_INPUT_VALUE (latch_input_value), // Latches/holds the Input value
  .CLOCK_ENABLE (clock_enable), // Clock Enable common to input and
      // output clock
  .INPUT_CLK (input_clk), // Clock for the input registers
  .OUTPUT_CLK (output_clk), // Clock for the output registers
  .OUTPUT_ENABLE (output_enable), // Output Pin Tristate/Enable
      // control
  .D_OUT_0 (d_out_0), // Data 0 - out to Pin/Rising clk
      // edge
  .D_OUT_1 (d_out_1), // Data 1 - out to Pin/Falling clk
      // edge
  .D_IN_0 (d_in_0), // Data 0 - Pin input/Rising clk
      // edge
  .D_IN_1 (d_in_1) // Data 1 - Pin input/Falling clk
      // edge
) /* synthesis DRIVE_STRENGTH= x2 */;
```

defparam IO_PIN_INST.PIN_TYPE = 6'b000000;
    // See Input and Output Pin Function Tables.
    // Default value of PIN_TYPE = 6'000000 i.e.
    // an input pad, with the input signal
    // registered.

defparam IO_PIN_INST.PULLUP = 1'b0;
    // By default, the IO will have NO pull up.
    // This parameter is used only on bank 0, 1,
    // and 2. Ignored when it is placed at bank 3

defparam IO_PIN_INST.NEG_TRIGGER = 1'b0;
    // Specify the polarity of all FFs in the IO to
    // be falling edge when NEG_TRIGGER = 1.
    // Default is rising edge.

defparam IO_PIN_INST.IO_STANDARD = "SB_LVCMOS";
    // Other IO standards are supported in bank 3
    // only: SB_SSTL2_CLASS_2, SB_SSTL2_CLASS_1,
    // SB_SSTL18_FULL, SB_SSTL18_HALF, SB_MDDR10,
    // SB_MDDR8, SB_MDDR4, SB_MDDR2 etc.
```
Global Buffer Primitives

**SB_GB_IO**

**Default Signal Values**
The ICEcube2 software assigns the logic '0' value to all unconnected input ports except for CLOCK_ENABLE.

Note that explicitly connecting a logic '1' value to port CLOCK_ENABLE will result in a non-optimal implementation, since an extra LUT will be used to generate the Logic '1'. If the user's intention is to keep the Input and Output registers always enabled, it is recommended that port CLOCK_ENABLE be left unconnected.

**Verilog Instantiation**

```verilog
SB_GB_IO My_Clock_Buffer_Package_Pin ( // A users external Clock reference pin
  .PACKAGE_PIN (Package_Pin), // User's Pin signal name
  .LATCH_INPUT_VALUE (latch_input_value), // Latches/holds the Input value
  .CLOCK_ENABLE (clock_enable)  // Clock Enable common to input and
                                // output clock
);                              //
```
INPUT_CLK (input_clk), // Clock for the input registers
OUTPUT_CLK (output_clk), // Clock for the output registers
OUTPUT_ENABLE (output_enable), // Output Pin Tristate/Enable control
D_OUT_0 (d_out_0), // Data 0 – out to Pin/Rising clk edge
D_OUT_1 (d_out_1), // Data 1 – out to Pin/Falling clk edge
D_IN_0 (d_in_0), // Data 0 – Pin input/Rising clk edge
D_IN_1 (d_in_1) // Data 1 – Pin input/Falling clk edge

GLOBAL_BUFFER_OUTPUT (Global_Buffered_User_Clock)
// Example use – clock buffer driven from the input pin
);
defparam My_Clock_Buffer_Package_Pin.PIN_TYPE = 6'b000000;
// See Input and Output Pin Function Tables.
// Default value of PIN_TYPE = 6'000000 i.e.
// an input pad, with the input signal registered
Note that this primitive is a superset of the SB_IO primitive, and includes the connectivity to drive a Global Buffer. For example SB_GB_IO pins are likely to be used for external Clocks.

**SB_GB Primitive**

```
user_signal_to_global_buffer          global_buffer_output
```

**Verilog Instantiation**

SB_GB My_Global_Buffer_i (  //Required for a user's internally generated
  //FPGA signal that is heavily loaded and
  //requires global buffering. For example, a
  //user's logic-generated clock.
.
USER_SIGNAL_TO_GLOBAL_BUFFER (Users_internal_CLK),
GLOBAL_BUFFER_OUTPUT (Global_Buffered_User_Signal)
);


PLL Primitives

The Phase Lock Loop (PLL) function is offered as a feature in certain devices of the iCE65 and iCE40 device family.

It is strongly recommended that the configuration of the PLL primitives be accomplished through the use of the PLL Configuration tool that is offered as part of the iCEcube2 software.

**iCE65 PLL Primitives**

There are 3 primitives that represent the PLL function in the iCEcube2 software viz. SB_PLL_CORE, SB_PLL_PAD, and SB_PLL_2_PAD. A short description of each primitive and its ports/parameters is provided in the following sections.

**SB_PLL_CORE**

The SB_PLL_CORE primitive should be used when the source clock of the PLL is driven by FPGA routing i.e. when the PLL source clock originates on the FPGA or is driven by an input pad that is not in the bottom IO bank (IO Bank 2).

![SB_PLL_CORE Diagram]

**Ports**

- **REFERENCECLK**: PLL source clock that serves as the input to the SB_PLL_CORE primitive.
- **PLLOUTGLOBAL**: Output clock generated by the PLL, drives a global clock network on the FPGA.
- **PLLOUTCORE**: Output clock generated by the PLL, drives regular FPGA routing. The frequency generated on this output is the same as the frequency of the clock signal generated on the PLLOUTGLOBAL port.
- **LOCK**: Output port, when HIGH, indicates that the signal on PLLOUTGLOBAL/PLLOUTCORE is locked to the PLL source on REFERENCECLK.
- **EXTFEEDBACK**: External feedback input to PLL. Enabled when the FEEDBACK_PATH parameter is set to EXTERNAL.
- **DYNAMICDELAY**: 4 bit input bus that enables dynamic control of the delay contributed by the Fine Delay Adjust Block. The Fine Delay Adjust Block is used when there is a need to adjust the phase alignment of...
PLLOUTGLOBAL/PLLOUTCORE with respect to REFERENCECLK. The DYNAMICDELAY port controls are enabled when the DELAY_ADJUSTMENT_MODE parameter is set to DYNAMIC.

RESET: Active low input that asynchronously resets the PLL.

BYPASS: Input signal, when asserted, connects the signal on REFERENCECLK to PLLOUTCORE/PLLOUTGLOBAL pins.

LATCHINPUTVALUE: Active high input, when enabled, forces the PLL into low-power mode. The PLLOUTGLOBAL/PLLOUTCORE pins are held static at their last value. This function is enabled when the parameter ENABLE_ICEGATE is set to ‘1’.

SCLK, SDI, SDO: These pins are used only for internal testing purposes, and need not be instantiated by users.

Parameters
The SB_PLL_CORE primitive requires configuration through the specification of the following parameters. It is strongly recommended that the configuration of the PLL primitives be accomplished through the use of the PLL Configuration tool that is offered as part of the iCEcube2 software.
<table>
<thead>
<tr>
<th>Parameter Name</th>
<th>Description</th>
<th>Parameter Value</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>FEEDBACK_PATH</td>
<td>Selects the feedback path to the PLL</td>
<td>SIMPLE</td>
<td>Feedback is internal to the PLL, directly from VCO</td>
</tr>
<tr>
<td></td>
<td></td>
<td>DELAY</td>
<td>Feedback is internal to the PLL, through the Fine Delay Adjust Block</td>
</tr>
<tr>
<td></td>
<td></td>
<td>PHASE_AND_DELAY</td>
<td>Feedback is internal to the PLL, through the Phase Shifter and the Fine Delay Adjust Block</td>
</tr>
<tr>
<td></td>
<td></td>
<td>EXTERNAL</td>
<td>Feedback path is external to the PLL, and connects to EXTFEEDBACK pin. Also uses the Fine Delay Adjust Block.</td>
</tr>
<tr>
<td>DELAY_ADJUSTMENT_MODE</td>
<td>Selects the mode for the Fine Delay Adjust block</td>
<td>FIXED</td>
<td>Delay of the Fine Delay Adjust Block is fixed, the value is specified by the FIXED_DELAY_ADJUSTMENT parameter setting</td>
</tr>
<tr>
<td></td>
<td></td>
<td>DYNAMIC</td>
<td>Delay of Fine Delay Adjust Block is determined by the signal value at the DYNAMICDELAY[3:0] pins</td>
</tr>
<tr>
<td>FIXED_DELAY_ADJUSTMENT</td>
<td>Sets a constant value for the Fine Delay Adjust Block</td>
<td>0, 1,…,15</td>
<td>The PLLOUTGLOBAL &amp; PLLOUTCORE signals are delay compensated by (n+1)*150 ps, where n = FIXED_DELAY_ADJUSTMENT, only if the setting of the DELAY_ADJUSTMENT_MODE is FIXED.</td>
</tr>
<tr>
<td>PLL_OUT_PHASE</td>
<td>Controls the phase alignment of the PLLOUTCORE &amp; PLLOUTGLOBAL signals relative to REFERENCECLK</td>
<td>NONE</td>
<td>No phase alignment. No duty cycle correction</td>
</tr>
<tr>
<td></td>
<td></td>
<td>0deg</td>
<td>0° phase shift</td>
</tr>
<tr>
<td></td>
<td></td>
<td>90deg</td>
<td>90° phase shift</td>
</tr>
<tr>
<td></td>
<td></td>
<td>180deg</td>
<td>180° phase shift</td>
</tr>
<tr>
<td></td>
<td></td>
<td>270deg</td>
<td>270° phase shift</td>
</tr>
<tr>
<td>DIVR</td>
<td>REFERENCECLK divider</td>
<td>0,1,2,…,15</td>
<td>These parameters are used to control the output frequency, depending on the FEEDBACK_PATH setting.</td>
</tr>
<tr>
<td>DIVF</td>
<td>Feedback divider</td>
<td>0,1,…63</td>
<td></td>
</tr>
<tr>
<td>DIVQ</td>
<td>VCO Divider</td>
<td>0,1,…,7</td>
<td></td>
</tr>
<tr>
<td>FILTER_RANGE</td>
<td>PLL Filter Range</td>
<td>0,1,…,7</td>
<td></td>
</tr>
<tr>
<td>EXTERNAL_DIVIDE_FACTOR</td>
<td>Divide-by factor of a divider in external feedback path</td>
<td>User specified</td>
<td>Specified only when there is a user-implemented divider in the external feedback path.</td>
</tr>
<tr>
<td>ENABLE_ICEGATE</td>
<td>Enables the PLL power-down control</td>
<td>0</td>
<td>Power-down control disabled</td>
</tr>
<tr>
<td></td>
<td></td>
<td>1</td>
<td>Power-down controlled by LATCHINPUTVALUE input</td>
</tr>
</tbody>
</table>
**SB_PLL_PAD**

The SB_PLL_PAD primitive should be used when the source clock of the PLL is driven by an input pad that is located in the bottom IO bank (IO Bank 2), and the source clock is not required inside the FPGA.

### Ports

**PACKAGEPIN:** PLL source clock that serves as the input to the SB_PLL_PAD primitive.

**PLLOUTGLOBAL:** Output clock generated by the PLL, drives a global clock network on the FPGA.

**PLLOUTCORE:** Output clock generated by the PLL, drives regular FPGA routing. The frequency generated on this output is the same as the frequency of the clock signal generated on the PLLOUTGLOBAL port.

**LOCK:** Output port, when HIGH, indicates that the signal on PLLOUTGLOBAL/PLLOUTCORE is locked to the PLL source on PACKAGEPIN.

**EXTFEEDBACK:** External feedback input to PLL. Enabled when the FEEDBACK_PATH parameter is set to EXTERNAL.

**DYNAMICDELAY:** 4 bit input bus that enables dynamic control of the delay contributed by the Fine Delay Adjust Block. The Fine Delay Adjust Block is used when there is a need to adjust the phase alignment of PLLOUTGLOBAL/PLLOUTCORE with respect to REFERENCECLK. The DYNAMICDELAY port controls are enabled when the DELAY_ADJUSTMENT_MODE parameter is set to DYNAMIC.

**RESET:** Active low input that asynchronously resets the PLL.

**BYPASS:** Input signal, when asserted, connects the signal on REFERENCECLK to PLLOUTCORE/PLLOUTGLOBAL pins.

**LATCHINPUTVALUE:** Active high input, when enabled, forces the PLL into low-power mode. The PLLOUTGLOBAL/PLLOUTCORE pins are held static at their last value. This function is enabled when the parameter ENABLE_ICEGATE is set to ‘1’.

**SCLK, SDI, SDO:** These pins are used only for internal testing purposes, and need not be instantiated by users.

### Parameters

The SB_PLL_PAD primitive requires configuration through the specification of the following parameters. It is strongly recommended that the configuration of the PLL primitives be accomplished through the use of the PLL Configuration tool that is offered as part of the iCEcube2 software.
<table>
<thead>
<tr>
<th>Parameter Name</th>
<th>Description</th>
<th>Parameter Value</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>FEEDBACK_PATH</td>
<td>Selects the feedback path to the PLL</td>
<td>SIMPLE</td>
<td>Feedback is internal to the PLL, directly from VCO</td>
</tr>
<tr>
<td></td>
<td></td>
<td>DELAY</td>
<td>Feedback is internal to the PLL, through the Fine Delay Adjust Block</td>
</tr>
<tr>
<td></td>
<td></td>
<td>PHASE_AND_DELAY</td>
<td>Feedback is internal to the PLL, through the Phase Shifter and the Fine Delay Adjust Block</td>
</tr>
<tr>
<td></td>
<td></td>
<td>EXTERNAL</td>
<td>Feedback path is external to the PLL, and connects to EXTFEEDBACK pin. Also uses the Fine Delay Adjust Block</td>
</tr>
<tr>
<td>DELAY_ADJUSTMENT_MODE</td>
<td>Selects the mode for the Fine Delay Adjust block.</td>
<td>FIXED</td>
<td>Delay of the Fine Delay Adjust Block is fixed, the value is specified by the FIXED_DELAY_ADJUSTMENT parameter setting</td>
</tr>
<tr>
<td></td>
<td></td>
<td>DYNAMIC</td>
<td>Delay of Fine Delay Adjust Block is determined by the signal value at the DYNAMICDELAY[3:0] pins</td>
</tr>
<tr>
<td>FIXED_DELAY_ADJUSTMENT</td>
<td>Sets a constant value for the Fine Delay Adjust Block.</td>
<td>0, 1,....,15</td>
<td>The PLLOUTGLOBAL &amp; PLLOUTCORE signals are delay compensated by (n+1)*150 ps, where n = FIXED_DELAY_ADJUSTMENT, only if the setting of the DELAY_ADJUSTMENT_MODE is FIXED.</td>
</tr>
<tr>
<td>PLL_OUT_PHASE</td>
<td>Controls the phase alignment of the PLLOUTCORE &amp; PLLOUTCORE signals relative to REFERENCECLK</td>
<td>NONE</td>
<td>No phase alignment. No duty cycle correction</td>
</tr>
<tr>
<td></td>
<td></td>
<td>0deg</td>
<td>0° phase shift</td>
</tr>
<tr>
<td></td>
<td></td>
<td>90deg</td>
<td>90° phase shift</td>
</tr>
<tr>
<td></td>
<td></td>
<td>180deg</td>
<td>180° phase shift</td>
</tr>
<tr>
<td></td>
<td></td>
<td>270deg</td>
<td>270° phase shift</td>
</tr>
<tr>
<td>DIVR</td>
<td>REFERENCECLK divider</td>
<td>0,1,2,...,15</td>
<td>These parameters are used to control the output frequency, depending on the FEEDBACK_PATH setting.</td>
</tr>
<tr>
<td>DIVF</td>
<td>Feedback divider</td>
<td>0,1,...63</td>
<td></td>
</tr>
<tr>
<td>DIVQ</td>
<td>VCO Divider</td>
<td>0,1,...,7</td>
<td></td>
</tr>
<tr>
<td>FILTER_RANGE</td>
<td>PLL Filter Range</td>
<td>0,1,...,7</td>
<td>Specified only when there is a user-implemented divider in the external feedback path.</td>
</tr>
<tr>
<td>EXTERNAL_DIVIDE_FACTOR</td>
<td>Divide-by factor of a divider in external feedback path</td>
<td>User specified</td>
<td></td>
</tr>
<tr>
<td>ENABLE_ICEGATE</td>
<td>Enables the PLL power-down control</td>
<td>0</td>
<td>Power-down control disabled</td>
</tr>
<tr>
<td></td>
<td></td>
<td>1</td>
<td>Power-down controlled by LATCHINPUTVALUE input</td>
</tr>
</tbody>
</table>
**SB_PLL_2_PAD**

The SB_PLL_2_PAD primitive should be used when the source clock of the PLL is driven by an input pad that is located in the bottom IO bank (IO Bank 2), and in addition to the PLL output, the source clock is also required inside the FPGA.

![SB_PLL_2_PAD Diagram](image)

**Ports**

PACKAGENPIN: PLL source clock that serves as the input to the SB_PLL_PAD primitive.

PLLOUTGLOBALA: The signal on PACKAGENPIN appears on the FPGA at this pin, and drives a global clock network on the FPGA. Do not use this pin in an external feedback path to the PLL.

PLLOUTCOREA: The signal on PACKAGENPIN appears on the FPGA at this pin, which drives regular FPGA routing. Do not use this pin in an external feedback path to the PLL.

PLLOUTGLOBALB: Output clock generated by the PLL, drives a global clock network on the FPGA.

PLLOUTCOREB: Output clock generated by the PLL, drives regular FPGA routing. The frequency generated on this output is the same as the frequency of the clock signal generated on the PLLOUTGLOBAL port.

LOCK: Output port, when HIGH, indicates that the signal on PLLOUTGLOBALB/PLLOUTCOREB is locked to the PLL source on PACKAGENPIN.

EXTFEEDBACK: External feedback input to PLL. Enabled when the FEEDBACK_PATH parameter is set to EXTERNAL.

DYNAMICDELAY: 4 bit input bus that enables dynamic control of the delay contributed by the Fine Delay Adjust Block. The Fine Delay Adjust Block is used when there is a need to adjust the phase alignment of PLLOUTGLOBAL/PLLOUTCORE with respect to REFERENCECLK. The DYNAMICDELAY port controls are enabled when the DELAY_ADJUSTMENT_MODE parameter is set to DYNAMIC.

RESET: Active low input that asynchronously resets the PLL.

BYPASS: Input signal, when asserted, connects the signal on REFERENCECLK to PLLOUTCORE/PLLOUTGLOBAL pins.
**LATCHINPUTVALUE**: Active high input, when enabled, forces the PLL into low-power mode. The PLLOUTGLOBALA/PLLOUTCOREA pins are held static at their last value only when the parameter ENABLE_ICEGATE_PORTA is set to ‘1’, and the LATCHINPUTVALUE signal is asserted. The PLLOUTGLOBALB/PLLOUTCOREB pins are held static at their last value only when the parameter ENABLE_ICEGATE_PORTB is set to ‘1’, and the LATCHINPUTVALUE signal is asserted.

**SCLK, SDI, SDO**: These pins are used only for internal testing purposes, and need not be instantiated by users.

**Parameters**
The SB_PLL_2_PAD primitive requires configuration through the specification of the following parameters. It is strongly recommended that the configuration of the PLL primitives be accomplished through the use of the PLL Configuration tool that is offered as part of the iCEcube2 software.
<table>
<thead>
<tr>
<th>Parameter Name</th>
<th>Description</th>
<th>Parameter Value</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>FEEDBACK_PATH</td>
<td>Selects the feedback path to the PLL</td>
<td>SIMPLE</td>
<td>Feedback is internal to the PLL, directly from VCO</td>
</tr>
<tr>
<td></td>
<td></td>
<td>DELAY</td>
<td>Feedback is internal to the PLL, through the Fine Delay Adjust Block</td>
</tr>
<tr>
<td></td>
<td></td>
<td>PHASE_AND_DELAY</td>
<td>Feedback is internal to the PLL, through the Phase Shifter and the Fine Delay Adjust Block</td>
</tr>
<tr>
<td></td>
<td></td>
<td>EXTERNAL</td>
<td>Feedback path is external to the PLL, and connects to EXTFEEDBACK pin. Also uses the Fine Delay Adjust Block.</td>
</tr>
<tr>
<td>DELAY_ADJUSTMENT_MODE</td>
<td>Selects the mode for the Fine Delay Adjust Block.</td>
<td>FIXED</td>
<td>Delay of the Fine Delay Adjust Block is fixed, the value is specified by the FIXED_DELAY_ADJUSTMENT parameter setting</td>
</tr>
<tr>
<td></td>
<td></td>
<td>DYNAMIC</td>
<td>Delay of Fine Delay Adjust Block is determined by the signal value at the DYNAMIC_DELAY[3:0] pins</td>
</tr>
<tr>
<td>FIXED_DELAY_ADJUSTMENT</td>
<td>Sets a constant value for the Fine Delay Adjust Block.</td>
<td>0, 1,...,15</td>
<td>The PLLOUTGLOBAL &amp; PLLOUTCORE signals are delay compensated by (n+1)*150 ps, where n = FIXED_DELAY_ADJUSTMENT, only if the setting of the DELAY_ADJUSTMENT_MODE is FIXED.</td>
</tr>
<tr>
<td>PLL_OUT_PHASE</td>
<td>Controls the phase alignment of the PLLOUTCORE &amp; PLLOUTGLOBAL signals relative to REFERENCECLK</td>
<td>NONE</td>
<td>No phase alignment. No duty cycle correction</td>
</tr>
<tr>
<td></td>
<td></td>
<td>0deg</td>
<td>0° phase shift</td>
</tr>
<tr>
<td></td>
<td></td>
<td>90deg</td>
<td>90° phase shift</td>
</tr>
<tr>
<td></td>
<td></td>
<td>180deg</td>
<td>180° phase shift</td>
</tr>
<tr>
<td></td>
<td></td>
<td>270deg</td>
<td>270° phase shift</td>
</tr>
<tr>
<td>DIVR</td>
<td>REFERENCECLK divider</td>
<td>0,1,2,...,15</td>
<td>These parameters are used to control the output frequency, depending on the FEEDBACK_PATH setting.</td>
</tr>
<tr>
<td>DIVF</td>
<td>Feedback divider</td>
<td>0,1,...,63</td>
<td></td>
</tr>
<tr>
<td>DIVQ</td>
<td>VCO Divider</td>
<td>0,1,...,7</td>
<td></td>
</tr>
<tr>
<td>FILTER_RANGE</td>
<td>PLL Filter Range</td>
<td>0,1,...,7</td>
<td></td>
</tr>
<tr>
<td>EXTERNAL_DIVIDE_FACTOR</td>
<td>Divide-by factor of a divider in external feedback path</td>
<td>User specified</td>
<td>Specified only when there is a user-implemented divider in the external feedback path.</td>
</tr>
<tr>
<td>ENABLE_ICEGATE_PORTA/</td>
<td>Separate power-down controls for Port A and Port B outputs</td>
<td>0</td>
<td>Power-down control disabled</td>
</tr>
<tr>
<td>ENABLE_ICEGATE_PORTB</td>
<td></td>
<td>1</td>
<td>Power-down controlled by LATCHINPUTVALUE input</td>
</tr>
</tbody>
</table>
ICE40 PLL Primitives

There are 5 primitives that represent the PLL function in the iCEcube2 software viz. SB_PLL40_CORE, SB_PLL40_PAD, SB_PLL40_2_PAD, SB_PLL40_2F_CORE and SB_PLL40_2F_PAD for the ice40 device family. A short description of each primitive and its ports/parameters is provided in the following sections.

It is strongly recommended that the configuration of the PLL primitives be accomplished through the use of the PLL Configuration tool that is offered as part of the iCEcube2 software.

SB_PLL40_CORE

The SB_PLL40_CORE primitive should be used when the source clock of the PLL is driven by FPGA routing i.e. when the PLL source clock originates on the FPGA or is driven by an input pad that is not in the bottom IO bank (IO Bank 2).

![SB_PLL40_CORE diagram](image)

Ports

REFERENCECLK: PLL source clock that serves as the input to the SB_PLL40_CORE primitive.

PLLOUTGLOBAL: Output clock generated by the PLL, drives a global clock network on the FPGA.

PLLOUTCORE: Output clock generated by the PLL, drives regular FPGA routing. The frequency generated on this output is the same as the frequency of the clock signal generated on the PLLOUTGLOBAL port.

LOCK: Output port, when HIGH, indicates that the signal on PLLOUTGLOBAL/PLLOUTCORE is locked to the PLL source on REFERENCECLK.

EXTFEEDBACK: External feedback input to PLL. Enabled when the FEEDBACK_PATH parameter is set to EXTERNAL.

DYNAMICDELAY: 7 bit input bus that enables dynamic control of the delay contributed by the Fine Delay Adjust Block. The Fine Delay Adjust Block is used when there is a need to adjust the phase alignment of PLLOUTGLOBAL/PLLOUTCORE with respect to REFERENCECLK. The DYNAMICDELAY port controls are enabled when the DELAY_ADJUSTMENT_MODE parameter is set to DYNAMIC.

RESETB: Active low input that asynchronously resets the PLL.
**BYPASS:** Input signal, when asserted, connects the signal on REFERENCECLK to PLLOUTCORE/PLLOUTGLOBAL pins.

**LATCHINPUTVALUE:** Active high input, when enabled, forces the PLL into low-power mode. The PLLOUTGLOBAL/PLLOUTCORE pins are held static at their last value. This function is enabled when the parameter ENABLE_ICEGATE is set to ‘1’.

**SCLK, SDI, SDO:** These pins are used only for internal testing purposes, and need not be instantiated by users.

**Parameters**
The SB_PLL40_CORE primitive requires configuration through the specification of the following parameters. It is strongly recommended that the configuration of the PLL primitives be accomplished through the use of the PLL Configuration tool that is offered as part of the iCEcube2 software.
<table>
<thead>
<tr>
<th>Parameter Name</th>
<th>Description</th>
<th>Parameter Value</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>FEEDBACK_PATH</td>
<td>Selects the feedback path to the PLL</td>
<td>SIMPLE</td>
<td>Feedback is internal to the PLL, directly from VCO</td>
</tr>
<tr>
<td></td>
<td></td>
<td>DELAY</td>
<td>Feedback is internal to the PLL, through the Fine Delay Adjust Block</td>
</tr>
<tr>
<td></td>
<td></td>
<td>PHASE_AND_DELAY</td>
<td>Feedback is internal to the PLL, through the Phase Shifter and the Fine Delay Adjust Block</td>
</tr>
<tr>
<td></td>
<td></td>
<td>EXTERNAL</td>
<td>Feedback path is external to the PLL, and connects to EXTFEEDBACK pin. Also uses the Fine Delay Adjust Block.</td>
</tr>
<tr>
<td>DELAY_ADJUSTMENT_MODE_FEEDBACK</td>
<td>Selects the mode for the Fine Delay Adjust block in the feedback path</td>
<td>FIXED</td>
<td>Delay of the Fine Delay Adjust Block is fixed, the value is specified by the FDA_FEEDBACK parameter setting</td>
</tr>
<tr>
<td></td>
<td></td>
<td>DYNAMIC</td>
<td>Delay of Fine Delay Adjust Block is determined by the signal value at the DYNAMICDELAY[3:0] pins</td>
</tr>
<tr>
<td>FDA_FEEDBACK</td>
<td>Sets a constant value for the Fine Delay Adjust Block in the feedback path</td>
<td>0, 1,…,15</td>
<td>The PLLOUTGLOBAL &amp; PLLOUTCORE signals are delay compensated by (n+1)*150 ps, where n = FDA_FEEDBACK only if the setting of the DELAY_ADJUSTMENT_MODE_FEEDBACK is FIXED.</td>
</tr>
<tr>
<td>DELAY_ADJUSTMENT_MODE_RELATIVE</td>
<td>Selects the mode for the Fine Delay Adjust block</td>
<td>FIXED</td>
<td>Delay of the Fine Delay Adjust Block is fixed, the value is specified by the FDA_RELATIVE parameter setting</td>
</tr>
<tr>
<td></td>
<td></td>
<td>DYNAMIC</td>
<td>Delay of Fine Delay Adjust Block is determined by the signal value at the DYNAMICDELAY[7:4] pins</td>
</tr>
<tr>
<td>FDA_RELATIVE</td>
<td>Sets a constant value for the Fine Delay Adjust Block</td>
<td>0, 1,…,15</td>
<td>The PLLOUTGLOBALA &amp; PLLOUTCOREA signals are additionally delayed by (n+1)*150 ps, where n = FDA_RELATIVE. Used if DELAY_ADJUSTMENT_MODE_RELATIVE is &quot;FIXED&quot;.</td>
</tr>
</tbody>
</table>
| SHIFTREG_DIV_MODE              | Selects shift register configuration              | 0,1             | Used when FEEDBACK_PATH is "PHASE_AND_DELAY".
|                                |                                                  |                 | 0⇒Divide by 4
|                                |                                                  |                 | 1⇒Divide by 7 |
| PLLOUT_SELECT                  | Selects the signal to be output at the PLLOUTCORE and PLLOUTGLOBAL ports | SHIFTREG_0deg   | 0° phase shift only if the setting of FEEDBACK_PATH is "PHASE_AND_DELAY" |
|                                |                                                  | SHIFTREG_90deg  | 90° phase shift only if the setting of FEEDBACK_PATH is "PHASE_AND_DELAY" and SHIFTREG_DIV_MODE=0 |
|                                |                                                  | GENCLK          | The internally generated PLL frequency will be output without any phase shift. |
|                                |                                                  | GENCLK_HALF     | The internally generated PLL frequency will be divided by 2 and then output. No phase shift. |
| DIVR                           | REFERENCECLK divider                             | 0,1,2,…,15      | These parameters are used to |
| DIVF            | Feedback divider | 0,1,...,63 | control the output frequency, depending on the FEEDBACK_PATH setting. |
| DIVQ            | VCO Divider      | 1,2,...,6  |                                                   |
| FILTER_RANGE    | PLL Filter Range | 0,1,...,7  |                                                   |
| EXTERNAL_DIVIDE_FACTOR | Divide-by factor of a divider in external feedback path | User specified value. Default 1 | Specified only when there is a user-implemented divider in the external feedback path. |
| ENABLE_ICEGATE  | Enables the PLL power-down control | 0 | Power-down control disabled |
|                |                  | 1          | Power-down controlled by LATCHINPUTVALUE input  |
**SB_PLL40_PAD**

The SB_PLL40_PAD primitive should be used when the source clock of the PLL is driven by an input pad that is located in the bottom IO bank (IO Bank 2) or the top IO bank (IO Bank 0), and the source clock is not required inside the FPGA.

![SB_PLL40_PAD Diagram](image)

### Ports

**PACKAGEPIN**: PLL source clock that serves as the input to the SB_PLL40_PAD primitive.

**PLLOUTGLOBAL**: Output clock generated by the PLL, drives a global clock network on the FPGA.

**PLLOUTCORE**: Output clock generated by the PLL, drives regular FPGA routing. The frequency generated on this output is the same as the frequency of the clock signal generated on the PLLOUTGLOBAL port.

**LOCK**: Output port, when HIGH, indicates that the signal on PLLOUTGLOBAL/PLLOUTCORE is locked to the PLL source on REFERENCECLK.

**EXTFEEDBACK**: External feedback input to PLL. Enabled when the FEEDBACK_PATH parameter is set to EXTERNAL.

**DYNAMICDELAY**: 7 bit input bus that enables dynamic control of the delay contributed by the Fine Delay Adjust Block. The Fine Delay Adjust Block is used when there is a need to adjust the phase alignment of PLLOUTGLOBAL/PLLOUTCORE with respect to REFERENCECLK. The DYNAMICDELAY port controls are enabled when the DELAY_ADJUSTMENT_MODE parameter is set to DYNAMIC.

**RESETB**: Active low input that asynchronously resets the PLL.

**BYPASS**: Input signal, when asserted, connects the signal on REFERENCECLK to PLLOUTCORE/PLLOUTGLOBAL pins.

**LATCHINPUTVALUE**: Active high input, when enabled, forces the PLL into low-power mode. The PLLOUTGLOBAL/PLLOUTCORE pins are held static at their last value. This function is enabled when the parameter ENABLE_ICEGATE is set to ‘1’.

**SCLK, SDI, SDO**: These pins are used only for internal testing purposes, and need not be instantiated by users.
Parameters
The SB_PLL40_PAD primitive requires configuration through the specification of the following parameters. It is strongly recommended that the configuration of the PLL primitives be accomplished through the use of the PLL Configuration tool that is offered as part of the iCEcube2 software.
<table>
<thead>
<tr>
<th>Parameter Name</th>
<th>Description</th>
<th>Parameter Value</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>FEEDBACK_PATH</td>
<td>Selects the feedback path to the PLL</td>
<td>SIMPLE</td>
<td>Feedback is internal to the PLL, directly from VCO</td>
</tr>
<tr>
<td></td>
<td></td>
<td>DELAY</td>
<td>Feedback is internal to the PLL, through the Fine Delay Adjust Block</td>
</tr>
<tr>
<td></td>
<td></td>
<td>PHASE_AND_DELAY</td>
<td>Feedback is internal to the PLL, through the Phase Shifter and the Fine Delay Adjust Block</td>
</tr>
<tr>
<td></td>
<td></td>
<td>EXTERNAL</td>
<td>Feedback path is external to the PLL, and connects to EXTFEEDBACK pin. Also uses the Fine Delay Adjust Block.</td>
</tr>
<tr>
<td>DELAY_ADJUSTMENT_MODE_FEEDBACK</td>
<td>Selects the mode for the Fine Delay Adjust block in the feedback path</td>
<td>FIXED</td>
<td>Delay of the Fine Delay Adjust Block is fixed, the value is specified by the FDA_FEEDBACK parameter setting</td>
</tr>
<tr>
<td></td>
<td></td>
<td>DYNAMIC</td>
<td>Delay of Fine Delay Adjust Block is determined by the signal value at the DYNAMICDELAY[3:0] pins</td>
</tr>
<tr>
<td>FDA_FEEDBACK</td>
<td>Sets a constant value for the Fine Delay Adjust Block in the feedback path</td>
<td>0, 1,…,15</td>
<td>The PLLOUTGLOBAL &amp; PLLOUTCORE signals are delay compensated by (n+1)*150 ps, where n = FDA_FEEDBACK only if the setting of the DELAY_ADJUSTMENT_MODE_FEEDBACK is FIXED.</td>
</tr>
<tr>
<td>FDA_RELATIVE</td>
<td>Sets a constant value for the Fine Delay Adjust Block</td>
<td>0, 1,…,15</td>
<td>The PLLOUTGLOBALA &amp; PLLOUTCOREA signals are additionally delayed by (n+1)*150 ps, where n = FDA_RELATIVE. Used if DELAY_ADJUSTMENT_MODE_RELATIVE is &quot;FIXED&quot;.</td>
</tr>
<tr>
<td>SHIFTREG_DIV_MODE</td>
<td>Selects shift register configuration</td>
<td>0,1</td>
<td>Used when FEEDBACK_PATH is &quot;PHASE_AND_DELAY&quot;. 0→Divide by 4 1→Divide by 7</td>
</tr>
<tr>
<td>PLLOUT_SELECT</td>
<td>Selects the signal to be output at the PLLOUTCORE and PLLOUTGLOBAL ports</td>
<td>SHIFTREG_0deg</td>
<td>0° phase shift only if the setting of FEEDBACK_PATH is &quot;PHASE_AND_DELAY&quot;</td>
</tr>
<tr>
<td></td>
<td></td>
<td>SHIFTREG_90deg</td>
<td>90° phase shift only if the setting of FEEDBACK_PATH is &quot;PHASE_AND_DELAY&quot; and SHIFTREG_DIV_MODE=0</td>
</tr>
<tr>
<td></td>
<td></td>
<td>GENCLK</td>
<td>The internally generated PLL frequency will be output without any phase shift.</td>
</tr>
<tr>
<td></td>
<td></td>
<td>GENCLK_HALF</td>
<td>The internally generated PLL frequency will be divided by 2 and then output. No phase shift.</td>
</tr>
<tr>
<td>DIVR</td>
<td>REFERENCECLK divider</td>
<td>0,1,2,…,15</td>
<td>These parameters are used to</td>
</tr>
<tr>
<td>DIVF</td>
<td>Feedback divider</td>
<td>0,1,...,63</td>
<td>control the output frequency, depending on the FEEDBACK_PATH setting.</td>
</tr>
<tr>
<td>---------</td>
<td>-----------------</td>
<td>-----------</td>
<td>---------------------------------------------------------------</td>
</tr>
<tr>
<td>DIVQ</td>
<td>VCO Divider</td>
<td>1,2,...,6</td>
<td></td>
</tr>
<tr>
<td>FILTER_RANGE</td>
<td>PLL Filter Range</td>
<td>0,1,...,7</td>
<td></td>
</tr>
<tr>
<td>EXTERNAL_DIVIDE_FACTOR</td>
<td>Divide-by factor of a divider in external feedback path</td>
<td>User specified value. Default 1</td>
<td>Specified only when there is a user-implemented divider in the external feedback path.</td>
</tr>
<tr>
<td>ENABLE_ICEGATE</td>
<td>Enables the PLL power-down control</td>
<td>0</td>
<td>Power-down control disabled</td>
</tr>
<tr>
<td></td>
<td></td>
<td>1</td>
<td>Power-down controlled by LATCHINPUTVALUE input</td>
</tr>
</tbody>
</table>
**SB_PLL40_2_PAD**

The SB_PLL40_2_PAD primitive should be used when the source clock of the PLL is driven by an input pad that is located in the bottom IO bank (IO Bank 2) or the top IO bank (IO Bank 0), and in addition to the PLL output, the source clock is also required inside the FPGA.

![Diagram of SB_PLL40_2_PAD](image)

**Ports**

- **PACKAGEPIN**: PLL source clock that serves as the input to the SB_PLL_PAD primitive.

- **PLLOUTGLOBALA**: The signal on PACKAGEPIN appears on the FPGA at this pin, and drives a global clock network on the FPGA. Do not use this pin in an external feedback path to the PLL.

- **PLLOUTCOREA**: The signal on PACKAGEPIN appears on the FPGA at this pin, which drives regular FPGA routing. Do not use this pin in an external feedback path to the PLL.

- **PLLOUTGLOBALB**: Output clock generated by the PLL, drives a global clock network on the FPGA.

- **PLLOUTCOREB**: Output clock generated by the PLL, drives regular FPGA routing. The frequency generated on this output is the same as the frequency of the clock signal generated on the PLLOUTGLOBAL port.

- **LOCK**: Output port, when HIGH, indicates that the signal on PLLOUTGLOBALB/PLLOUTCOREB is locked to the PLL source on PACKAGEPIN.

- **EXTFEEDBACK**: External feedback input to PLL. Enabled when the FEEDBACK_PATH parameter is set to EXTERNAL.

- **DYNAMICDELAY**: 4 bit input bus that enables dynamic control of the delay contributed by the Fine Delay Adjust Block. The Fine Delay Adjust Block is used when there is a need to adjust the phase alignment of PLLOUTGLOBAL/PLLOUTCORE with respect to REFERENCECLK. The DYNAMICDELAY port controls are enabled when the DELAY_ADJUSTMENT_MODE parameter is set to DYNAMIC.

- **RESET**: Active low input that asynchronously resets the PLL.

- **BYPASS**: Input signal, when asserted, connects the signal on REFERENCECLK to PLLOUTCORE/PLLOUTGLOBAL pins.
LATCHINPUTVALUE: Active high input, when enabled, forces the PLL into low-power mode. The PLLOUTGLOBALA/PLLOUTCOREA pins are held static at their last value only when the parameter ENABLE_ICEGATE_PORTA is set to ‘1’, and the LATCHINPUTVALUE signal is asserted. The PLLOUTGLOBALB/PLLOUTCOREB pins are held static at their last value only when the parameter ENABLE_ICEGATE_PORTB is set to ‘1’, and the LATCHINPUTVALUE signal is asserted.

SCLK, SDI, SDO: These pins are used only for internal testing purposes, and need not be instantiated by users.

Parameters
The SB_PLL40_2_PAD primitive requires configuration through the specification of the following parameters. It is strongly recommended that the configuration of the PLL primitives be accomplished through the use of the PLL Configuration tool that is offered as part of the iCEcube2 software.
<table>
<thead>
<tr>
<th>Parameter Name</th>
<th>Description</th>
<th>Parameter Value</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>FEEDBACK_PATH</td>
<td>Selects the feedback path to the PLL</td>
<td>SIMPLE</td>
<td>Feedback is internal to the PLL, directly from VCO</td>
</tr>
<tr>
<td></td>
<td></td>
<td>DELAY</td>
<td>Feedback is internal to the PLL, through the Fine Delay Adjust Block</td>
</tr>
<tr>
<td></td>
<td></td>
<td>PHASE_AND_DELAY</td>
<td>Feedback is internal to the PLL, through the Phase Shifter and the Fine Delay Adjust Block</td>
</tr>
<tr>
<td></td>
<td></td>
<td>EXTERNAL</td>
<td>Feedback path is external to the PLL, and connects to EXTFEEDBACK pin. Also uses the Fine Delay Adjust Block.</td>
</tr>
<tr>
<td>DELAY_ADJUSTMENT_MODE _FEEDBACK</td>
<td>Selects the mode for the Fine Delay Adjust block in the feedback path</td>
<td>FIXED</td>
<td>Delay of the Fine Delay Adjust Block is fixed, the value is specified by the FDA_FEEDBACK parameter setting</td>
</tr>
<tr>
<td></td>
<td></td>
<td>DYNAMIC</td>
<td>Delay of Fine Delay Adjust Block is determined by the signal value at the DYNAMICDELAY[3:0] pins</td>
</tr>
<tr>
<td>FDA_FEEDBACK</td>
<td>Sets a constant value for the Fine Delay Adjust Block in the feedback path</td>
<td>0, 1,…,15</td>
<td>The PLLOUTGLOBAL &amp; PLLOUTCORE signals are delay compensated by (n+1)*150 ps, where n = FDA_FEEDBACK only if the setting of the DELAY_ADJUSTMENT_MODE _FEEDBACK is FIXED.</td>
</tr>
<tr>
<td>DELAY_ADJUSTMENT_MODE _RELATIVE</td>
<td>Selects the mode for the Fine Delay Adjust block</td>
<td>FIXED</td>
<td>Delay of the Fine Delay Adjust Block is fixed, the value is specified by the FDA_RELATIVE parameter setting</td>
</tr>
<tr>
<td></td>
<td></td>
<td>DYNAMIC</td>
<td>Delay of Fine Delay Adjust Block is determined by the signal value at the DYNAMICDELAY[7:4] pins</td>
</tr>
<tr>
<td>FDA_RELATIVE</td>
<td>Sets a constant value for the Fine Delay Adjust Block</td>
<td>0, 1,…,15</td>
<td>The PLLOUTGLOBALA &amp; PLLOUTCOREA signals are delayed w.r.t. the Port B signals, by (n+1)*150 ps, where n = FDA_RELATIVE. Used if DELAY_ADJUSTMENT_MODE _RELATIVE is “FIXED”.</td>
</tr>
<tr>
<td>SHIFTREG_DIV_MODE</td>
<td>Selects shift register configuration</td>
<td>0,1</td>
<td>Used when FEEDBACK_PATH is “PHASE_AND_DELAY”. 0⇒Divide by 4 1⇒Divide by 7</td>
</tr>
<tr>
<td>PLLOUT_SELECT_PORTB</td>
<td>Selects the signal to be output at the PLLOUTCOREB and PLLOUTGLOBALB ports</td>
<td>SHIFTREG_0deg</td>
<td>0° phase shift only if the setting of FEEDBACK_PATH is “PHASE_AND_DELAY”</td>
</tr>
<tr>
<td></td>
<td></td>
<td>SHIFTREG_90deg</td>
<td>90° phase shift only if the setting of FEEDBACK_PATH is “PHASE_AND_DELAY” and SHIFTREG_DIV_MODE=0</td>
</tr>
<tr>
<td></td>
<td></td>
<td>GENCLK</td>
<td>The internally generated PLL frequency will be output to PortB. No phase shift.</td>
</tr>
<tr>
<td></td>
<td></td>
<td>GENCLK_HALF</td>
<td>The internally generated PLL frequency will be divided by 2 and then output to PORTB. No phase shift.</td>
</tr>
<tr>
<td>Parameter</td>
<td>Description</td>
<td>Values</td>
<td>Notes</td>
</tr>
<tr>
<td>----------------------</td>
<td>-----------------------------------------------------------------------------</td>
<td>----------------</td>
<td>-----------------------------------------------------------------------------------------------</td>
</tr>
<tr>
<td>DIVR</td>
<td>REFERENCECLK divider</td>
<td>0,1,2,…,15</td>
<td>These parameters are used to control the output frequency, depending on the FEEDBACK_PATH setting.</td>
</tr>
<tr>
<td>DIVF</td>
<td>Feedback divider</td>
<td>0,1,…,63</td>
<td></td>
</tr>
<tr>
<td>DIVQ</td>
<td>VCO Divider</td>
<td>1,2,…,6</td>
<td></td>
</tr>
<tr>
<td>FILTER_RANGE</td>
<td>PLL Filter Range</td>
<td>0,1,…,7</td>
<td></td>
</tr>
<tr>
<td>EXTERNAL_DIVIDE_FACTOR</td>
<td>Divide-by factor of a divider in external feedback path</td>
<td>User specified value. Default 1</td>
<td>Specified only when there is a user-implemented divider in the external feedback path.</td>
</tr>
<tr>
<td>ENABLE_ICEGATE_PORTA</td>
<td>Enables the PLL power-down control</td>
<td>0,1</td>
<td>Power-down control disabled / Power-down controlled by LATCHINPUTVALUE input</td>
</tr>
<tr>
<td>ENABLE_ICEGATE_PORTB</td>
<td>Enables the PLL power-down control</td>
<td>0,1</td>
<td>Power-down control disabled / Power-down controlled by LATCHINPUTVALUE input</td>
</tr>
</tbody>
</table>

**SB_PLL40_2F_CORE**

The SB_PLL40_2F_CORE primitive should be used when PLL is used to generate 2 different output frequencies, and the source clock of the PLL is driven by FPGA routing i.e. when the PLL source clock originates on the FPGA.

<table>
<thead>
<tr>
<th>Port</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>REFERENCECLK</td>
<td>PLL source clock that serves as the input to the SB_PLL40_2F_CORE primitive.</td>
</tr>
<tr>
<td>PLLOUTGLOBALA</td>
<td>Output clock generated by the PLL, drives a global clock network on the FPGA.</td>
</tr>
<tr>
<td>PLLOUTCOREA</td>
<td>Output clock generated by the PLL, drives regular FPGA routing. The frequency generated on this output is the same as the frequency of the clock signal generated on the PLLOUTGLOBALA port.</td>
</tr>
<tr>
<td>PLLOUTGLOBALB</td>
<td>Output clock generated by the PLL, drives a global clock network on the FPGA.</td>
</tr>
<tr>
<td>PLLOUTCOREB</td>
<td>Output clock generated by the PLL, drives regular FPGA routing. The frequency generated on this output is the same as the frequency of the clock signal generated on the PLLOUTGLOBALB port.</td>
</tr>
<tr>
<td>LOCK</td>
<td>Output port, when HIGH, indicates that the signal on PLLOUTGLOBALB/PLLOUTCOREB is locked to the PLL source on PACKAGEPIN.</td>
</tr>
</tbody>
</table>

**Ports**

**REFERENCECLK**: PLL source clock that serves as the input to the SB_PLL40_2F_CORE primitive.

**PLLOUTGLOBALA**: Output clock generated by the PLL, drives a global clock network on the FPGA.

**PLLOUTCOREA**: Output clock generated by the PLL, drives regular FPGA routing. The frequency generated on this output is the same as the frequency of the clock signal generated on the PLLOUTGLOBALA port.

**PLLOUTGLOBALB**: Output clock generated by the PLL, drives a global clock network on the FPGA.

**PLLOUTCOREB**: Output clock generated by the PLL, drives regular FPGA routing. The frequency generated on this output is the same as the frequency of the clock signal generated on the PLLOUTGLOBALB port.

**LOCK**: Output port, when HIGH, indicates that the signal on PLLOUTGLOBALB/PLLOUTCOREB is locked to the PLL source on PACKAGEPIN.
**EXTFEEDBACK**: External feedback input to PLL. Enabled when the FEEDBACK_PATH parameter is set to EXTERNAL.

**DYNAMICDELAY**: 4 bit input bus that enables dynamic control of the delay contributed by the Fine Delay Adjust Block. The Fine Delay Adjust Block is used when there is a need to adjust the phase alignment of PLLGLOBAL/PLLOUTCORE with respect to REFERENCECLK. The DYNAMICDELAY port controls are enabled when the DELAY_ADJUSTMENT_MODE parameter is set to DYNAMIC.

**RESETB**: Active low input that asynchronously resets the PLL.

**BYPASS**: Input signal, when asserted, connects the signal on REFERENCECLK to PLLCORE/PLLGLOBAL pins.

**LATCHINPUTVALUE**: Active high input, when enabled, forces the PLL into low-power mode. The PLLGLOBALA/PLLOUTCOREA pins are held static at their last value only when the parameter ENABLE_ICEGATE_PORTA is set to ‘1’, and the LATCHINPUTVALUE signal is asserted. The PLLGLOBALB/PLLOUTCOREB pins are held static at their last value only when the parameter ENABLE_ICEGATE_PORTB is set to ‘1’, and the LATCHINPUTVALUE signal is asserted.

**SCLK, SDI, SDO**: These pins are used only for internal testing purposes, and need not be instantiated by users.

**Parameters**
The SB_PLL40_2F_CORE primitive requires configuration through the specification of the following parameters. It is strongly recommended that the configuration of the PLL primitives be accomplished through the use of the PLL Configuration tool that is offered as part of the iCEcube2 software.
<table>
<thead>
<tr>
<th>Parameter Name</th>
<th>Description</th>
<th>Parameter Value</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>FEEDBACK_PATH</td>
<td>Selects the feedback path to the PLL</td>
<td>SIMPLE</td>
<td>Feedback is internal to the PLL, directly from VCO</td>
</tr>
<tr>
<td></td>
<td></td>
<td>DELAY</td>
<td>Feedback is internal to the PLL, through the Fine Delay Adjust Block</td>
</tr>
<tr>
<td></td>
<td></td>
<td>PHASE_AND_DELAY</td>
<td>Feedback is internal to the PLL, through the Phase Shifter and the Fine Delay Adjust Block</td>
</tr>
<tr>
<td></td>
<td></td>
<td>EXTERNAL</td>
<td>Feedback path is external to the PLL, and connects to EXTFEEDBACK pin. Also uses the Fine Delay Adjust Block.</td>
</tr>
<tr>
<td>DELAY_ADJUSTMENT_MODE _FEEDBACK</td>
<td>Selects the mode for the Fine Delay Adjust block in the feedback path</td>
<td>FIXED</td>
<td>Delay of the Fine Delay Adjust Block is fixed, the value is specified by the FDA_FEEDBACK parameter setting</td>
</tr>
<tr>
<td></td>
<td></td>
<td>DYNAMIC</td>
<td>Delay of Fine Delay Adjust Block is determined by the signal value at the DYNAMICDELAY[3:0] pins</td>
</tr>
<tr>
<td>FDA_FEEDBACK</td>
<td>Sets a constant value for the Fine Delay Adjust Block in the feedback path</td>
<td>0, 1,…,15</td>
<td>The PLLOUTGLOBALA &amp; PLLOUTCOREA signals are delay compensated by (n+1)*150 ps, where n = FDA_FEEDBACK only if the setting of the DELAY_ADJUSTMENT_MODE _FEEDBACK is FIXED.</td>
</tr>
<tr>
<td>DELAY_ADJUSTMENT_MODE _RELATIVE</td>
<td>Selects the mode for the Fine Delay Adjust block</td>
<td>FIXED</td>
<td>Delay of the Fine Delay Adjust Block is fixed, the value is specified by the FDA_RELATIVE parameter setting</td>
</tr>
<tr>
<td></td>
<td></td>
<td>DYNAMIC</td>
<td>Delay of Fine Delay Adjust Block is determined by the signal value at the DYNAMICDELAY[7:4] pins</td>
</tr>
<tr>
<td>FDA_RELATIVE</td>
<td>Sets a constant value for the Fine Delay Adjust Block</td>
<td>0, 1,…,15</td>
<td>The PLLOUTGLOBALA &amp; PLLOUTCOREA signals are delayed w.r.t. the Port B signals, by (n+1)*150 ps, where n = FDA_RELATIVE. Used if DELAY_ADJUSTMENT_MODE _RELATIVE is “FIXED”.</td>
</tr>
<tr>
<td>SHIFTREG_DIV_MODE</td>
<td>Selects shift register configuration</td>
<td>0,1</td>
<td>Used when FEEDBACK_PATH is “PHASE_AND_DELAY”: 0→Divide by 4 1→Divide by 7</td>
</tr>
<tr>
<td>PLLOUT_SELECT_PORTA</td>
<td>Selects the signal to be output at the PLLOUTCOREA and PLLOUTGLOBALA ports</td>
<td>SHIFTREG_0deg</td>
<td>0° phase shift only if the setting of FEEDBACK_PATH is “PHASE_AND_DELAY”</td>
</tr>
<tr>
<td></td>
<td></td>
<td>SHIFTREG_90deg</td>
<td>90° phase shift only if the setting of FEEDBACK_PATH is “PHASE_AND_DELAY” and SHIFTREG_DIV_MODE=0</td>
</tr>
<tr>
<td></td>
<td></td>
<td>GENCLK</td>
<td>The internally generated PLL frequency will be output to PortA. No phase shift.</td>
</tr>
<tr>
<td></td>
<td></td>
<td>GENCLK_HALF</td>
<td>The internally generated PLL frequency will be divided by 2 and then output to PORTA. No phase shift.</td>
</tr>
<tr>
<td>Parameter</td>
<td>Description</td>
<td>Type</td>
<td>Default</td>
</tr>
<tr>
<td>---------------------------------</td>
<td>-----------------------------------------------------------------------------</td>
<td>-------------------</td>
<td>---------</td>
</tr>
<tr>
<td>PLLOUT_SELECT_PORTB</td>
<td>Selects the signal to be output at the PLLOUTCOREB and PLLOUTGLOBALB ports</td>
<td></td>
<td></td>
</tr>
<tr>
<td>SHIFTREG_0deg</td>
<td>0° phase shift only if the setting of FEEDBACK_PATH is “PHASE_AND_DELAY”</td>
<td></td>
<td></td>
</tr>
<tr>
<td>SHIFTREG_90deg</td>
<td>90° phase shift only if the setting of FEEDBACK_PATH is “PHASE_AND_DELAY”</td>
<td></td>
<td></td>
</tr>
<tr>
<td>GENCLK</td>
<td>The internally generated PLL frequency will be output to PortB. No phase shift.</td>
<td></td>
<td></td>
</tr>
<tr>
<td>GENCLK_HALF</td>
<td>The internally generated PLL frequency will be divided by 2 and then output to PORTB. No phase shift.</td>
<td></td>
<td></td>
</tr>
<tr>
<td>DIVR</td>
<td>REFERENCECLK divider</td>
<td>0,1,2,…,15</td>
<td></td>
</tr>
<tr>
<td>DIVF</td>
<td>Feedback divider</td>
<td>0,1,…,63</td>
<td></td>
</tr>
<tr>
<td>DIVQ</td>
<td>VCO Divider</td>
<td>1,2,…,6</td>
<td></td>
</tr>
<tr>
<td>FILTER_RANGE</td>
<td>PLL Filter Range</td>
<td>0,1,…,7</td>
<td></td>
</tr>
<tr>
<td>EXTERNAL_DIVIDE_FACTOR</td>
<td>Divide-by factor of a divider in external feedback path</td>
<td>User specified value. Default 1</td>
<td></td>
</tr>
<tr>
<td>ENABLE_ICEGATE_PORTA</td>
<td>Enables the PLL power-down control</td>
<td></td>
<td></td>
</tr>
<tr>
<td>ENABLE_ICEGATE_PORTB</td>
<td>Enables the PLL power-down control</td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

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**SB_PLL40_2F_PAD**

The SB_PLL40_2F_PAD primitive should be used when the PLL is used to generate 2 different output frequencies, and the source clock of the PLL is driven by an input pad located in the bottom IO bank (IO Bank 2) or the top IO bank (IO Bank 0).

![SB_PLL40_2F_PAD Diagram](image)

**Ports**

- **PACKAGEPIN**: PLL source clock that serves as the input to the SB_PLL40_2F_PAD primitive.
- **PLLOUTGLOBALA**: Output clock generated by the PLL, drives a global clock network on the FPGA.
- **PLLOUTCOREA**: Output clock generated by the PLL, drives regular FPGA routing. The frequency generated on this output is the same as the frequency of the clock signal generated on the PLLOUTGLOBALA port.
- **PLLOUTGLOBALB**: Output clock generated by the PLL, drives a global clock network on the FPGA.
- **PLLOUTCOREB**: Output clock generated by the PLL, drives regular FPGA routing. The frequency generated on this output is the same as the frequency of the clock signal generated on the PLLOUTGLOBALB port.
- **LOCK**: Output port, when HIGH, indicates that the signal on PLLOUTGLOBALB/PLLOUTCOREB is locked to the PLL source on PACKAGEPIN.
- **EXTFEEDBACK**: External feedback input to PLL. Enabled when the FEEDBACK_PATH parameter is set to EXTERNAL.
- **DYNAMICDELAY**: 4 bit input bus that enables dynamic control of the delay contributed by the Fine Delay Adjust Block. The Fine Delay Adjust Block is used when there is a need to adjust the phase alignment of PLLOUTGLOBAL/PLLOUTCORE with respect to REFERENCECLK. The DYNAMICDELAY port controls are enabled when the DELAY_ADJUSTMENT_MODE parameter is set to DYNAMIC.
- **RESETB**: Active low input that asynchronously resets the PLL.
- **BYPASS**: Input signal, when asserted, connects the signal on REFERENCECLK to PLLOUTCORE/PLLOUTGLOBAL pins.
**LATCHINPUTVALUE:** Active high input, when enabled, forces the PLL into low-power mode. The PLLOUTGLOBALA/PLLOUTCOREA pins are held static at their last value only when the parameter ENABLE_ICEGATE_PORTA is set to ‘1’, and the LATCHINPUTVALUE signal is asserted. The PLLOUTGLOBALB/PLLOUTCOREB pins are held static at their last value only when the parameter ENABLE_ICEGATE_PORTB is set to ‘1’, and the LATCHINPUTVALUE signal is asserted.

**SCLK, SDI, SDO:** These pins are used only for internal testing purposes, and need not be instantiated by users.

**Parameters**
The SB_PLL40_2F_PAD primitive requires configuration through the specification of the following parameters. It is strongly recommended that the configuration of the PLL primitives be accomplished through the use of the PLL Configuration tool that is offered as part of the iCEcube2 software.
<table>
<thead>
<tr>
<th>Parameter Name</th>
<th>Description</th>
<th>Parameter Value</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>FEEDBACK_PATH</td>
<td>Selects the feedback path to the PLL</td>
<td>SIMPLE</td>
<td>Feedback is internal to the PLL, directly from VCO</td>
</tr>
<tr>
<td></td>
<td></td>
<td>DELAY</td>
<td>Feedback is internal to the PLL, through the Fine Delay Adjust Block</td>
</tr>
<tr>
<td></td>
<td></td>
<td>PHASE_AND_DELAY</td>
<td>Feedback is internal to the PLL, through the Phase Shifter and the Fine Delay Adjust Block</td>
</tr>
<tr>
<td></td>
<td></td>
<td>EXTERNAL</td>
<td>Feedback path is external to the PLL, and connects to EXTFEEDBACK pin. Also uses the Fine Delay Adjust Block.</td>
</tr>
<tr>
<td>DELAY_ADJUSTMENT_MODE_FEEDBACK</td>
<td>Selects the mode for the Fine Delay Adjust block in the feedback path</td>
<td>FIXED</td>
<td>Delay of the Fine Delay Adjust Block is fixed, the value is specified by the FDA_FEEDBACK parameter setting</td>
</tr>
<tr>
<td></td>
<td></td>
<td>DYNAMIC</td>
<td>Delay of Fine Delay Adjust Block is determined by the signal value at the DYNAMICDELAY[3:0] pins</td>
</tr>
<tr>
<td>FDA_FEEDBACK</td>
<td>Sets a constant value for the Fine Delay Adjust Block in the feedback path</td>
<td>0, 1,…,15</td>
<td>The PLLOUTGLOBALA &amp; PLLOUTCOREA signals are delay compensated by (n+1)*150 ps, where n = FDA_FEEDBACK only if the setting of the DELAY_ADJUSTMENT_MODE_FEEDBACK is FIXED.</td>
</tr>
<tr>
<td>DELAY_ADJUSTMENT_MODE_RELATIVE</td>
<td>Selects the mode for the Fine Delay Adjust block</td>
<td>FIXED</td>
<td>Delay of the Fine Delay Adjust Block is fixed, the value is specified by the FDA_RELATIVE parameter setting</td>
</tr>
<tr>
<td></td>
<td></td>
<td>DYNAMIC</td>
<td>Delay of Fine Delay Adjust Block is determined by the signal value at the DYNAMICDELAY[7:4] pins</td>
</tr>
<tr>
<td>FDA_RELATIVE</td>
<td>Sets a constant value for the Fine Delay Adjust Block</td>
<td>0, 1,…,15</td>
<td>The PLLOUTGLOBALA &amp; PLLOUTCOREA signals are delayed w.r.t. the Port B signals, by (n+1)*150 ps, where n = FDA_RELATIVE. Used if DELAY_ADJUSTMENT_MODE_RELATIVE is “FIXED”.</td>
</tr>
<tr>
<td>SHIFTREG_DIV_MODE</td>
<td>Selects shift register configuration</td>
<td>0, 1</td>
<td>Used when FEEDBACK_PATH is “PHASE_AND_DELAY”: 0→Divide by 4, 1→Divide by 7</td>
</tr>
<tr>
<td>PLLOUT_SELECT_PORTA</td>
<td>Selects the signal to be output at the PLLOUTCOREA and PLLOUTGLOBALA ports</td>
<td>SHIFTREG_0deg</td>
<td>0° phase shift only if the setting of FEEDBACK_PATH is “PHASE_AND_DELAY”</td>
</tr>
<tr>
<td></td>
<td></td>
<td>SHIFTREG_90deg</td>
<td>90° phase shift only if the setting of FEEDBACK_PATH is “PHASE_AND_DELAY” and SHIFTREG_DIV_MODE=0</td>
</tr>
<tr>
<td></td>
<td></td>
<td>GENCLK</td>
<td>The internally generated PLL frequency will be output to PortA. No phase shift.</td>
</tr>
<tr>
<td></td>
<td></td>
<td>GENCLK_HALF</td>
<td>The internally generated PLL frequency will be divided by 2 and then output to PORTA. No phase shift.</td>
</tr>
<tr>
<td>Parameter</td>
<td>Description</td>
<td>Value(s)</td>
<td>Details</td>
</tr>
<tr>
<td>---------------------</td>
<td>------------------------------------------------------------------------------</td>
<td>---------------------------</td>
<td>-------------------------------------------------------------------------</td>
</tr>
<tr>
<td>PLLOUT_SELECT_PORTB</td>
<td>Selects the signal to be output at the PLLOUTCOREB and PLLOUTGLOBALB ports</td>
<td></td>
<td></td>
</tr>
<tr>
<td>SHIFTREG_0deg</td>
<td></td>
<td>0° phase shift only if the setting of FEEDBACK_PATH is “PHASE_AND_DELAY”</td>
<td></td>
</tr>
<tr>
<td>SHIFTREG_90deg</td>
<td></td>
<td>90° phase shift only if the setting of FEEDBACK_PATH is “PHASE_AND_DELAY” and SHIFTREG_DIV_MODE=0</td>
<td></td>
</tr>
<tr>
<td>GENCLK</td>
<td>The internally generated PLL frequency will be output to PortB. No phase shift.</td>
<td></td>
<td></td>
</tr>
<tr>
<td>GENCLK_HALF</td>
<td>The internally generated PLL frequency will be divided by 2 and then output to PORTB. No phase shift.</td>
<td></td>
<td></td>
</tr>
<tr>
<td>DIVR</td>
<td>REFERENCECLK divider</td>
<td>0,1,2,.....,15</td>
<td>These parameters are used to control the output frequency, depending on the FEEDBACK_PATH setting.</td>
</tr>
<tr>
<td>DIVF</td>
<td>Feedback divider</td>
<td>0,1,....,63</td>
<td></td>
</tr>
<tr>
<td>DIVQ</td>
<td>VCO Divider</td>
<td>1,2,....,6</td>
<td></td>
</tr>
<tr>
<td>FILTER_RANGE</td>
<td>PLL Filter Range</td>
<td>0,1,.....,7</td>
<td></td>
</tr>
<tr>
<td>EXTERNAL_DIVIDE_FACTOR</td>
<td>Divide-by factor of a divider in external feedback path</td>
<td>User specified value.</td>
<td>Specified only when there is a user-implemented divider in the external feedback path.</td>
</tr>
<tr>
<td>ENABLE_ICEGATE_PORTA</td>
<td>Enables the PLL power-down control</td>
<td>0</td>
<td>Power-down control disabled</td>
</tr>
<tr>
<td></td>
<td></td>
<td>1</td>
<td>Power-down controlled by LATCHINPUTVALUE input</td>
</tr>
<tr>
<td>ENABLE_ICEGATE_PORTB</td>
<td>Enables the PLL power-down control</td>
<td>0</td>
<td>Power-down control disabled</td>
</tr>
<tr>
<td></td>
<td></td>
<td>1</td>
<td>Power-down controlled by LATCHINPUTVALUE input</td>
</tr>
</tbody>
</table>
**Hard Macro Primitives**

*iCE40LM Hard Macros*

This section describes the following dedicated hard macro primitives available in iCE40LM devices.

- **SB_HSOSC** (macro primitive for HSSG)
- **SB_LSOSC** (macro primitive for LPSG)
- **SB_I2C**
- **SB_SPI**

**SB_HSOSC (For HSSG)**

SB_HSOSC primitive can be used to instantiate High Speed Strobe Generator (HSSG), which generates 12 MHz strobe signal. The strobe can drive either the global clock network or fabric routes directly based on the clock network selection.

![SB_HSOSC Diagram]

**Ports**

<table>
<thead>
<tr>
<th>Signal Name</th>
<th>Direction</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>ENACLKM</td>
<td>Input</td>
<td>Enable High Speed Strobe Generator. Active High.</td>
</tr>
<tr>
<td>CLKM</td>
<td>Output</td>
<td>Strobe Generator Output (12Mhz).</td>
</tr>
</tbody>
</table>

**Clock Network Selection**

By default the strobe generator use one of the dedicated clock networks in the device to drive the elements. The user may configure the strobe generator to use the fabric routes instead of global clock network using the synthesis attributes.

**Synthesis Attribute**

```
/* synthesis ROUTE_THROUGH_FABRIC=<value> */
```

Value:

- 0: Use dedicated clock network. Default option.
- 1: Use fabric routes.

**Verilog Instantiation**

```verilog
SB_HSOSC OSCInst0 (
  .ENACLKM(ENACLKM),
  .CLKM(CLKM)
) /* synthesis ROUTE_THROUGH_FABRIC= [0|1] */;
```
**SB_LSOSC (For LPSG)**

SB_LSOSC primitive can instantiate Low Power Strobe Generator (LPSG), which generates 10 KHz strobe signal. The strobe can drive either the global clock network or fabric routes directly based on the clock network selection.

![SB_LSOSC Block Diagram]

<table>
<thead>
<tr>
<th>Signal Name</th>
<th>Direction</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>ENACLKK</td>
<td>Input</td>
<td>Enable Low Power Strobe Generator. Active High.</td>
</tr>
<tr>
<td>CLKK</td>
<td>Output</td>
<td>Strobe Generator Output (10Khz).</td>
</tr>
</tbody>
</table>

**Clock Network Selection**

By default the strobe generator use one of the dedicated clock networks in the device to drive the elements. The user may configure the strobe generator to use the fabric routes instead of global clock network using the synthesis attribute.

**Synthesis Attribute:**

```
/* synthesis ROUTE_THROUGH_FABRIC=<value> */
```

- **Value:**
  - 0: Use dedicated clock network. Default option.
  - 1: Use fabric routes.

**Verilog Instantiation**

```verilog
SB_LSOSC OSCInst0 (  .ENACLKK(ENACLKK),  .CLKK(CLKK) ) /* synthesis ROUTE_THROUGH_FABRIC= [0|1] */;
```

**SB_I2C**

The I2C hard IP provides industry standard two pin communication interface that conforms to V2.1 of the I2C bus specification. It could be configured as either master or slave port. In master mode, it support configurable data transfer rate and perform arbitration detection to allow it to operate in multi-master systems. It supports both 7 bits and 10 bits addressing in slave mode with configurable slave address and clock stretching in both master and slave mode with enable/disable capability.

iCE40LM device supports two I2C hard IP primitives, located at upper left corner and upper right corner of the chip.
## Ports

<table>
<thead>
<tr>
<th>Signal Name</th>
<th>Direction</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>SBCLKI</td>
<td>Input</td>
<td>System Clock input.</td>
</tr>
<tr>
<td>SBRWI</td>
<td>Input</td>
<td>System Read/Write Input.</td>
</tr>
<tr>
<td>SBSTBI</td>
<td>Input</td>
<td>Strobe Signal</td>
</tr>
<tr>
<td>SBADRI0</td>
<td>Input</td>
<td>System Bus Control registers address. Bit 0.</td>
</tr>
<tr>
<td>SBADRI1</td>
<td>Input</td>
<td>System Bus Control registers address. Bit 1.</td>
</tr>
<tr>
<td>SBADRI2</td>
<td>Input</td>
<td>System Bus Control registers address. Bit 2.</td>
</tr>
<tr>
<td>SBADRI3</td>
<td>Input</td>
<td>System Bus Control registers address. Bit 3.</td>
</tr>
<tr>
<td>SBADRI5</td>
<td>Input</td>
<td>System Bus Control registers address. Bit 5.</td>
</tr>
<tr>
<td>SBADRI6</td>
<td>Input</td>
<td>System Bus Control registers address. Bit 6.</td>
</tr>
<tr>
<td>SBADRI7</td>
<td>Input</td>
<td>System Bus Control registers address. Bit 7.</td>
</tr>
<tr>
<td>SBDATI0</td>
<td>Input</td>
<td>System Data Input. Bit 0.</td>
</tr>
<tr>
<td>SBDATI1</td>
<td>Input</td>
<td>System Data input. Bit 1.</td>
</tr>
<tr>
<td>SBDATI2</td>
<td>Input</td>
<td>System Data input. Bit 2.</td>
</tr>
<tr>
<td>SBDATI3</td>
<td>Input</td>
<td>System Data input. Bit 3.</td>
</tr>
<tr>
<td>SBDATI5</td>
<td>Input</td>
<td>System Data input. Bit 5.</td>
</tr>
<tr>
<td>SBDATI7</td>
<td>Input</td>
<td>System Data input. Bit 7.</td>
</tr>
<tr>
<td>SBDATO0</td>
<td>Output</td>
<td>System Data Output. Bit 0.</td>
</tr>
<tr>
<td>SBDATO1</td>
<td>Output</td>
<td>System Data Output. Bit 1.</td>
</tr>
<tr>
<td>SBDATO2</td>
<td>Output</td>
<td>System Data Output. Bit 2.</td>
</tr>
<tr>
<td>SBDATO3</td>
<td>Output</td>
<td>System Data Output. Bit 3.</td>
</tr>
<tr>
<td>SBDATO5</td>
<td>Output</td>
<td>System Data Output. Bit 5.</td>
</tr>
<tr>
<td>SBDATO7</td>
<td>Output</td>
<td>System Data Output. Bit 7.</td>
</tr>
<tr>
<td>Parameter</td>
<td>Description</td>
<td></td>
</tr>
<tr>
<td>--------------------</td>
<td>-----------------------------------------------------</td>
<td></td>
</tr>
<tr>
<td>SBACKO</td>
<td>Output System Acknowledgement.</td>
<td></td>
</tr>
<tr>
<td>I2CIRQ</td>
<td>Output I2C Interrupt output.</td>
<td></td>
</tr>
<tr>
<td>I2CWKUP</td>
<td>Output I2C Wake Up from Standby signal.</td>
<td></td>
</tr>
<tr>
<td>SCLI</td>
<td>Input Serial Clock Input.</td>
<td></td>
</tr>
<tr>
<td>SCLO</td>
<td>Output Serial Clock Output</td>
<td></td>
</tr>
<tr>
<td>SCLOE</td>
<td>Output Serial Clock Output Enable. Active High.</td>
<td></td>
</tr>
<tr>
<td>SDAI</td>
<td>Input Serial Data Input</td>
<td></td>
</tr>
<tr>
<td>SDAO</td>
<td>Output Serial Data Output</td>
<td></td>
</tr>
<tr>
<td>SDAOE</td>
<td>Output Serial Data Output Enable. Active High.</td>
<td></td>
</tr>
</tbody>
</table>

**Parameters**

I2C Primitive requires configuring certain parameters for slave initial address and selecting I2C IP location.

<table>
<thead>
<tr>
<th>I2C Location</th>
<th>Parameters</th>
<th>Parameter Default Value.</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>Upper Left Corner</td>
<td>I2C_SLAVE_INIT_ADDR</td>
<td>0b1111100001</td>
<td>Upper Bits &lt;9:2&gt; can be changed through control registers. Lower bits &lt;1:0&gt; are fixed.</td>
</tr>
<tr>
<td></td>
<td>BUS_ADDR74</td>
<td>0b0001</td>
<td>Fixed value. SBADRI [7:4] bits also should match with this value to activate the IP.</td>
</tr>
<tr>
<td>Upper Right Corner</td>
<td>I2C_SLAVE_INIT_ADDR</td>
<td>0b1111100010</td>
<td>Upper Bits &lt;9:2&gt; can be changed through control registers. Lower bits &lt;1:0&gt; are fixed.</td>
</tr>
<tr>
<td></td>
<td>BUS_ADDR74</td>
<td>0b0011</td>
<td>Fixed value. SBADRI [7:4] bits also should match with this value to activate the IP.</td>
</tr>
</tbody>
</table>

**Synthesis Attribute**

Synthesis attribute "I2C_CLK_DIVIDER" is used by PNR and STA tools for optimization and deriving the appropriate clock frequency at SCLO output with respect to the SBCLKI input clock frequency.

```c
/* synthesis I2C_CLK_DIVIDER=[Divide Range] */
```

Divide Range : 0, 1, 2, 3 ... 1023. Default is 0.
Verilog Instantiation

SB_I2C i2cInst0 (  
  .SBCLKI(sbclki),  
  .SBRWI(sbrwi),  
  .SBSTBI(sbstbi),  
  .SBADRI7(sbadri[7]),  
  .SBADRI6(sbadri[6]),  
  .SBADRI5(sbadri[5]),  
  .SBADRI4(sbadri[4]),  
  .SBADRI3(sbadri[3]),  
  .SBADRI2(sbadri[2]),  
  .SBADRI1(sbadri[1]),  
  .SBADRI0(sbadri[0]),  
  .SBDATI7(sbdati[7]),  
  .SBDATI6(sbdati[6]),  
  .SBDATI5(sbdati[5]),  
  .SBDATI4(sbdati[4]),  
  .SBDATI3(sbdati[3]),  
  .SBDATI2(sbdati[2]),  
  .SBDATI1(sbdati[1]),  
  .SBDATI0(sbdati[0]),  
  .SCLI(scli),  
  .SDAI(sda),  
  .SBDATO7(sbdato[7]),  
  .SBDATO6(sbdato[6]),  
  .SBDATO5(sbdato[5]),  
  .SBDATO4(sbdato[4]),  
  .SBDATO3(sbdato[3]),  
  .SBDATO2(sbdato[2]),  
  .SBDATO1(sbdato[1]),  
  .SBDATO0(sbdato[0]),  
  .SBACKO(sbacko),  
  .I2CIRQ(i2cirq),  
  .I2CWKUP(i2cwkup),  
  .SCLO(sclo),  
  .SCLOE(scloe),  
  .SDAO(sdao),  
  .SDAOE(sdaoe)  
)/* synthesis I2C_CLK_DIVIDER= 1 */;

defparam i2cInst0.I2C_SLAVE_INIT_ADDR = "0b1111100001";
defparam i2cInst0.BUS_ADDR74 = "0b0001";

SB_SPI

The SPI hard IP provide industry standard four-pin communication interface with 8 bit wide System Bus to communicate with System Host. It could be configured as Master or Slave SPI port with separate Chip Select Pin. In master mode, it provides programmable baud rate, and supports CS HOLD capability for multiple transfers. It provides variety status flags, such as Mode Fault Error flag, Transmit/Receive status flag etc. for easy communicate with system host.

iCE40LM device supports two SPI hard IP primitives, located at lower left corner and lower right corner of the chip.
## Ports

<table>
<thead>
<tr>
<th>Signal Name</th>
<th>Direction</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>SBCLKI</td>
<td>Input</td>
<td>System Clock input.</td>
</tr>
<tr>
<td>SBRWI</td>
<td>Input</td>
<td>System Read/Write Input.</td>
</tr>
<tr>
<td>SBSTBI</td>
<td>Input</td>
<td>Strobe Signal</td>
</tr>
<tr>
<td>SBADRI0</td>
<td>Input</td>
<td>System Bus Control registers address. Bit 0.</td>
</tr>
<tr>
<td>SBADRI1</td>
<td>Input</td>
<td>System Bus Control registers address. Bit 1.</td>
</tr>
<tr>
<td>SBADRI2</td>
<td>Input</td>
<td>System Bus Control registers address. Bit 2.</td>
</tr>
<tr>
<td>SBADRI3</td>
<td>Input</td>
<td>System Bus Control registers address. Bit 3.</td>
</tr>
<tr>
<td>SBADRI5</td>
<td>Input</td>
<td>System Bus Control registers address. Bit 5.</td>
</tr>
<tr>
<td>SBADRI6</td>
<td>Input</td>
<td>System Bus Control registers address. Bit 6.</td>
</tr>
<tr>
<td>SBADRI7</td>
<td>Input</td>
<td>System Bus Control registers address. Bit 7.</td>
</tr>
<tr>
<td>SBDATI0</td>
<td>Input</td>
<td>System Data Input. Bit 0.</td>
</tr>
<tr>
<td>SBDATI1</td>
<td>Input</td>
<td>System Data input. Bit 1.</td>
</tr>
<tr>
<td>SBDATI2</td>
<td>Input</td>
<td>System Data input. Bit 2.</td>
</tr>
<tr>
<td>SBDATI3</td>
<td>Input</td>
<td>System Data input. Bit 3.</td>
</tr>
<tr>
<td>SBDATI5</td>
<td>Input</td>
<td>System Data input. Bit 5.</td>
</tr>
<tr>
<td>SBDATI7</td>
<td>Input</td>
<td>System Data input. Bit 7.</td>
</tr>
<tr>
<td>SBDATO0</td>
<td>Input</td>
<td>System Data Output. Bit 0.</td>
</tr>
<tr>
<td>SBDATO1</td>
<td>Input</td>
<td>System Data Output. Bit 1.</td>
</tr>
<tr>
<td>SBDATO2</td>
<td>Input</td>
<td>System Data Output. Bit 2.</td>
</tr>
<tr>
<td>SBDATO3</td>
<td>Input</td>
<td>System Data Output. Bit 3.</td>
</tr>
<tr>
<td>SBDATO5</td>
<td>Input</td>
<td>System Data Output. Bit 5.</td>
</tr>
<tr>
<td>SBDATO7</td>
<td>Input</td>
<td>System Data Output. Bit 7.</td>
</tr>
<tr>
<td>-----------</td>
<td>--------------------</td>
<td>-----------------------------</td>
</tr>
<tr>
<td>SBACKO</td>
<td>Output</td>
<td>System Acknowledgement</td>
</tr>
<tr>
<td>SPIIRQ</td>
<td>Output</td>
<td>SPI Interrupt output</td>
</tr>
<tr>
<td>SPIWKUP</td>
<td>Output</td>
<td>SPI Wake Up from Standby signal.</td>
</tr>
<tr>
<td>MI</td>
<td>Input</td>
<td>Master Input from PAD</td>
</tr>
<tr>
<td>SO</td>
<td>Output</td>
<td>Slave Output to PAD</td>
</tr>
<tr>
<td>SOE</td>
<td>Output</td>
<td>Slave Output Enable to PAD. Active High.</td>
</tr>
<tr>
<td>SI</td>
<td>Input</td>
<td>Slave Input from PAD</td>
</tr>
<tr>
<td>MO</td>
<td>Output</td>
<td>Master Output to PAD</td>
</tr>
<tr>
<td>MOE</td>
<td>Output</td>
<td>Master Output Enable to PAD. Active High</td>
</tr>
<tr>
<td>SCKI</td>
<td>Input</td>
<td>Slave Clock Input From PAD</td>
</tr>
<tr>
<td>SCKO</td>
<td>Output</td>
<td>Slave Clock Output to PAD</td>
</tr>
<tr>
<td>SCKOE</td>
<td>Output</td>
<td>Slave Clock Output Enable to PAD. Active High.</td>
</tr>
<tr>
<td>SCSNI</td>
<td>Input</td>
<td>Slave Chip Select Input From PAD</td>
</tr>
<tr>
<td>MCSNO0</td>
<td>Output</td>
<td>Master Chip Select Output to PAD. Line 0.</td>
</tr>
<tr>
<td>MCSNO1</td>
<td>Output</td>
<td>Master Chip Select Output to PAD. Line 1.</td>
</tr>
<tr>
<td>MCSNO2</td>
<td>Output</td>
<td>Master Chip Select Output to PAD. Line 2.</td>
</tr>
<tr>
<td>MCSNO3</td>
<td>Output</td>
<td>Master Chip Select Output to PAD. Line 3.</td>
</tr>
<tr>
<td>MCSNOE0</td>
<td>Output</td>
<td>Master Chip Select Output Enable to PAD. Active High. Line 0.</td>
</tr>
<tr>
<td>MCSNOE1</td>
<td>Output</td>
<td>Master Chip Select Output Enable to PAD. Active High. Line 1.</td>
</tr>
<tr>
<td>MCSNOE2</td>
<td>Output</td>
<td>Master Chip Select Output Enable to PAD. Active High. Line 2.</td>
</tr>
<tr>
<td>MCSNOE3</td>
<td>Output</td>
<td>Master Chip Select Output Enable to PAD. Active High. Line 3</td>
</tr>
</tbody>
</table>

### Parameters

SPI Primitive requires configuring a parameter for selecting the SPI IP location.

<table>
<thead>
<tr>
<th>I2C Location</th>
<th>Parameters</th>
<th>Parameter Default Value.</th>
<th>Description.</th>
</tr>
</thead>
<tbody>
<tr>
<td>Lower Left Corner</td>
<td>BUS_ADDR74</td>
<td>0b0000</td>
<td>Fixed value. SBADRI [7:4] bits also should match with this value to activate the IP.</td>
</tr>
<tr>
<td>Lower Right Corner</td>
<td>BUS_ADDR74</td>
<td>0b0001</td>
<td>Fixed value. SBADRI [7:4] bits also should match with this value to activate the IP.</td>
</tr>
</tbody>
</table>

### Synthesis Attribute

Synthesis attribute “SPI_CLK_DIVIDER” is used by PNR and STA tools for optimization and deriving the appropriate clock frequency at SCKO output with respect to the SBCLKI input clock frequency.

```c
/* synthesis SPI_CLK_DIVIDER= [Divide Range] */

Divide Range : 0, 1, 2, 3…63. Default is 0.
```
Verilog Instantiation

SB_SPI spiInst0 (
  .SBCLKI(sbclki),
  .SBRWI(sbwrwi),
  .SBSTBI(sbstbi),
  .SBADRI7(sbadri[7]),
  .SBADRI6(sbadri[6]),
  .SBADRI5(sbadri[5]),
  .SBADRI4(sbadri[4]),
  .SBADRI3(sbadri[3]),
  .SBADRI2(sbadri[2]),
  .SBADRI1(sbadri[1]),
  .SBADRI0(sbadri[0]),
  .SBDATI7(sbdati[7]),
  .SBDATI6(sbdati[6]),
  .SBDATI5(sbdati[5]),
  .SBDATI4(sbdati[4]),
  .SBDATI3(sbdati[3]),
  .SBDATI2(sbdati[2]),
  .SBDATI1(sbdati[1]),
  .SBDATI0(sbdati[0]),
  .MI(mi),
  .SI(si),
  .SCKI(sck1),
  .SCSNI(scsn1),
  .SBDAT07(sbdato[7]),
  .SBDAT06(sbdato[6]),
  .SBDAT05(sbdato[5]),
  .SBDAT04(sbdato[4]),
  .SBDAT03(sbdato[3]),
  .SBDAT02(sbdato[2]),
  .SBDAT01(sbdato[1]),
  .SBDAT00(sbdato[0]),
  .SBACKO(sbacko),
  .SPIIRQ(spiirq),
  .SPIWKUP(spiwkup),
  .SO(so),
  .SOE(soe),
  .MO(mo),
  .MOE(moe),
  .SCKO(scko),
  .SCKOE(sckoe),
  .MCSNO3(mcsno_hi[3]),
  .MCSNO2(mcsno_hi[2]),
  .MCSNO1(mcsno_lo[1]),
  .MCSNO0(mcsno_lo[0]),
  .MCSNOE3(mcsnoe_hi[3]),
  .MCSNOE2(mcsnoe_hi[2]),
  .MCSNOE1(mcsnoe_lo[1]),
  .MCSNOE0(mcsnoe_lo[0]),
) /* synthesis SPI_CLK_DIVIDER = "1" */;

defparam spiInst0.BUS_ADDR74 = "0b0000";
**iCE5LP (iCE40 Ultra) Hard Macros**

This section describes the following dedicated hard macro primitives available in iCE5LP (iCE40 Ultra) devices.

- SB_HFOSC
- SB_LFOSC
- SB_LED_DRV_CUR
- SB_RGB_DRV
- SB_IR_DRV
- SB_IO_OD
- SB_I2C
- SB_SPI
- SB_MAC16

### SB_HFOSC

SB_HFOSC primitive generates 48MHz nominal clock frequency within +/- 10% variation, with user programmable divider value of 1, 2, 4, and 8. The HFOSC can drive either the global clock network or fabric routes directly based on the clock network selection.

#### Ports

<table>
<thead>
<tr>
<th>Signal Name</th>
<th>Direction</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>CLKHFPFU</td>
<td>Input</td>
<td>Power up the HFOSC circuit. After power up, oscillator output will be stable after 100us. Active High.</td>
</tr>
<tr>
<td>CLKHFEN</td>
<td>Input</td>
<td>Enable the clock output. Enable should be low for the 100us power up period. Active High.</td>
</tr>
<tr>
<td>CLKFH</td>
<td>Output</td>
<td>HF Oscillator output.</td>
</tr>
</tbody>
</table>

#### Parameters

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Parameter Values</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>CLKFH_DIV</td>
<td>&quot;0b00&quot;</td>
<td>Sets 48MHz HFOSC output.</td>
</tr>
<tr>
<td></td>
<td>&quot;0b01&quot;</td>
<td>Sets 24MHz HFOSC output.</td>
</tr>
<tr>
<td></td>
<td>&quot;0b10&quot;</td>
<td>Sets 12MHz HFOSC output.</td>
</tr>
<tr>
<td></td>
<td>&quot;0b11&quot;</td>
<td>Sets 6MHz HFOSC output</td>
</tr>
</tbody>
</table>

#### Default Signal Values

The iCEcube2 software assigns the following signal value to unconnected port:

- Input CLKHFPFU: Logic "0"
- Input CLKHFEN: Logic "0"
Clock Network Selection
By default the oscillator use one of the dedicated clock networks in the device to drive the elements. The user may configure the oscillator to use the fabric routes instead of global clock network using the synthesis attribute.

Synthesis Attributes

```c
/* synthesis ROUTE_THROUGH_FABRIC = <value> */

Value:
0: Use dedicated clock network. Default option.
1: Use fabric routes.
```

Verilog Instantiation

```verilog
SB_HFOSC OSCInst0 (.
.CLKHFEN(ENCLKHF),
.CLKHFPU(CLKHF_POWERUP),
.CLKHF(CLKHF)
) /* synthesis ROUTE_THROUGH_FABRIC= [0|1] */;

defparam OSCInst0.CLKHF_DIV = "0b00";
```

\textbf{SB\_LFOSC}

SB\_LFOSC primitive generates 10 KHz nominal clock frequency within +/- 10\% variation. There is no divider on the LFOSC.

The LFOSC can drive either the global clock network or fabric routes directly based on the clock network selection.

Ports

<table>
<thead>
<tr>
<th>Signal Name</th>
<th>Direction</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>CLKLFPU</td>
<td>Input</td>
<td>Power up the LFOSC circuit. After power up, oscillator output will be stable after 100us. Active High.</td>
</tr>
<tr>
<td>CLKLFEN</td>
<td>Input</td>
<td>Enable the clock output. Enable should be low for the 100us power up period. Active High.</td>
</tr>
<tr>
<td>CLKLF</td>
<td>Output</td>
<td>LF Oscillator output.</td>
</tr>
</tbody>
</table>

Default Signal Values

The iCEcube2 software assigns the following signal value to unconnected port:

- Input CLKLFP: Logic “0”
- Input CLKLFP: Logic “0”
Clock Network Selection
By default the oscillator use one of the dedicated clock networks in the device to drive the elements. The user may configure the oscillator to use the fabric routes instead of global clock network using the synthesis attribute.

Synthesis Attributes

```verbatim
/* synthesis ROUTE_THROUGH_FABRIC = <value> */

Value:
0: Use dedicated clock network. Default option.
1: Use fabric routes.
```

Verilog Instantiation

```verbatim
SB_LFOSC OSCInst1 ( .CLKLFEN(ENCLKLF),
  .CLKLFPU(CLKLF_POWERUP),
  .CLKLF(CLKLF)
) /* synthesis ROUTE_THROUGH_FABRIC= [0|1] */;
```

**SB_LED_DRV_CUR**

SB_LED_DRV_CUR primitive generates the constant reference current required to power up the SB_RGB_DRV and SB_IR_DRV primitives.

![Image](image.png)

### Ports

<table>
<thead>
<tr>
<th>Signal Name</th>
<th>Direction</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>EN</td>
<td>Input</td>
<td>Enable to generate constant current source for SB_RGB_DRV and SB_IR_DRV primitives. After Enable, reference current value will be stable after 100us. Active High.</td>
</tr>
<tr>
<td>LEDPU</td>
<td>Output</td>
<td>Power up signal for SB_RGB_DRV and SB_IR_DRV primitives. This port should be connected only to RGBPU/IRPU pins of SB_RGB_DRV and SB_IR_DRV primitives.</td>
</tr>
</tbody>
</table>

Default Signal Values

The iCEcube2 software assigns the following signal value to unconnected port:

Input EN : Logic "0"
Verilog Instantiation

```verilog
SB_LED_DRV_CUR   LED_CUR_inst
  (.EN(enable_led_current),
   .LEDPU(led_power_up))
);
```

**SB_RGB_DRV**

SB_RGB_DRV primitive contains 3 dedicated open drain I/O pins for RGB LED outputs. Each of the RGB LED output is bonded out together with an SB_IO_OD primitive to the package pin. User can either use SB_RGB_DRV primitive or the SB_IO_OD primitive to drive the package pin, but not both.

The primitive allows configuration of each of the 3 RGB LED outputs individually. When the RGBx_CURRENT parameter of RGBx output is set to "0b000000", then SB_IO_OD can be used to drive the package pin.

![SB_RGB_DRV Diagram](image)

### Ports

<table>
<thead>
<tr>
<th>Signal Name</th>
<th>Direction</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>RGBLEDEN</td>
<td>Input</td>
<td>Enable the SB_RGB_DRV primitive. Active High.</td>
</tr>
<tr>
<td>RGBPU</td>
<td>Input</td>
<td>Power Up Signal. Connect to LEDPU port of SB_LED_DRV_CUR primitive.</td>
</tr>
<tr>
<td>RGB0PWM</td>
<td>Input</td>
<td>Input data to drive RGB0 LED pin. This input is usually driven from the SB_LEDD_IP.</td>
</tr>
<tr>
<td>RGB1PWM</td>
<td>Input</td>
<td>Input data to drive RGB1 LED pin. This input is usually driven from the SB_LEDD_IP.</td>
</tr>
<tr>
<td>RGB2PWM</td>
<td>Input</td>
<td>Input data to drive RGB2 LED pin. This input is usually driven from the SB_LEDD_IP.</td>
</tr>
<tr>
<td>RGB0</td>
<td>Output</td>
<td>RGB0 LED output.</td>
</tr>
<tr>
<td>RGB1</td>
<td>Output</td>
<td>RGB1 LED output.</td>
</tr>
<tr>
<td>RGB2</td>
<td>Output</td>
<td>RGB2 LED output.</td>
</tr>
</tbody>
</table>

### Default Signal Values

The iCEcube2 software assigns the following signal value to unconnected port:
- Input RGBLEDEN : Logic "0"
- Input RGB0PWM : Logic "0"
- Input RGB1PWM : Logic "0"
Input RGB2PWM : Logic "0"
Input RGBPU : Logic "0"

Parameters
The SB_RGB_DRV primitive contains the following parameter and their default values:

Parameter RGB0_CURRENT = "0b0000000";
Parameter RGB1_CURRENT = "0b0000000";
Parameter RGB2_CURRENT = "0b0000000";

Parameter values:
"0b0000000" = 0mA. // Set this value to use the associated SB_IO_OD instance at RGB LED location.
"0b0000001" = 4mA.
"0b0000011" = 8mA.
"0b0000111" = 12mA.
"0b0001111" = 16mA.
"0b0111111" = 24mA.

Verilog Instantiation
SB_RGB_DRV RGB_DRIVER (  
    .RGBLEDEN(ENABLE_LED),  
    .RGB0PWM(RGB0),  
    .RGB1PWM(RGB1),  
    .RGB2PWM(RGB2),  
    .RGBPU(led_power_up),  
    .RGB0(LED0),  
    .RGB1(LED1),  
    .RGB2(LED2)  
);  
defparam RGB_DRIVER.RGB0_CURRENT = "0b1111111";  
defparam RGB_DRIVER.RGB1_CURRENT = "0b1111111";  
defparam RGB_DRIVER.RGB2_CURRENT = "0b1111111";

SB_IR_DRV
SB_IR_DRV primitive contains a single dedicated open drain I/O pin for IRLED output. The IRLED output is bonded out together with an SB_IO_OD primitive to the package pin. User can either use SB_IR_DRV primitive or the SB_IO_OD primitive to drive the package pin, but not both.

When the IR_CURRENT parameter is set to "0b0000000000", then SB_IO_OD can be used to drive the package pin.
### Ports

<table>
<thead>
<tr>
<th>Signal Name</th>
<th>Direction</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>IRLEDDEN</td>
<td>Input</td>
<td>Enable the SB IR_DRV primitive. Active High.</td>
</tr>
<tr>
<td>IRPU</td>
<td>Input</td>
<td>Power Up Signal. Connect to LEDPU port of SB_LED_DRV_CUR primitive.</td>
</tr>
<tr>
<td>IRPWM</td>
<td>Input</td>
<td>PWM Input data to drive IRLED pin.</td>
</tr>
<tr>
<td>IRLED</td>
<td>Output</td>
<td>IR LED output.</td>
</tr>
</tbody>
</table>

### Default Signal Values

The iCEcube2 software assigns the following signal value to unconnected port:

- Input IRLEDDEN: Logic "0"
- Input IRPWM: Logic "0"

### Parameter

The SB_IR_DRV primitive contains the following parameter and their default values:

Parameter IR_CURRENT = "0b00000000000";

Parameter Values:

- "0b00000000000": 0mA. // Set this value to use the associated SB_IO_OD instance at // IR LED location.
- "0b00000000001": 50mA
- "0b00000000011": 100mA
- "0b00000000111": 150mA
- "0b00000001111": 200mA
- "0b00000011111": 250mA
- "0b00000111111": 300mA
- "0b00011111111": 350mA
- "0b01111111111": 400mA
- "0b11111111111": 450mA
- "0b11111111111": 500mA

### Verilog Instantiation

```verilog
SB_IR_DRV IRRVinst (  
  .IRLEDDEN(ENABLE_IRLED),  
  .IRPWM(IR_INPUT),  
  .IRPU(led_power_up),  
  .IRLED(IR_LED)  
);  
defparam IRRVinst.IR_CURRENT = "0b1111111111";
```
**SB_RGB_IP**

SB_RGB_IP primitive generates the 3 RGB PWM outputs, to be connected to the LED drivers.

![SB_RGB_IP block diagram]

<table>
<thead>
<tr>
<th>Ports</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>SB_RGB_IP Ports</strong></td>
</tr>
<tr>
<td><strong>Signal Name</strong></td>
</tr>
<tr>
<td>CLK</td>
</tr>
<tr>
<td>RST</td>
</tr>
<tr>
<td>PARAMSOK</td>
</tr>
<tr>
<td>RGBCOLOR[3:0]</td>
</tr>
<tr>
<td>BRIGHTNESS[3:0]</td>
</tr>
<tr>
<td>BREATHRAMP[3:0]</td>
</tr>
<tr>
<td>BLINKRATE[3:0]</td>
</tr>
<tr>
<td>REDPWM</td>
</tr>
<tr>
<td>GREENPWM</td>
</tr>
<tr>
<td>BLUEPWM</td>
</tr>
</tbody>
</table>

**Default Signal Values**

The iCEcube2 software assigns the logic “0” value to all unconnected input ports.

**Verilog Instantiation**

```verilog
SB_RGB_IP RGBPWMIP_inst(  .CLK (CLK),  .RST (RST), // Async rst  .PARAMSOK (PARAMSOK),  .RGBCOLOR (RGBCOLOR),  .BRIGHTNESS (BRIGHTNESS),  .BREATHRAMP (BREATHRAMP),  .BLINKRATE (BLINKRATE),  .REDPWM (REDPWM),  .GREENPWM (GREENPWM),  .BLUEPWM (BLUEPWM)
);
```
**SB_IO_OD**

The SB_IO_OD is the open drain IO primitive. When the Tristate output is enabled, the IO pulls down the package pin signal to zero. The following figure and Verilog template illustrate the complete user accessible logic diagram, and its Verilog instantiation.

**Ports**

<table>
<thead>
<tr>
<th>Signal Name</th>
<th>Direction</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>PACKAGEPIN</td>
<td>Bidirectional</td>
<td>Bidirectional IO pin.</td>
</tr>
<tr>
<td>LATCHINPUTVALUE</td>
<td>Input</td>
<td>Latches/Holds the input data.</td>
</tr>
<tr>
<td>CLOCKENABLE</td>
<td>Input</td>
<td>Clock enable signal.</td>
</tr>
<tr>
<td>INPUTCLK</td>
<td>Input</td>
<td>Clock for the input registers.</td>
</tr>
<tr>
<td>OUTPUTCLK</td>
<td>Input</td>
<td>Clock for the output registers.</td>
</tr>
<tr>
<td>OUTPUTENABLE</td>
<td>Input</td>
<td>Enable Tristate output. Active high.</td>
</tr>
<tr>
<td>DOUT0</td>
<td>Input</td>
<td>Data to package pin.</td>
</tr>
<tr>
<td>DOUT1</td>
<td>Input</td>
<td>Data to package pin.</td>
</tr>
<tr>
<td>DIN0</td>
<td>Output</td>
<td>Data from package pin.</td>
</tr>
<tr>
<td>DIN1</td>
<td>Output</td>
<td>Data from package pin.</td>
</tr>
</tbody>
</table>
Default Signal Values

The iCEcube2 software assigns the logic “0” value to all unconnected input ports except for CLOCKENABLE.
Note that explicitly connecting logic “1” value to port CLOCKENABLE will result in a non-optimal implementation, since extra LUT will be used to generate the Logic “1”. If the user’s intention is to keep the Input and Output registers always enabled, it is recommended that port CLOCKENABLE to be left unconnected.

Parameter Values

Parameter PIN_TYPE = 6'b000000;
// See Input and Output Pin Function Tables in SB_IO.
// Default value of PIN_TYPE = 6'b000000
Parameter NEG_TRIGGER = 1'b0;
// Specify the polarity of all FFs in the I/O to be falling edge when NEG_TRIGGER = 1. Default is 1'b0, rising edge.

Input and Output Pin Function Tables

Refer SB_IO Input and Output Pin Functional Table for the PIN_TYPE settings. Some of the output pin configurations are not applicable for SB_IO_OD primitive.

Verilog Instantiation

SB_IO_OD OpenDrainInst0

.PACKAGEPIN (PackagePin),
.LATCHINPUTVALUE (latchinputvalue),
.CLOCKENABLE (clockenable),
.INPUTCLK (inputclk),
.OUTPUTCLK (outputclk),
.OUTPUTENABLE (outputenable),
.DOUT0 (dout0),
.DOUT1 (dout1),
.DIN0 (din0),
.DIN1 (din1)
);
defparam OpenDrainInst0.PIN_TYPE = 6'b000000;
defparam OpenDrainInst0.NEG_TRIGGER = 1'b0;
**SB_I2C**

iCE5LP device supports two I2C hard IP primitives, located at upper left corner and upper right corner of the chip.

### Ports

The port interface is similar as ICE40LM SB_I2C primitive. Refer Page 127.

### Parameters

The parameters are same as ICE40LM SB_I2C primitive.

### Synthesis Attribute

**I2C_CLK_DIVIDER**

Synthesis attribute "I2C_CLK_DIVIDER" is used by PNR and STA tools for optimization and deriving the appropriate clock frequency at SCLO output with respect to the SBCLKI input clock frequency.

```
/* synthesis I2C_CLK_DIVIDER = Divide Value */
```

Divide Value: 0, 1, 2, 3 … 1023. Default is 0.

**SDA_INPUT_DELAYED**

SDA_INPUT_DELAYED attribute is used to add 50ns additional delay to the SDAI signal.

```
/* synthesis SDA_INPUT_DELAYED = value */
```

Value:
0: No delay.
1: Add 50ns delay. (Default value).

**SDA_OUTPUT_DELAYED**

SDA_OUTPUT_DELAYED attribute is used to add 50ns additional delay to the SDAO signal.

```c
/* synthesis SDA_OUTPUT_DELAYED = value */
```

Value:
0: No delay (Default value).
1: Add 50ns delay.

**SB_SPI**

iCE5LP device supports two SPI hard IP primitives, located at lower left corner and lower right corner of the chip. The port interface of SB_SPI is similar as ICE40LM SB_SPI primitive. Refer Page 130.

### Ports

The port interface is similar as iCE40LM SB_SPI primitive. Refer Page 130.

### Parameters

The parameters are same as ICE40LM SB_SPI primitive.

### Synthesis Attribute

The synthesis attribute is same as ICE40LM SB_SPI primitive.
**SB_MAC16**

The SB_MAC16 primitive is the dedicated configurable DSP block available in iCE5LP devices. The SB_MAC16 can be configured into a multiplier, adder, subtracter, accumulator, multiply-add and multiply-sub through the instance parameters. The SB_MAC16 blocks can be cascaded to implement wider functional units.

iCEcube2 2014.04 supports only 32 predefined SB_MAC16 functional configurations. Refer Page 151 for the list of supported configurations.
Ports

<table>
<thead>
<tr>
<th>Signal Name</th>
<th>Direction</th>
<th>Description</th>
<th>Default Values</th>
</tr>
</thead>
<tbody>
<tr>
<td>CLK</td>
<td>Input</td>
<td>Clock input. Applies to all clocked elements in the MAC16 Block.</td>
<td>1'b1</td>
</tr>
<tr>
<td>CE</td>
<td>Input</td>
<td>Clock Enable Input. Active High.</td>
<td>16'b0</td>
</tr>
<tr>
<td>C[15:0]</td>
<td>Input</td>
<td>Input to the C Register / Direct input to the adder accumulator.</td>
<td>16'b0</td>
</tr>
<tr>
<td>A[15:0]</td>
<td>Input</td>
<td>Input to the A Register / Direct input to the multiplier blocks /Direct input to the adder accumulator.</td>
<td>16'b0</td>
</tr>
<tr>
<td>B[15:0]</td>
<td>Input</td>
<td>Input to the B Register / Direct input to the multiplier blocks /Direct input to the adder accumulator.</td>
<td>16'b0</td>
</tr>
<tr>
<td>D[15:0]</td>
<td>Input</td>
<td>Input to the D Register / Direct input to the adder accumulator.</td>
<td>16'b0</td>
</tr>
<tr>
<td>A HOLD</td>
<td>Input</td>
<td>Hold A registers Data .Controls data flow into the input register A. Active High.</td>
<td>1'b0</td>
</tr>
</tbody>
</table>

0 Update (load) register at next active clock edge.
<p>| | | | |</p>
<table>
<thead>
<tr>
<th></th>
<th></th>
<th></th>
<th></th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>B HOLD</strong></td>
<td>Input</td>
<td>Hold B registers Data. Controls data flow into the B input register. Active High.</td>
<td>1'b0</td>
</tr>
<tr>
<td></td>
<td></td>
<td>0 Update (load) register at next active clock edge.</td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>1 Hold (retain) current register value, regardless of clock.</td>
<td></td>
</tr>
<tr>
<td><strong>C HOLD</strong></td>
<td>Input</td>
<td>Hold C registers Data. Controls data flow into the A input register. Active High.</td>
<td>1'b0</td>
</tr>
<tr>
<td></td>
<td></td>
<td>0 Update (load) register at next active clock edge.</td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>1 Hold (retain) current register value, regardless of clock.</td>
<td></td>
</tr>
<tr>
<td><strong>D HOLD</strong></td>
<td>Input</td>
<td>Hold D registers Data. Controls data flow into the A input register. Active High.</td>
<td>1'b0</td>
</tr>
<tr>
<td></td>
<td></td>
<td>0 Update (load) register at next active clock edge.</td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>1 Hold (retain) current register value, regardless of clock.</td>
<td></td>
</tr>
<tr>
<td><strong>IRST TOP</strong></td>
<td>Input</td>
<td>Reset input to the A and C input registers, and the pipeline registers in the upper half of the multiplier block. Active High</td>
<td>1'b0</td>
</tr>
<tr>
<td><strong>IRST BOT</strong></td>
<td>Input</td>
<td>Reset input to the B and C input registers, and the pipeline registers in the lower half of the multiplier block, and the 32-bit multiplier result pipeline register. Active High.</td>
<td>1'b0</td>
</tr>
<tr>
<td><strong>ORST TOP</strong></td>
<td>Input</td>
<td>Reset the high-order bits of the accumulator register ([31:16]). Active High.</td>
<td>1'b0</td>
</tr>
<tr>
<td><strong>ORST BOT</strong></td>
<td>Input</td>
<td>Reset the low-order accumulator register bits ([15:0]). Active High.</td>
<td>1'b0</td>
</tr>
<tr>
<td><strong>O LOAD TOP</strong></td>
<td>Input</td>
<td>High-order Accumulator Register Accumulate/Load. Controls whether the accumulator register accepts the output of the adder/subtractor or whether the register is loaded with the value from Input C (or Register C, if configured).</td>
<td>1'b0</td>
</tr>
<tr>
<td></td>
<td></td>
<td>0 Accumulator Register [31:16] loaded with output from adder/subtractor.</td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>1 Accumulator Register [31:16] loaded with Input C or Register C, depending on primitive parameter value.</td>
<td></td>
</tr>
<tr>
<td><strong>O LOAD BOT</strong></td>
<td>Input</td>
<td>Low-order Accumulator Register Accumulate/Load. Controls whether the low-order accumulator register bits (15:0) accepts the output of the adder/subtractor or whether the register is loaded with the value from Input D (or Register D, if configured).</td>
<td>1'b0</td>
</tr>
<tr>
<td></td>
<td></td>
<td>0 Accumulator Register [15:0] loaded with output from adder/subtractor.</td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>1 Accumulator Register [15:0] loaded with Input D or Register D, depending on primitive parameter value.</td>
<td></td>
</tr>
<tr>
<td><strong>ADD SUB TOP</strong></td>
<td>Input</td>
<td>High-order Add/Subtract. Controls whether the adder/subtractor adds or subtracts.</td>
<td>1'b0: Add</td>
</tr>
<tr>
<td></td>
<td></td>
<td>0 Add: W+X+HCI</td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>1 Subtract: W-X-HCI</td>
<td></td>
</tr>
<tr>
<td><strong>ADD SUB BOT</strong></td>
<td>Input</td>
<td>Low-order Add/Subtract. Controls whether the adder/subtractor adds or subtracts.</td>
<td>1'b0: Add</td>
</tr>
<tr>
<td></td>
<td></td>
<td>0 Add: W+X+HCI</td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>1 Subtract: W-X-HCI</td>
<td></td>
</tr>
</tbody>
</table>
### OHOLDTOP
**Input**
High-order Accumulator Register Hold. Controls data flow into the high-order ([31:16]) bits of the accumulator.

<table>
<thead>
<tr>
<th>Configuration</th>
<th>Description</th>
<th>Values</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>Update (load) register at next active clock edge.</td>
<td>All the registers are rising_edge triggered.</td>
</tr>
<tr>
<td>1</td>
<td>Hold (retain) current register value, regardless of clock.</td>
<td>All the registers are falling_edge triggered.</td>
</tr>
</tbody>
</table>

### OHOLDBOT
**Input**
Low-order Accumulator Register Hold. Controls data flow into the high-order ([15:0]) bits of the accumulator.

<table>
<thead>
<tr>
<th>Configuration</th>
<th>Description</th>
<th>Values</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>Update (load) register at next active clock edge.</td>
<td>All the registers are rising_edge triggered.</td>
</tr>
<tr>
<td>1</td>
<td>Hold (retain) current register value, regardless of clock.</td>
<td>All the registers are falling_edge triggered.</td>
</tr>
</tbody>
</table>

### CI
**Input**
Carry/borrow input from lower logic tile.

### ACCUMCI
**Input**
Cascade Carry/borrow input from lower MAC16 block.

### SIGNEXTIN
**Input**
Sign extension input from lower MAC16 block.

### O[31:0]
**Output**
32 bit MAC16 Output.

<table>
<thead>
<tr>
<th>Configuration</th>
<th>Description</th>
<th>Values</th>
</tr>
</thead>
<tbody>
<tr>
<td>O[31:0]</td>
<td>32-bit result of a 16x16 multiply operation or a 32-bit adder/accumulate function.</td>
<td>All the registers are rising_edge triggered.</td>
</tr>
<tr>
<td>O[31:16]</td>
<td>16-bit result of an 8x8 multiply operation or a 32-bit adder/accumulate function.</td>
<td>All the registers are falling_edge triggered.</td>
</tr>
<tr>
<td>O[15:0]</td>
<td>16-bit result of an 8x8 multiply operation or a 32-bit adder/accumulate function.</td>
<td>All the registers are falling_edge triggered.</td>
</tr>
</tbody>
</table>

### CO
**Output**
Carry/borrow output to higher logic tile.

### ACCUMCO
**Output**
Cascade Carry/borrow output to higher MAC16 block.

### SIGNEXTOUT
**Output**
Sign extension output to higher MAC16 block.

### Parameters
The parameter table below shows the list of parameters to configure the SB_MAC16 block. This table also maps the parameter to the configuration bits shown in the SB_MAC16 Functional diagram.

<table>
<thead>
<tr>
<th>Parameter Name</th>
<th>Configuration bits</th>
<th>Parameter Description</th>
<th>Parameter Values</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>NEG_TRIGGER</td>
<td></td>
<td>Controls input clock polarity</td>
<td>0</td>
<td>All the registers are rising_edge triggered.</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>1</td>
<td>All the registers are falling_edge triggered.</td>
</tr>
<tr>
<td>C_REG</td>
<td>C0</td>
<td>Input C register Control.</td>
<td>0</td>
<td>Input C not registered</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>1</td>
<td>Input C registered</td>
</tr>
<tr>
<td>A_REG</td>
<td>C1</td>
<td>Input A register Control.</td>
<td>0</td>
<td>Input A not registered</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>1</td>
<td>Input A registered</td>
</tr>
<tr>
<td>B_REG</td>
<td>C2</td>
<td>Input B register Control.</td>
<td>0</td>
<td>Input B not registered</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>1</td>
<td>Input B registered</td>
</tr>
<tr>
<td>D_REG</td>
<td>C3</td>
<td>Input D register Control.</td>
<td>0</td>
<td>Input D not registered</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>1</td>
<td>Input D registered</td>
</tr>
<tr>
<td>TOP_8x8_MULTI_REG</td>
<td>C4</td>
<td>Top 8x8 multiplier output register control (point F)</td>
<td>0</td>
<td>Top 8x8 multiplier output is not registered.</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>1</td>
<td>Top 8x8 multiplier output is registered.</td>
</tr>
<tr>
<td>BOT_8x8_MULTI_REG</td>
<td>C5</td>
<td>Bottom 8x8 multiplier</td>
<td>0</td>
<td>Bottom 8x8 multiplier</td>
</tr>
<tr>
<td>Register Description</td>
<td>Control Bit(s)</td>
<td>Function</td>
<td></td>
<td></td>
</tr>
<tr>
<td>----------------------</td>
<td>---------------</td>
<td>----------</td>
<td></td>
<td></td>
</tr>
<tr>
<td>output register control. (point G)</td>
<td>C6</td>
<td>0: Intermediate 8x8 multiplier pipeline register controls (points J and K). These multipliers are only used for 16x16 multiply operations. For 8x8 multiply operations, set C6 and C7 to 1, which reduces power consumption. 1: Intermediate 8x8 multiplier outputs are registered.</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Bottom 8x8 multiplier output is not registered.</td>
<td>1</td>
<td>Bottom 8x8 multiplier output is registered.</td>
<td></td>
<td></td>
</tr>
<tr>
<td>PIPELINE_16x16_MULT_REG1</td>
<td>C6</td>
<td>0: Intermediate 8x8 multiplier outputs are not registered. 1: Intermediate 8x8 multiplier outputs are registered.</td>
<td></td>
<td></td>
</tr>
<tr>
<td>PIPELINE_16x16_MULT_REG2</td>
<td>C7</td>
<td>0: 32-bit output from 16x16 multiplier is not registered. 1: 32-bit output from 16x16 multiplier is registered.</td>
<td></td>
<td></td>
</tr>
<tr>
<td>TOPOOUTPUT_SELECT</td>
<td>C9,C8</td>
<td>00: 16-bit output of Multiplexer P, from top adder/subtractor. 01: 16-bit output from upper accumulator register, Q. 10: 16-bit output from upper 8x8 multiplier, F. 11: Upper 16-bit output from 16x16 multiplier, H.</td>
<td></td>
<td></td>
</tr>
<tr>
<td>TOPADDSUB_LOWERINPUT</td>
<td>C11,C10</td>
<td>00: 16-bit input from A input or associated input register. 01: 16-bit output from upper 8x8 multiplier, F. 10: Upper 16-bit output from 16x16 multiplier, H. 11: Sign extension input from lower adder/subtractor, Z[15]. Duplicate 16 bits.</td>
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<td>TOPADDSUB_UPPERINPUT</td>
<td>C12</td>
<td>0: 16-bit feedback from upper accumulator register, Q. 1: 16-bit input from C input or associated pipeline register.</td>
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<td>TOPADDSUB_CARRYSELECT</td>
<td>C14,C13</td>
<td>00: Constant 0. 01: Constant 1. 10: Cascade Carry/borrow output from lower adder/subtractor. 11: Carry/borrow output from lower adder/subtractor.</td>
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| BOTOUTPUT_SELECT | C16,C15 | 00: 16-bit output of multiplexer R from lower adder/subtractor. 01: 16-bit output from lower accumulator register, S. 10: 16-bit output from lower 8x8 multiplier.
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<tr>
<th>Feature</th>
<th>Code</th>
<th>Description</th>
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<tr>
<td>BOTADDSUBLOWERINPUT</td>
<td>C18,C17</td>
<td>Selects Input Z for the lower adder/subtractor</td>
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<td>16-bit input from B input or associated pipeline register</td>
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<td>16-bit output from lower 8x8 multiplier, G</td>
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<td>Lower 16-bit output from 16x16 multiplier, H</td>
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<td>Sign extension input SIGNEXTIN. Duplicate 16 bits.</td>
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<td>BOTADDSUBCARRYSELECT</td>
<td>C21,C20</td>
<td>Carry/borrow input select to lower adder/subtractor</td>
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<td>Carry/borrow input from CI</td>
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<tr>
<td>MODE_8x8</td>
<td>C22</td>
<td>Selects 8x8 Multiplier mode and 8x8 Low-Power Multiplier Blocking Option</td>
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<tr>
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<td>0</td>
<td>No effect</td>
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<td></td>
<td>1</td>
<td>Selects 8x8 Multiplier mode. Holds the pipelining registers associate with a 16x16 multiplier in clock disable mode. Helps reduce the dynamic power consumption within the multiplier function. Used in conjunction with C6, C7 settings.</td>
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<td>A_SIGNED</td>
<td>C23</td>
<td>Indicates whether multiplier input A is signed or unsigned. Applies regardless if input A is 16-or 32-bits wide.</td>
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<td>Multiplier input A is signed.</td>
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<tr>
<td>B_SIGNED</td>
<td>C24</td>
<td>Indicates whether multiplier input B is signed or unsigned. Applies regardless if input B is 16-or 32-bits wide.</td>
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SB_MAC16 Configurations

The following SB_MAC16 functional blocks are supported in iCEcube2 2014.08.

1. Multiplier.
2. Multiply and Accumulate (MAC).
3. Accumulator (ACC).
4. Add/Subtract (ADD/SUB).
5. Multiply and Add/Subtract (MULTADDSUB)

The valid configuration parameter settings for each functional block are listed below.

Table 1 : Multiplier Configurations

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<tr>
<th>SB_MAC16 Function/Parameter Settings</th>
<th>B_SIGNED</th>
<th>A_SIGNED</th>
<th>MODE_8x8</th>
<th>BOTADDSUB_CARRYSELECT</th>
<th>BOTADDSUB_UPPERINPUT</th>
<th>BOTADDSUB_LOWERINPUT</th>
<th>BOTOUTPUT_SELECT</th>
<th>TOPADDSUB_CARRYSELECT</th>
<th>TOPADDSUB_UPPERINPUT</th>
<th>TOPADDSUB_LOWERINPUT</th>
<th>TOPOUTPUT_SELECT</th>
<th>PIPELINE_16x16_MULT_REG2</th>
<th>PIPELINE_16x16_MULT_REG1</th>
<th>PIPELINE_8x8_MULT_REG</th>
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Table 2: MAC Configurations

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Table 5: Multiply Add/Subtract Configurations
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Verilog Instantiation

SB_MAC16 \text{i}_{\text{sbmac16}} \{
\begin{array}{l}
\text{.A}(A_{\text{i}}), \\
\text{.B}(B_{\text{i}}), \\
\text{.C}(C_{\text{i}}), \\
\text{.D}(D_{\text{i}}), \\
\text{.O}(O), \\
\text{.CLK}(\text{SYSCLK}_{\text{i}}), \\
\text{.CE}(\text{CE}_{\text{i}}), \\
\text{.IRSTTOP}(\text{RST}_{\text{i}}), \\
\text{.IRSTBOT}(\text{RST}_{\text{i}}), \\
\text{.AHOLD}(\text{AHOLD}_{\text{i}}), \\
\text{.BHOLD}(\text{BHOLD}_{\text{i}}), \\
\text{.CHOLD}(\text{CHOLD}_{\text{i}}), \\
\text{.DHALD}(\text{DHOLD}_{\text{i}}), \\
\text{.OHOLDTOP}(\text{HLDTOPOUT}_{\text{i}}), \\
\text{.OHOLDBOT}(\text{HLDBOTOUT}_{\text{i}}), \\
\text{.LOADTOP}(\text{LOADTOP}_{\text{i}}), \\
\text{.LOADBOT}(\text{LOADBOT}_{\text{i}}), \\
\text{.ADDSUBTOP}(\text{ADDSUBTOP}_{\text{i}}), \\
\text{.ADDSUBBOT}(\text{ADDSUBBOT}_{\text{i}}), \\
\text{.CO}(\text{CO}), \\
\text{.CI}(\text{CI}), \\
\text{//MAC cascading ports.} \\
\text{.ACCUMCI()}, \\
\text{.ACCUMCO()}, \\
\text{.SIGNEXTIN()}, \\
\text{.SIGNEXTOUT()} \\
\end{array}
\}

defparam \text{i}_{\text{sbmac16}}. \text{C}_{\text{REG}} = 1'b0 ; \\
defparam \text{i}_{\text{sbmac16}}. \text{A}_{\text{REG}} = 1'b0 ; \\
defparam \text{i}_{\text{sbmac16}}. \text{B}_{\text{REG}} = 1'b0 ; \\
defparam \text{i}_{\text{sbmac16}}. \text{D}_{\text{REG}} = 1'b0 ; \\
defparam \text{i}_{\text{sbmac16}}. \text{TOP}_{8\times8} \text{MULT}_{\text{REG}} = 1'b0 ; \\
defparam \text{i}_{\text{sbmac16}}. \text{BOT}_{8\times8} \text{MULT}_{\text{REG}} = 1'b0 ; \\
defparam \text{i}_{\text{sbmac16}}. \text{PIPELINE}_{16\times16} \text{MULT}_{\text{REG}1} = 1'b0 ; \\
defparam \text{i}_{\text{sbmac16}}. \text{PIPELINE}_{16\times16} \text{MULT}_{\text{REG}2} = 1'b0 ; \\
defparam \text{i}_{\text{sbmac16}}. \text{TOPOUTPUT}_{\text{SELECT}} = 2'b10 ; \\
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defparam \text{i}_{\text{sbmac16}}. \text{TOPADDSUB}_{\text{UPPER}_{\text{INPUT}}} = 1'b0 ; \\
defparam \text{i}_{\text{sbmac16}}. \text{TOPADDSUB}_{\text{CARRYSELECT}} = 2'b00 ; \\
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defparam \text{i}_{\text{sbmac16}}. \text{MODE}_{8\times8} = 1'b1 ; \\
defparam \text{i}_{\text{sbmac16}}. \text{A}_{\text{SIGNED}} = 1'b0 ; \\
defparam \text{i}_{\text{sbmac16}}. \text{B}_{\text{SIGNED}} = 1'b0 ;
Device Configuration Primitives

**SB_WARMBOOT**

iCE FPGA devices permit the user to load a different configuration image during regular operation. Through the use of the Warm Boot Primitive, the user can load one of 4 pre-defined configuration images into the iCE FPGA device.

*Note that this Warm Boot mode is different from the Cold Boot operation, which is executed during the initial device boot-up sequence.*

![SB_WARMBOOT Diagram]

The selection of one of these 4 images is accomplished through 2 input signals, S1 and S0. In order to trigger the selection of a new image, an additional signal, BOOT, is provided. It should be noted that this signal is level-triggered, and should be used for every Warm Boot operation i.e. every time the user wishes to load a new image into the device.

The successful instantiation of this primitive also requires the user to specify the address locations of the 4 images. These addresses should be specified in the iCEcube2 software as per the Warm Boot Application Note.

**Verilog Instantiation**

```verilog
SB_WARMBOOT my_warmboot_i (  
    .BOOT (my_boot),          // Level-sensitive trigger signal  
    .S1 (my_sell),            // S1, S0 specify selection of the  
    .S0 (my_sel0)             // configuration image
);
```