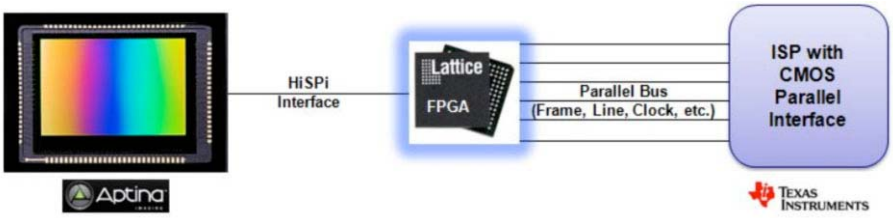
HiSPi-to-Parallel Sensor Bridge

April 2014 Reference Design RD1120

Introduction

The HiSPi-to-Parallel Sensor Interface Bridge is designed to convert an Aptina sensor delivering HiSPi (High-Speed Serial Pixel) serial data to a traditional parallel data bus. The parallel data bus is designed to be compatible with standard ISP (Image Signal Processing) devices (see Figure 1). This reference design covers all normal HiSPi operating modes including Packetized-SP, Streaming-SP, Streaming-S and ActiveStart SP8, as defined in HiSPi Protocol v1.00.00. In addition, the reference design also supports the HDR (High Dynamic Range) operating mode defined in TN-09-215: HiSPi Protocol Specification for the MT9M024 and other Aptina sensors.

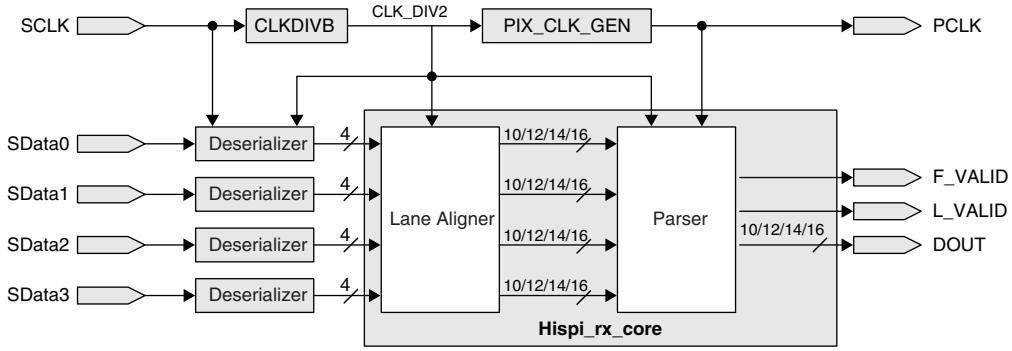
Figure 1. HiSPi-to-Parallel Sensor Bridge Overview



Functional Description

The HiSPi bridge can accept up to four differential serial lanes. Normally two or four lanes are used. As shown in Figures 2 and 3, each serial data lane in the Lattice FPGA is sampled and converted to a 4-bit or 8-bit wide interface by using a dedicated IDDR (Input Double Data Rate) element with x2 or x4 gearing respectively. The Lane Aligner performs the word and lane alignment according to the selected HiSPi mode. The Parser decodes lines, frames and converts them to the parallel data format. The parallel output includes a pixel clock, frame valid and line valid signals as well as a data bus, which is compatible with most in-system programmable devices. Parallel output signals can be configured to LVCMOS18, LVCMOS25 or LVCMOS33 (1.8V, 2.5V or 3.3V respectively). Even though the linear mode (normal operating mode) and the HDR operating mode are combined into a single packet in this reference design, they are illustrated separately for reference.

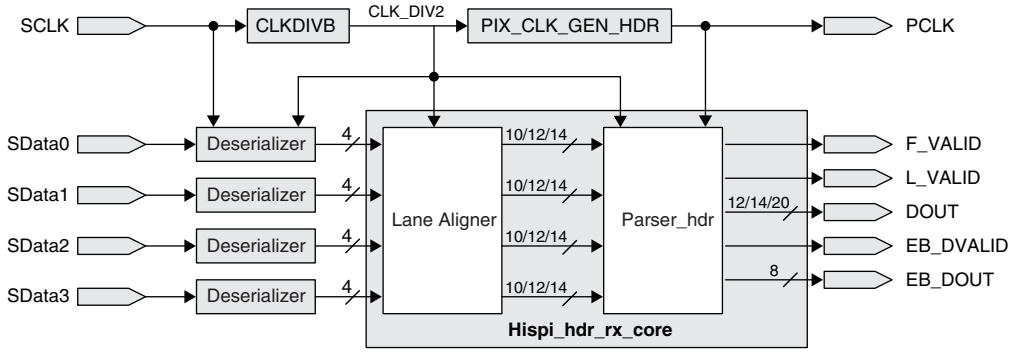
Figure 2. HiSPi-to-Parallel Sensor Bridging Block Diagram (Normal Operating Mode)



Features of the normal operating mode:

- Supports HiSPi formats Packetized-SP, Streaming-SP, Streaming-S and ActiveStart – SP8
- Supports lane number range from one to four
- Supports output parallel bit widths of 10, 12, 14 or 16 bits

Figure 3. HiSPi-to-Parallel Sensor Bridging Block Diagram (HDR Operating Mode)



Features of the HDR operating mode:

- Supports all the HDR operating modes introduced in TN-09-215: 20-bit over 4 lanes; 12/14 bits over 3 lanes; 12 bits over two lanes or 14 bits over two lanes
- Pixel data extraction for the selected mode
- Embedded data extraction for the selected mode

Parameter Settings

Table 1. Configurable Parameters

Parameter	Range/Options	Default
pmi_family	“XP2” “XO2” “XO3L” “ECP3” “ECP5”	“XO2”
c_HDR_MODE[1]	“true” “false”	“false”
c_HISPI_MODE[2]	“Packetized-SP” “Streaming-SP” “Streaming-S” “ActiveStart-SP8”	“Packetized-SP”
c_WORD_WIDTH[3]	10/12/14/16/20	12
c_LANE_WIDTH[4]	1/2/3/4	4
c_BRIDGES[5]	Reserved	1
c_3D	Reserved	“none”
pix_per_ln[6]	0 to 2^12-1	1080
FLR_enable[7]	0/1	0

1. If parameter c_HDR_MODE is set to “true”, the HDR operating mode is selected, otherwise the normal operating mode is selected.
2. Parameter c_HISPI_MODE is only used in normal operating mode.
3. 10/12/14/16 are available for normal operating mode. Options 12/14/20 are available for the HDR operating mode.
4. In HDR operating mode, the formats listed in Table 2 are supported.
5. MachXO2 only. Defines the number of bridges to initiate.
6. pix_per_ln is an input bus to the bridge core. It defines the number of pixels per active horizontal line. Used for all modes except Packetized-SP.
7. Adds a latency of c_LANE_WIDTH to the active space readout. Set to 0 for most cases.

Table 2. Supported Formats in HDR Operating Mode

c_WORD_WIDTH	c_LANE_WIDTH	Description
20 bits	4	20 bits over 4 lanes
12 bits	3	12 bits over 3 lanes
14 bits	3	14 bits over 3 lanes
12 bits	2	12 bits over 2 lanes
14 bits	2	14 bits over 2 lanes

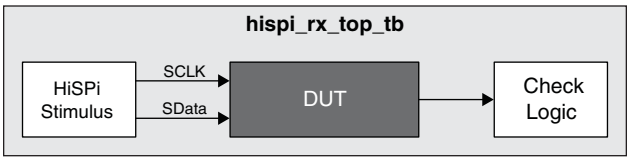
Table 3. HiSPi-to-Parallel Sensor Interface Bridge I/Os

Signal Name	Definition	Direction
rstn	Sensor Bridge reset, active low	Input
sclk	HiSPi serial differential clock	Input
sdata [0]	HiSPi serial differential data; Lane 1	Input
sdata [1]	Lane 2	
sdata [2]	Lane 3	
sdata [3]	Lane 4	
pclk	Pixel clock	Output
f_valid	Field valid indication	Output
l_valid	Line valid indication	Output
dout [c_WORD_WIDTH-1:0]	Pixel data	Output
Reset to sensor	Reset for sensor	Output

Test Bench Description

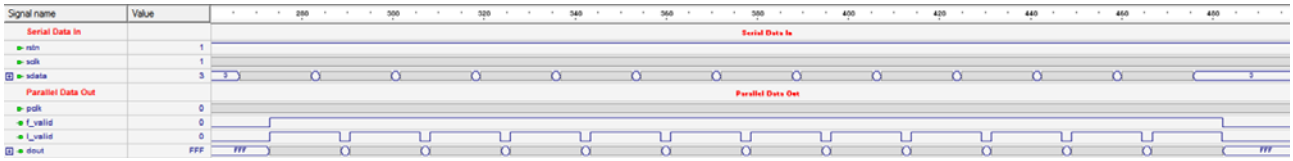
A behavioral simulation is also included in the reference design. The simulation is supports both the ModelSim and Active-HDL environments. For either environment, set the simulator's working directory to the location of the .do script and execute it. If Lattice Diamond® is not installed in the default directory, update the macro definition LATTICE_SRC in the script file manually.

Figure 4. Simulation Structure for the HiSPi-to-Parallel Sensor Bridge



The simulation is supported for both the ModelSim and Active-HDL simulators. For each simulator, set the simulator's working directory to the location of the .do script and then execute the .do script. If Lattice Diamond™ is not installed in the default directory, update the macro definition LATTICE_SRC in the script file manually.

Figure 5. Simulation of HiSPi Bridge (Frame with Reduced Line Size)



Implementation

Table 4. Performance and Resource Utilization[1]

Device Family	HiSPi Mode	Word Width	Lane Width	Registers		LUTs		EBRs	PLL
				LSE	Syn	LSE	Syn		
MachXO3L [6]	Packetized-SP	12	2	430	430	340	336	2	1
	Packetized-SP	12	4	711	711	545	541	4	1
	Packetized-SP	16	4	859	859	550	546	5	1
	Streaming-SP	16	4	787	787	550	546	5	1
MachXO2™ [2]	Packetized-SP	12	2	392		340		2	1
	Packetized-SP	12	4	673		511		4	1
	Packetized-SP	14	2	420		370		2	1
	Packetized-SP	14	4	721		623		4	1
	Streaming-SP	12	2	362		300		2	1
	Streaming-SP	12	4	614		500		4	1
	Streaming-SP	14	2	386		349		2	1
	Streaming-SP	14	4	657		606		4	1
	HDR	20	4	773		589		3	1
LatticeXP2™ [3]	Packetized-SP	12	2	311		295		1	1
	Packetized-SP	12	4	514		499		2	1
	Packetized-SP	14	2	347		312		1	1
	Packetized-SP	14	4	580		550		2	1
	Streaming-SP	12	2	283		194		1	1
	Streaming-SP	12	4	458		478		2	1
	Streaming-SP	14	2	315		315		1	1
	Streaming-SP	14	4	516		532		2	1
	HDR	20	4	577		477		2	1
ECP5™ [5]	Packetized-SP	12	2	316		315		1	1
	Packetized-SP	12	4	540		546		2	1
	Packetized-SP	14	2	350		384		1	1
	Packetized-SP	14	4	611		634		2	1
	Streaming-SP	12	2	289		309		1	1
	Streaming-SP	12	4	487		537		2	1
	Streaming-SP	14	2	322		330		1	1
	Streaming-SP	14	4	543		568		2	1
	HDR	20	4	624		540		2	1

1. Packetized-SP and Streaming-SP linear modes are provided in NGO format. For other modes, visit the Lattice sensor bridge web page at www.latticesemi.com/solutions/solutions/sensor bridge or visit the Aptina HiSPi to Parallel Sensor Bridge page www.latticesemi.com/en/Products/DesignSoftwareAndIP/IntellectualProperty/ReferenceDesigns/ReferenceDesigns01/AptinaHiSPitoParallelSensorBridge to create a custom HiSPi bridge.
2. Resource utilization characters are generated using LCMXO2-4000HE-6MG132C with Lattice Diamond 1.4 design software. When using this design in a different device, the utilization may vary.
3. Resource utilization characters are generated using LFXP2-8E-7M132C with Lattice Diamond 1.1 design software. When using this design in a different device, the utilization may vary.
4. Resource utilization in a LatticeECP3 device will be similar to the LatticeXP2 implementation.
5. Resource utilization characters are generated using LFE5UM-85F-8MG400C with Lattice Diamond 3.0 design software. When using this design in a different device, the utilization may vary.
6. Resource utilization characters are generated using LCMXO3L-4300C-6BG256C with the x4 gearing mode on Lattice Diamond 3.1 design software. When using this design in a different device or the x2 gearing mode, the utilization may vary. Diamond 3.1 users will need to install a patch to enable the x4 gearing mode on MachXO3L. To get the patch, please send your request to techsupport@latticesemi.com.

Table 5. I/O Timing Analysis of Serial Data Lanes

	Setup (ns)	Hold (ns)	Setup (ns)	Hold (ns)	Setup (ns)	Hold (ns)
MachXO3L[4]	Speed Grade 4		Speed Grade 5		Speed Grade 6	
	-	-	-0.472	1.012	-0.387	0.788
MachXO2[1]	Speed Grade 4		Speed Grade 5		Speed Grade 6	
	0.248	0.292	0.246	0.223	0.243	0.158
LatticeXP2[2]	Speed Grade 5		Speed Grade 6		Speed Grade 7	
	-0.272	0.447	-0.268	0.380	-0.263	0.317
ECP5[3]	Speed Grade 8		Speed Grade 6		Speed Grade 7	
	-0.104	0.481	-0.268	0.380	-0.263	0.317

1. Timing parameters are generated using LCMXO2-4000HE-6MG132C with Lattice Diamond 1.4 design software.
2. Timing parameters are generated using LFXP2-8E-7M132C with Lattice Diamond 1.4 design software.
3. Timing parameters are generated using LFE5UM-85F-8MG400C with Lattice Diamond 3.0 design software.
4. Timing parameters are generated for LCMXO3L-4300C-6BG256C on Lattice Diamond 3.1 design software.

Table 6. Aptina Sensor Bridge Recommended Pinout for LatticeXP2-5/8, LatticeXO2-1200/2000/4000 and LatticeXO3L-2100/4300/6900 FPGAs

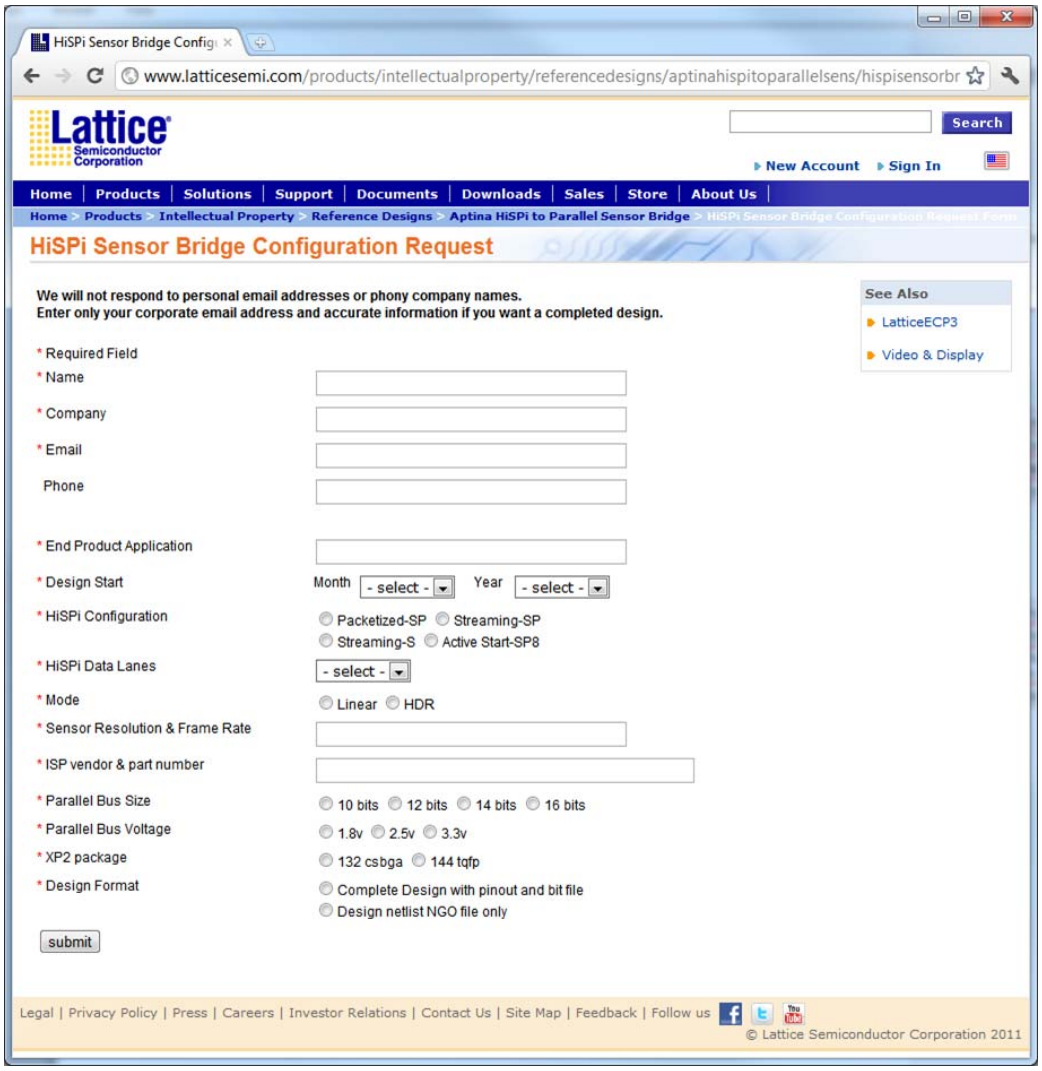
Signal Name	LatticeXP2 132-csBGA Pin	MachXO2 132-csBGA Pin	MachXO3L BG256 Pin
rstn_to_sensor 1	B9	F2	G3
rstn_to_bridge 2	F12	C1	E2
sclk_p	H1	N6	T7
sclk_n	H3	P6	R8
sdata_p [0]	D2	M11	P12
sdata_n [0]	E3	P12	T13
sdata_p [1]	D1	P8	R9
sdata_n [1]	E1	M8	T10
sdata_p [2]	H2	P2	P4
sdata_n [2]	G3	N2	T4
sdata_p [3]	L1	M7	T9
sdata_n [3]	L3	N8	P9
pclk	P2	A11	B11
f_valid	P14	B7	A8
l_valid	P13	C4	B6
dout [0]	N8	C6	C7
dout [1]	M6	B3	B5
dout [2]	M5	C11	C11
dout [3]	M7	A12	B12
dout [4]	N12	A7	C8
dout [5]	N7	B5	B7
dout [6]	P12	A9	A10
dout [7]	P5	A10	A11
dout [8]	P6	A2	C4
dout [9]	N2	B12	A12
dout [10]	P7	C12	C12
dout [11]	N4	B13	A13

1. rstn_to_sensor is used in the top level design to reset the Aptina sensor, but is not part of the sensor bridge itself. It is recommended to connect the reset pin for sensor control in your design.
2. rstn_to_bridge controls a reset counter in our top level design. This is done to remove debounce and ensure the sensor and bridge have been completely restarted. After reset the sensor is held Idle before programming the sensor via I^2C. The top level design holds the sensor and bridge in reset for ~2.5 seconds. The sensor is then programmed after an additional ~2.5 seconds.

To request a reference design meeting your specific design requirements visit the Lattice Semiconductor website and complete the HiSPi Sensor Bridge Configuration Request form.

www.latticesemi.com/products/intellectualproperty/referencedesigns/aptinahispitoparallelsens/hispisensorbridge-configur.cfm

Figure 6. HiSPi Sensor Bridge Request Form



Hardware Validation

The HiSPi-to-Parallel Sensor Bridge reference design has been hardware tested using the HDR-60 and an interface board to the Aptina MT9M024 sensor. In addition, the Texas Instruments 812X IP Network Camera uses this bridge with the Aptina J003 sensor.

References

- HiSPi Protocol v1.00.00
- TN-09-215: HiSPi Protocol Specification for the MT9M023 and MT9M033 Introduction

Technical Support Assistance

e-mail: techsupport@latticesemi.com

Internet: www.latticesemi.com

Revision History

Date	Version	Change Summary
April 2011	01.0	Initial release.
December 2011	01.1	Updated for MachXO2 and added pinout table.
July 2013	01.2	Updated for Sapphire.
		Updated the Performance and Resource Utilization and the I/O Timing Analysis of Serial Data Lanes tables.
		Updated document with new corporate logo.
		Updated Technical Support Assistance information.
April 2014	01.3	Updated Table 1, Configurable Parameters.
		Updated Sapphire device to ECP5 device.
		Added support for MachXO3L device.