Sil9437/Sil9438 Product Qualification Summary

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STANDARD QUALIFICATION AND REFERENCE DOCUMENTS

Table#1

Description	Abv.	reference	Condition	Test Intervals	Sample Size
High Temperature Operating Life	HTOL	JESD22-A108	Tj=Not to exceed 150°C at 1.1XVdd For 1000 hours	0, 168, 500 & 1000 Hrs	1 lot x 77 units
Human Body Model	HBM	JS-001-2014	+/- 2000V	Before & after stress	1 lot x 3units
Charge Device Model	CDM	JS-002-2014	+/- 500V	Before & after stress	1 lot x 3units
Machine Model	MM	JESD22-A115	+/- 200V	Before & after stress	1 lot x 3units
Latch Up	LU	JESD78	200mA Current injection & power supply overvoltage tests	Before & after stress	1 lot x 3units
Preconditioning before: THB, HAST, TC, & UHAST	PC	IPC/JEDEC J-STD-020D.1/JESD22-A113	JEDEC MSL Level 3 Reflow Peak Temp 260 °C	Before & after stress with C-Sam on 100% Units	1 lot x 231 units
High Temperature Storage Life	HTSL	JESD22-A103	150 °C for 1000 Hrs	0, 168, 500 & 1000 Hrs	1 lots x 77 units
Accelerated Moisture Resistance - unbiased HAST	uHAST	JESD22-A102	130 ºC / 85% R.H / 33.3 psia for 96Hrs	0, 96 Hrs	1 lot x 77 units
Temperature-Humidity-Bias Life Test	THBT	JESD22-A101	85ºC/85% RH with bias 1000 Hrs	0, 168, 500 & 1000Hrs	1 lots x 77 units
Temperature Cycling	TCT	JESD22-A104	-65 ºC to +150 ºC 1000 cycles	0, 500 & 1000 cycles	1 lot x 77 unit

TECHNOLOGY QUALIFICATION DATA FOR SII9437/SII9438 PRODUCT

Product Family: SiI9437/SiI9438
Packages offered: 32 QFN
Process Technology Fab: TSMC Fab14
Process Technology Node: 130nm GP Process
Wafer Size: 8 inches
Die Size: X: 2.220mm; Y: 2.120mm

PRODUCT LIFE (HTOL) DATA

1.1 High Temperature Operating Life (HTOL) Test:

The High Temperature Operating Life test is used to thermally accelerate those wear out and failure mechanisms that would occur as a result of operating the device continuously in a system application. Consistent with JESD22-A108 "Temperature, Bias, and Operating Life", the device is continuously exercised at specified voltages.

Life Test (HTOL) Conditions:
Stress Duration: 1000 hours
Stress Conditions: Max operating supplies, Ambient = 125°C
Method: JESD22-A108D

		168hrs			500hrs			1000hrs		
Rev. ID	Lot #	Rej.	Qty.	Note	Rej.	Qty.	Note	Rej.	Qty.	Note
0.0	P6V65.6Q	0	78		0	78		0	N/A	
0.1	P6V654.8	0	79		0	79		0	79	
	Total	0	157		0	157		0	79	

PRODUCT LIFE CALCULATION DATA

Cumulative Life Testing Device Hours = 118,000
FIT Rate = 99.8 FIT
FIT Assumptions: CL=60%, AE=0.7eV, Tjref=55C

ESD AND LATCH UP DATA

1.2 Electrostatic Discharge-Human Body Model:

The SiI9437/SiI9438 product was tested per the JS-001-2014 Electrostatic Discharge (ESD) Sensitivity Testing Human Body Model (HBM) standard.

All units were tested at room ambient prior to and after reliability stress. No failures were observed within the passing classification.

SiI9437/SiI9438 ESD-HBM:

Rev. ID	Lot #	Voltage Level	Rej.	Qty.	Note
0.0	P6V65.6Q	2000V	0	3	
0.1	P6V654.8	2000V	0	3	

HBM classification per JS-001-2014 is CLASS 2.
All HBM levels indicated are dual-polarity (±).

1.3 Electrostatic Discharge-Machine Model:

The SiI9437/SiI9438 product was tested per the JESD22-A115C Electrostatic Discharge (ESD) Sensitivity Testing Machine Model (MM) standard.

All units were tested at room ambient prior to and after reliability stress. No failures were observed within the passing classification.

SiI9437/SiI9438 ESD MM:

Rev. ID	Lot #	Voltage Level	Rej.	Qty.	Note
0.0	P6V65.6Q	200V	0	3	
0.1	P6V654.8	200V	0	3	

All MM levels indicated are dual-polarity (±).

1.4 Electrostatic Discharge-Charged Device Model:

The SiI9437/SiI9438 product was tested per the JS-002-2014 Field-Induced Charged-Device Model Test standard.

All units were tested at room ambient prior to and after reliability stress. No failures were observed within the passing classification.

SiI9437/SiI9438 ESD CDM:

Rev. ID	Lot #	Voltage Level	Rej.	Qty.	Note
0.0	P6V65.6Q	500V	0	3	
0.1	P6V654.8	500V	0	3	

CDM classification per JS-002-2014 is CLASS C2a.
All CDM levels indicated are dual-polarity (±).

1.5 Latch-Up:

The SiI9437/SiI9438 product was tested per the JESD78D IC Latch-up Test standard.
All units were tested at room ambient prior to and after reliability stress. No failures were observed within the passing classification.

Rev. ID	Lot #	I-Test	Rej.	Qty.	Note
0.0	P6V65.6Q	+/-200mA	0	3	
0.1	P6V654.8	+/-200mA	0	3	

Rev. ID	Lot #	Over Voltage	Rej.	Qty.	Note
0.0	P6V65.6Q	Vddmax * 1.5x	0	3	
0.1	P6V654.8	Vddmax * 1.5x	0	3	

I-Test/Over Voltage classification per JESD78D is CLASS II (70°C room ambient).
All I-Test levels indicated are dual-polarity (±).

PACKAGE QUALIFICATION DATA FOR SII9437/SII9438

The SiI9437/SiI9438 product is offered in a 32 QFN ePAD packages. This report details the package qualification results of the SiI9437/SiI9438 product. Package qualification tests include Preconditioning (PC), Temperature Cycling (TC), Unbiased HAST (UHAST), Temperature Humidity Bias (THB) and High Temperature Storage (HTSL). Mechanical evaluation tests include Scanning Acoustic Tomography (SAT) and visual package inspection.

1.6 Package Data

Assembly information	Description
Assembly site	ASECL
Package type	32 SQFN
Package size	4 x 4 mm
Body Thickness	0.90mm
Lead Pitch	0.40 mm
Lead Frame Manufacturer	SAMSUNG
Lead Frame Thickness	0.203mm
Lead Frame Base Material	C194-FH
Plating Thickness specification	SILVER RING PLATING
Die Attach	EN-4900G
Wire Supplier & Composition	Cu-Pd
Wire Diameter	20 um
Longest Wire Length	1.594mm
Bond Pad Metal Composition	Al
Pad Size and Pad Opening	47X47 um
Mold Compound Name	CEL-9240HF
Manufacturer	HITACHI

1.7 Package Qualification Testing

The Surface Mount Preconditioning (SMPC) Test is used to model the surface mount assembly conditions during component solder processing. All devices stressed through Temperature Cycling, Unbiased HAST and THB were preconditioned. This preconditioning step is consistent with J-STD-020E "Moisture/Reflow Sensitivity Classification for Nonhermetic Surface Mount Devices" and JESD22-A113G "Preconditioning of Nonhermetic Surface Mount Devices Prior to Reliability Testing".

1.7.1 Surface Mount Preconditioning

(5 Temperature Cycles Condition B, 24 hours bake @ 125°C, 30°C/60% RH, soak 192 hours, 3x IR reflow @260°C Reflow Simulation. Performed before Temperature Cycling, Unbiased HAST, and THB package tests.

Classification Level: MSL3

Method: J-STD-020E and JESD22-A113G

Package	Assembly Site	Lot #	Rej.	Qty.	Note
32 QFN	ASECL	P6V65.6Q	0	239	

1.7.2 Temperature Cycling Data

The Temperature Cycling test is used to accelerate those failures resulting from mechanical stresses induced by differential thermal expansion of adjacent films, layers and metallurgical interfaces in the die and package. Devices are tested at 25°C after exposure to repeated cycling between -65°C and +150°C in an air to air thermal shock environment consistent with JESD22-A104E "Temperature Cycling" standard. Prior to Temperature Cycling testing, all devices are subjected to Surface Mount Preconditioning.

MSL3 Packages: 32 QFN

Stress Duration: 1000 cycles

Stress Conditions: Temperature cycling between -65°C to 150°C

Method: JESD22-A104E Condition C

Package	Assembly Site	Lot #	Rej.	Qty.	Note
32 QFN	ASECL	P6V65.6Q	0	78	

1.7.3 Unbiased HAST Data

Unbiased Highly Accelerated Stress Test (UHAST) testing uses both pressure and temperature to accelerate penetration of moisture into the package and to the die surface. The Unbiased HAST test is designed to detect ionic contaminants present within the package or on the die surface, which can cause chemical corrosion. This stress is consistent with JESD22-A118B, "Accelerated Moisture Resistance - Unbiased HAST". The Unbiased HAST condition is 96 hours exposure at 130°C and 85% relative humidity. Prior to Unbiased HAST testing, all devices are subjected to Surface Mount Preconditioning.

MSL3 Packages: 32 QFN
Stress Duration: 96 Hours
Stress Conditions: 130°C/85% RH
Method: JESD22-A118B Condition A

Package	Assembly Site	Lot #	Rej.	Qty.	Note
32 QFN	ASECL	P6V65.6Q	0	77	

1.7.4 THB: Temperature Humidity Bias Data

The THB test is used to accelerate threshold shifts in MOS devices associated with moisture diffusion into the gate oxide region as well as electrochemical corrosion mechanisms within the device package. This stress is consistent with JESD22-A101D "Steady State Temperature Humidity Bias Life Test" standard. The THB conditions are with supply rails biased at data sheet max operating and alternate pin biasing in an ambient of 85°C/85% relative humidity. Prior to THB testing, all devices are subjected to Surface Mount Preconditioning.

MSL3 Packages: 32 QFN
Stress Conditions: Maximum Operating Supplies and 85°C/85%RH
Stress Duration: 1000 hours
Method: JESD22-A101D

Package	Assembly Site	Lot #	Rej.	Qty.	Note
32 QFN	ASECL	P6V654.5	0	84	

1.7.5 High Temperature Storage Life (HTSL)

The High Temperature Storage Life test is used to determine the effect of time and temperature, under storage conditions, for thermally activated failure mechanisms. This stress is consistent with JESD22-A103E "High Temperature Storage Life". The devices are subjected to high temperature storage Condition B (150°C) for 1000 hours.

MSL3 Packages: 32 QFN
Stress Duration: 500 hours, 1000 hours
Temperature: 150°C (ambient)
Method: JESD22-A103E Condition B

Package	Assembly Site	Lot #	Rej.	Qty.	Note
32 QFN	ASECL	P6V65.5	0	76	

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REVISION HISTORY

Date	Revision	Change Summary
November, 2016	A	Initial release.
May, 2018	B	Correct Fab location and Die Size

REFERENCE DOCUMENTS

SiI-DS-02063 – Datasheet
SiI-PS-02052 – Package Bill of Materials