SiI9396CNUC Product Qualification Summary

Lattice (Silicon Image) Document # SiI-QP-02014 September 2016

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1 INTRODUCTION

The SiI9396 device is a superMHLTM 1.0/MHL® to HDMI 2.0 bridge with HDCP 2.2 repeater support targeted for superMHL and MHL dongle from Lattice Semiconductor. The SiI9396 device is also a superMHL 1.0/HDMI 2.0 transmitter targeted for superMHL source and Set Top Box (STB).

The SiI9396 receiver port can be configured into a superMHL compliant port, an MHL 3 compliant port, or an HDMI 2.0 compliant port.

The SiI9396 device can receive and decompress VESA Display Stream Compression (DSC) 1.1 video signals up to 4K x 2K @ 60 Hz. As a bridge, the SiI9396 device supports superMHL and MHL input up to 4K x 2K @ 30 Hz with YCbCr 4:2:2.

As a superMHL transmitter, the SiI9396 device supports one output with three-lane superMHL. It also supports audio insertion through S/PDIF or 2-channel I2S input with downsampling.

As an HDMI transmitter, the SiI9396 device supports one output with HDMI 2.0 up to 18 Gb/s. The SiI9396 device can convert certain types of reduced blank formats such as a 337 MHz Transition Minimized Differential Signaling (TMDS™) input of 10-bit 4K @50/60 Hz 4:2:0 into an HDMI 2.0 standard 4K@ 50/60 Hz 4:2:2 10-bit output.

1.1. superMHL Input

- Configurable for one or three data lanes operating at 6 Gb/s per lane
- Three-lane superMHL input supports video resolution up to 4K x 2K @ 60 Hz with YCbCr 4:4:4/RGB
- One-lane superMHL input supports video resolution up to 4K x 2K @ 30 Hz with YCbCr 4:2:2
- One-lane superMHL input via DSC decompression can support up to 4K x 2K @ 60Hz with YCbCr 4:4:4/RGB

1.2. MHL Input

- Supports 6 Gb/s MHL 3 compatible input, backward compatible with MHL 1 and MHL 2

1.3. HDMI Input

- Supports 18 Gb/s HDMI 2.0 compatible input, backward compatible with HDMI 1.4

1.4. superMHL Output

- Supports three-lane superMHL output resolution up to 4K x 2K @ 60 Hz with superMHL connector
- Supports superMHL connector with reversible cable

1.5. HDMI Output

- Supports 18 Gb/s HDMI 2.0 compatible output, backward compatible with HDMI 1.4

1.6. Video Format Conversion

- BT.601/BT.709 color space conversion
- supports xvYCC colorimetry

- Supports 8-bit YCbCr 4:2:2 to YCbCr 4:4:4 chroma upsampling, 8-bit YCbCr 4:4:4 to YCbCr 4:2:2 chroma downsampling
- Supports 8/10-bit YCbCr 4:2:0 to YCbCr 4:2:2, and 8/10-bit YCbCr 4:2:2 to YCbCr 4:2:0 conversion
- Supports pixel reorder with 4K x 2K @ 30 Hz

1.7. DSC Decoder

- Supports 8-bit DSC decoder with YCbCr 4:4:4/RGB
- Supports 8/10-bit DSC decoder with YCbCr 4:2:0

1.8. Audio

- Supports audio insertion through one I2S input up to two channels or S/PDIF input
- Supports audio extraction up to eight channels through four I2S outputs or S/PDIF output
- Supports up to 192 kHz PCM and compressed audio formats
- Supports high bitrate (HBR) audio output up to 384 kHz

1.9. HDCP

- Built in HDCP 2.2/HDCP 1.4 decryption engine
- Built in HDCP 2.2/HDCP 1.4 encryption engine
- Supports HDCP 2.2 and HDCP 1.4 repeater

1.10. Host Interface

- Inter-Integrated Circuit (I2C)
- Serial Peripheral Interface (SPI)

1.11. Microprocessor

- Built-in enhanced microprocessor

2 LATTICE PRODUCT QUALIFICATION PROGRAM

Lattice Semiconductor (Silicon Image) Corp. maintains a comprehensive reliability qualification program to assure that each product achieves its reliability goals. After initial qualification, the continued high reliability of Lattice (Silicon Image) products is assured through ongoing monitor programs as described in Lattice Semiconductor's (Silicon Image) Reliability Monitor Program Procedure (Doc. #SiI-QA-0007). All products qualification plans are generated in conformance with Lattice Semiconductor's (Silicon Image) Qualification Procedure (Doc. # SiI-QA-0007) with failure analysis performed in conformance with Lattice Semiconductor's (Silicon Image) Failure Analysis Procedure (Doc. #SiI-QA-0045). Both documents are referenced in Lattice Semiconductor's (Silicon Image) Quality Assurance Manual, which can be obtained upon request from a Lattice Semiconductor sales office. Figure1 shows the Product Qualification Process Flow.

If failures occur during qualification, an 8D process is used to find root cause and eliminate the failure mode from the design, materials, or process. The effectiveness of any fix or change is validated through additional testing as required. Final testing results are reported in the qualification reports.

Failure rates in this reliability report are expressed in FITs. Due to the very low failure rate of integrated circuits, it is convenient to refer to failures in a population during a period of 10^9 device hours; one failure in 10^9 device hours is defined as one FIT.

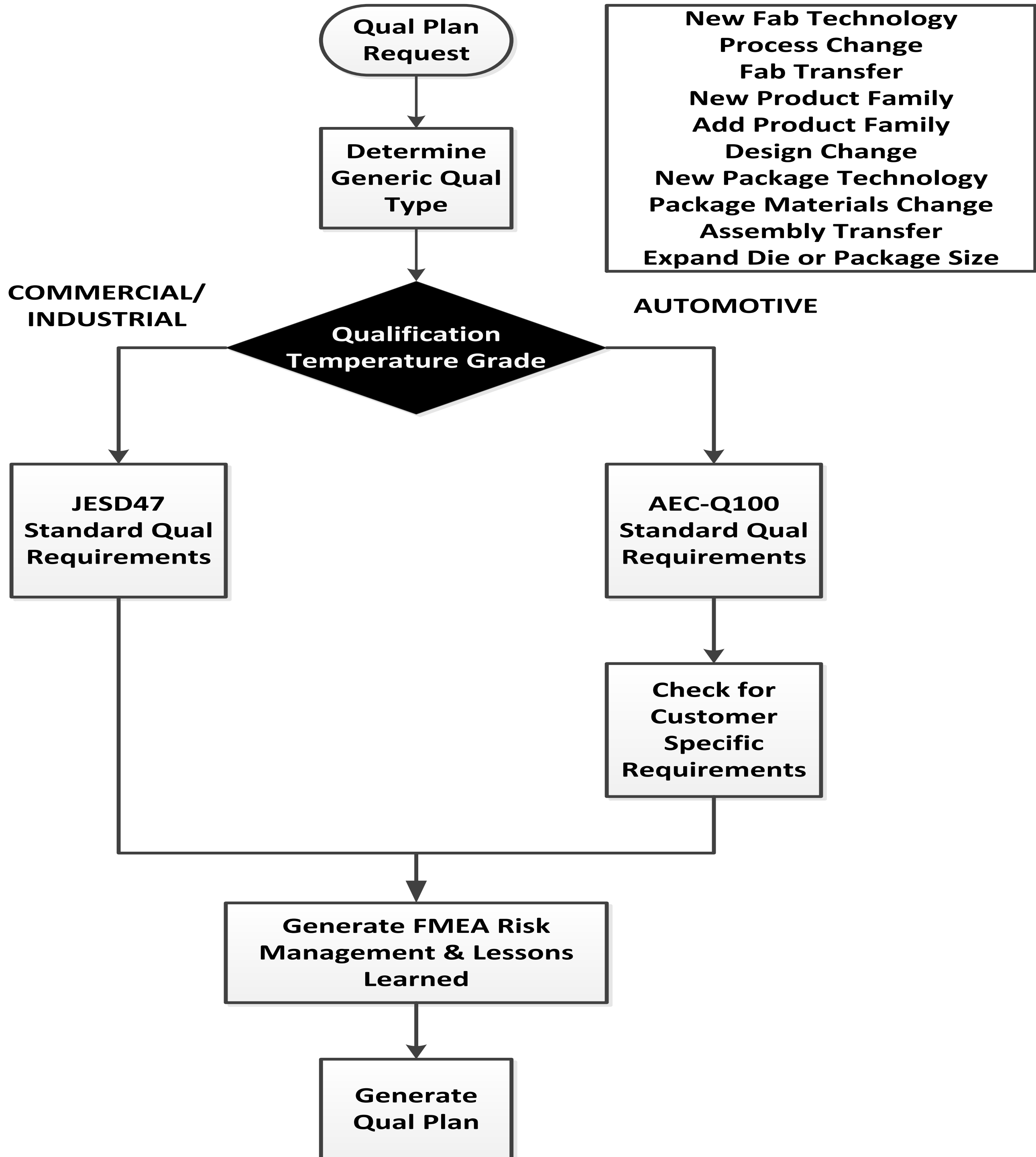
Product families are qualified based upon the requirements outlined in Figure#1. In general, Lattice Semiconductor (Silicon Image) follows the current Joint Electron Device Engineering Council (JEDEC) and Military Standard testing methods. Lattice Commercial products are qualified and characterized to the Electron Device Engineering Council (JEDEC) testing requirements and methods. Product family qualification will include products with a wide range of circuit densities, package types, and package lead counts. Major changes to products, processes, or vendors require additional qualification before implementation.

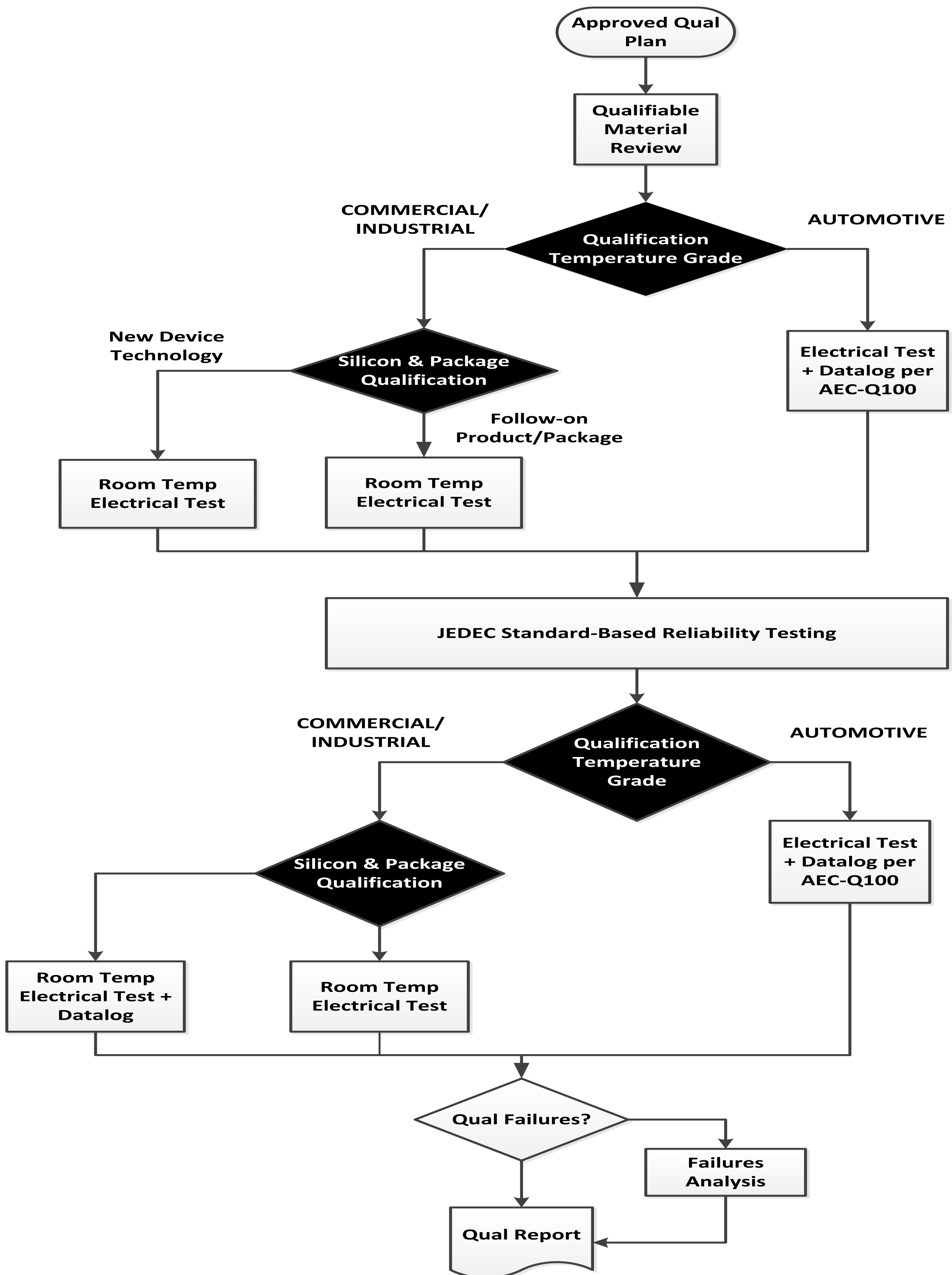
Lattice Semiconductor (Silicon Image) maintains a regular reliability monitor program. The current Lattice (Silicon Image) Reliability Monitor Report which can be obtained upon request.

2.1 Lattice (Silicon Image) Standard Product Qualification Process Flow

This diagram represents the standard qualification flow used by Lattice (Silicon Image) to qualify new Product Families. The target end market for the Product determines which flow options are used. The SII9396CNUC Product was qualified using the Commercial Option.

Figure1




Approved Qual Plan
Qualifiable Material Review
COMMERCIAL/ INDUSTRIAL
Qualification Temperature Grade
AUTOMOTIVE
New Device Technology
Silicon & Package Qualification
Electrical Test + Datalog per AEC-Q100
Follow-on Product/Package
Room Temp Electrical Test
Room Temp Electrical Test
JEDEC Standard-Based Reliability Testing
COMMERCIAL/ INDUSTRIAL
Qualification Temperature Grade
AUTOMOTIVE
Silicon & Package Qualification
Electrical Test + Datalog per AEC-Q100
Room Temp Electrical Test + Datalog
Room Temp Electrical Test
Qual Failures?
Failures Analysis
Qual Report

3 STANDARD QUALIFICATION AND REFERENCE DOCUMENTS

Table#1

Description	Abv.	reference	Condition	Test Intervals	Sample Size	Comments
High Temperature Operating Life	HTOL	JESD 22A108	Tj=Not to exceed 150°C at 1.1XVdd For 1000 hours	0, 168, 500 & 1000 Hrs	1 lot x 77 units	
Human Body Model	HBM	JS-001-2014	+/- 2000V	Before & after stress	1 lot x 3units	
Charge Device Model	CDM	JS-002-2014	+/- 500V	Before & after stress	1 lot x 3units	
Machine Model	MM	JESD 22A115	+/- 150V	Before & after stress	1 lot x 3units	
Latch Up	LU	JESD 78	200mA current injection & power supply overvoltage tests	Before & after stress	1 lot x 3units	
Preconditioning before: THB, HAST,TC, AC, & UHAST	PC	JSTD 020 / JESD 22A113	JEDEC MSL Level 3 Reflow Peak Temp 260 °C	Before & after stress with C-Sam on 100% Units	3 lot x 231 units	
High Temperature Storage Life	HTSL	JESD 22A103	150°C for 1000 Hrs	0, 168, 500 & 1000 Hrs	3 lots x 77 units	
Accelerated Moisture Resistance - unbiased HAST	uHAST	JESD 22A102	130ºC / 85% R.H / 33.3 psia for 96Hrs	0, 96 Hrs	3 lot x 77 units	
Temperature-Humidity-Bias Life Test	THBT	JESD 22A101	85ºC/85% RH with bias 1000 Hrs	0, 168, 500 & 1000Hrs	3 lot x 77 units	
Temperature Cycling	TCT	JESD 22A104	-65ºC to +150 ºC 1000 cycles	0, 500 & 1000 cycles	3 lot x 77 units	

4 TECHNOLOGY QUALIFICATION DATA FOR SII9396CNUC PRODUCT

Product Family: SiI9396CNUC
Packages offered: 76 MQFN
Process Technology Fab: TSMC Fab.12
Process Technology Node: 55nm, 1P7M GP Process
Wafer Size: 12 inches
Die Size: X: 4.184mm; Y: 4.779mm

5 PRODUCT LIFE (HTOL) DATA

5.1 High Temperature Operating Life (HTOL) Test:

The High Temperature Operating Life test is used to thermally accelerate those wear out and failure mechanisms that would occur as a result of operating the device continuously in a system application. Consistent with JESD22-A108 “Temperature, Bias, and Operating Life”, a pattern specifically designed to exercise the maximum amount of circuitry is programmed into the device and this pattern is continuously exercised at specified voltages as described in test conditions for each device type.

The Early Life Failure Rate (ELFR) test uses large samples sizes for a short duration (48hrs) HTOL stress to determine the infant mortality rate of a device family.

Life Test (HTOL) Conditions:
Stress Duration: 168, 500, 1000 hours
Stress Conditions: Max operating supplies, Ambient = 125°C
Method: JESD22-A108

		168hrs			500hrs			1000hrs		
Rev. ID	Lot #	Rej.	Qty.	Note	Rej.	Qty.	Note	Rej.	Qty.	Note
1.0	N6R160.11	0	77		0	77		0	77	
1.1	N6R160.Q4	0	77		0	77		0	77	
	Total	0	154		0	154		0	154	

6 PRODUCT LIFE CALCULATION DATA

FITs= 60%	76.45	FITs
EFR (PPM)= 60%	5,949.94	Hours
MTTF= 60%	13,079,613.03	Hours
Useful Life Time=	8.88	Years
In-Stress Device Hours=	154000.00	Hours

FIT Assumptions: CL=60%, AE=0.7eV, Tjref=55C

7 ESD AND LATCH UP DATA

7.1 Electrostatic Discharge-Human Body Model:

The SiI9396CNUC product was tested per JS-001-2014 Electrostatic Discharge (ESD) Sensitivity Testing Human Body Model (HBM) procedure from ESDA/JEDEC Joint Standard.

All units were tested at room ambient prior to reliability stress and after reliability stress. No failures were observed within the passing classification.

SiI9396CNUC ESD-HBM:

Rev. ID	Lot #	Voltage Level	Rej.	Qty.	Note
1.1	N6R160.10	2000V	0	3	
1.1	N6R160.10	4000V	0	3	

HBM classification for Commercial products, per ESD-HBM per JS-001-2014.
All HBM levels indicated are dual-polarity (±).
HBM worst-case performance is the package with the smallest RLC parasitic.

7.2 Electrostatic Discharge-Machine Model:

The SiI9396CNUC product was tested per JESD22-A115 Electrostatic Discharge (ESD) Sensitivity Testing Machine Model (MM) procedure.

All units were tested at room ambient prior to reliability stress and after reliability stress. No failures were observed within the passing classification.

SiI9396CNUC ESD MM:

Rev. ID	Lot #	Voltage Level	Rej.	Qty.	Note
1.1	N6R160.10	150V	0	3	

MM classification for Industrial products, per JESD22-A115.
All MM levels indicated are dual-polarity (±).
MM worst-case performance is the package with the smallest RLC parasitic.

7.3 Electrostatic Discharge-Charged Device Model:

The SiI9396CNUC product was tested per the JS-002-2014, Field-Induced Charged-Device Model Test Method for Electrostatic-Discharge-Withstand Thresholds of ESDA/JEDEC Joint Standard.

All units were tested at room ambient prior to reliability stress and after reliability stress. No failures were observed within the passing classification.

SiI9396CNUC ESD CDM:

Rev. ID	Lot #	Voltage Level	Rej.	Qty.	Note
1.1	N6R160.10	500V	0	3	
1.1	N6R160.10	1000V	0	3	

CDM classification Commercial products, per JS-002-2014.
All CDM levels indicated are dual-polarity (±).
CDM worst-case performance is the package with the largest bulk capacitance.

7.4 Latch-Up:

The SiI9396CNUC product was tested per the JESD78 IC Latch-up Test procedure.
All units were tested at room ambient prior to reliability stress and after reliability stress. No failures were observed within the passing classification.

Rev. ID	Lot #	I-Test	Rej.	Qty.	Note
1.1	N6R160.10	+/-200mA	0	3	

Rev. ID	Lot #	Over Voltage	Rej.	Qty.	Note
1.1	N6R160.10	Vddmax * 1.5x	0	3	

I-Test classification for Commercial products, per JESD78, Class II (85°C room ambient).
All I-Test levels indicated are dual-polarity (±).
I-Test worst-case performance is the package with access to the most IOs.

8 PACKAGE QUALIFICATION DATA FOR SII9396CNUC

The SiI9396CNUC product is offered in 76 QFN ePAD packages. This report details the package qualification results of the SiI9396CNUC product. Package qualification tests include Preconditioning (PC), Temperature Cycling (TC), Unbiased HAST (UHAST), Temperature Humidity Bias (THB) and High Temperature Storage (HTSL). Mechanical evaluation tests include Scanning Acoustic Tomography (SAT) and visual package inspection.

8.1 Package Data

Assembly information	Description
Assembly site	SPIL
Package type	MQFN (Saw Type)
Ball count	76 pin
Package size	10x10mm
Pitch	0.4mm
Moulding Compound	G631B
Moulding Manufacturer	Sumitomo
Lead Frame Manufacturer	MHT
L/F Thickness	2.5 ~ 7.1 um
Lead Frame Base Material	A194FH
Plating Material/Process	Ag-dual ring / Plating
Die Attach Material	1033BF
Brand Name	Sumitomo
Wire Supplier & Composition	Au-Pd-Cu
Wire Diameter	0.8 mil
Longest Wire Length	137.02

8.2 Package Qualification Testing

The Surface Mount Preconditioning (SMPC) Test is used to model the surface mount assembly conditions during component solder processing. All devices stressed through Temperature Cycling, Unbiased HAST and Biased HAST were preconditioned. This preconditioning is consistent with JESD22-A113F "Preconditioning Procedures of Plastic Surface Mount Devices Prior to Reliability Testing", Moisture Sensitivity Level 3 (MSL3) package moisture sensitivity and dry-pack storage requirements.

8.2.1 Surface Mount Preconditioning (MSL3)

(5 Temperature Cycles Condition B, 24 hours bake @ 125°C, 30°C/60% RH, soak 192 hours, 3x IR reflow @260 °C Reflow Simulation. Performed before all package tests.

MSL3 Packages: 76 MQFN

Method: J-STD-020D and JESD22-A113

Package	**Assembly Site**	Lot #	Rej.	Qty.	Note
76 MQFN	SPIL	N6R160.2Q	0	231	
76 MQFN	SPIL	N6R160.3Q	0	231	
76 MQFN	SPIL	N6R160.4Q	0	231	

8.2.2 Temperature Cycling Data

The Temperature Cycling test is used to accelerate those failures resulting from mechanical stresses induced by differential thermal expansion of adjacent films, layers and metallurgical interfaces in the die and package. Devices are tested at 25°C after exposure to repeated cycling between -65°C and +150°C in an air environment consistent with JESD22-A104 "Temperature Cycling", Condition C temperature cycling requirements. Prior to Temperature Cycling testing, all devices are subjected to Surface Mount Preconditioning.

MSL3 Packages: 76 MQFN

Stress Duration: 500cycles, 1000 cycles

Stress Conditions: Temperature cycling between -65°C to 150°C

Method: JESD22-A104 Condition C

Package	**Assembly Site**	Lot #	Rej.	Qty.	Note
76 MQFN	SPIL	N6R160.2Q	0	77	
76 MQFN	SPIL	N6R160.3Q	0	77	
76 MQFN	SPIL	N6R160.4Q	0	77	

8.2.3 Unbiased HAST Data

Unbiased Highly Accelerated Stress Test (UHAST) testing uses both pressure and temperature to accelerate penetration of moisture into the package and to the die surface. The Unbiased HAST test is designed to detect ionic contaminants present within the package or on the die surface, which can cause chemical corrosion. Consistent with JESD22-A118, "Accelerated Moisture Resistance - Unbiased HAST," the Unbiased HAST condition is 96 hours exposure at 130°C and 85% relative humidity. Prior to Unbiased HAST testing, all devices are subjected to Surface Mount Preconditioning.

MSL3 Packages: 76 MQFN
Stress Duration: 96 Hours
Stress Conditions: 130°C/85% RH
Method: JESD22-A118

Package	Assembly Site	Lot #	Rej.	Qty.	Note
76 MQFN	SPIL	N6R160.2Q	0	77	
76 MQFN	SPIL	N6R160.3Q	0	77	
76 MQFN	SPIL	N6R160.4Q	0	77	

8.2.4 THB: Temperature Humidity Biased Data

Biased Highly Accelerated Stress Test (THB) testing uses both pressure and temperature to accelerate penetration of moisture into the package and to the die surface. The Biased THB test is used to accelerate threshold shifts in the MOS device associated with moisture diffusion into the gate oxide region as well as electrochemical corrosion mechanisms within the device package. Consistent with JESD22-A101 "Steady State Temperature Humidity
Bias Life Test (THB)", the biased THB conditions are with supply rails biased and alternate pin biasing in an ambient of 85°C, 85% relative humidity. Prior to Biased HAST testing, all devices are subjected to Surface Mount Preconditioning.

MSL3 Packages: 76 MQFN
Stress Conditions: Maximum Operating Supplies and 85°C / 85%RH, 49.1 psig
Stress Duration: 500 hours, 1000 hours
Method: JESD22-A101

Package	Assembly Site	Lot #	Rej.	Qty.	Note
76 MQFN	SPIL	N6R160.2Q	0	77	
76 MQFN	SPIL	N6R160.3Q	0	77	
76 MQFN	SPIL	N6R160.4Q	0	77	

8.2.5 High Temperature Storage Life (HTSL)

The High Temperature Storage Life test is used to determine the effect of time and temperature, under storage conditions, for thermally activated failure mechanisms. Consistent with JESD22-A103, the devices are subjected to high temperature storage Condition B: +150 (-0/+10) °C for 1000 hours.

MSL3 Packages: 76 MQFN
Stress Duration: 500 hours, 1000 hours
Temperature: 150°C (ambient)
Method: JESD22-A103

Package	**Assembly Site**	Lot #	Rej.	Qty.	Note
76 QFN	SPIL	N6R160.2Q	0	77	
76 QFN	SPIL	N6R160.3Q	0	77	
76 QFN	SPIL	N6R160.4Q	0	77	

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