Lattice Platform Manager 2 Product Family Qualification Summary

Lattice Document # 25 – 107312 October 2014

Dear Customer,

Enclosed is Lattice Semiconductor's Platform Manager 2 Product Family Qualification Report.

This report was created to assist you in the decision making process of selecting and using our products. The information contained in this report represents the entire qualification effort for this device family.

The information is drawn from an extensive qualification program of the wafer technology and packaging assembly processes used to manufacture our products. The program adheres to JEDEC and Automotive Industry standards for qualification of the technology and device packaging. This program ensures you only receive product that meets the most demanding requirements for Quality and Reliability.

Your feedback is valuable to Lattice. If you have suggestions to improve this report, or the data included, we encourage you to contact your Lattice representative.

Sincerely,

James M. Orr
Vice President,
Corporate Quality & Product Development
Lattice Semiconductor Corporation

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1.0 INTRODUCTION

The Lattice Platform Manager 2 device is a fast-reacting, programmable logic-based Hardware Management Controller. Platform Manager 2 is an integrated solution combining analog sense and control elements with scalable programmable logic resources.

The L-ASC10 (Analog Sense and Control - 10 rail also referred to as ASC) is a Hardware Management Expander designed to be used with Platform Manager 2 or MachXO2 FPGAs to implement the Hardware Management Control function in a circuit board.

Table 1.01 Platform Manager 2 Family

	H/W Management Expander	Hardware Management Controller	
	L-ASC10	LPTM20	LPTM21
Voltage Monitoring Inputs	10	8	10
Current Monitoring Inputs	2	2	2
Temperature Monitoring Inputs	2	2	2
Number of Trimming Channels	4	2	4
MOSFET Drives	4	4	4
On-Chip Non-Volatile Fault Log	✓	✓	✓
Number of LUTs	-	640	1280
Distributed RAM (Kbits)	-	5	10
EBR SRAM (kBits)	-	18	64
Number of EBR Blocks (9 kBits)	-	2	7
User Flash Memory (kBits)	-	24	64
Number of PLLs	-	0	1
Communication I/F	I2C	I2C/SPI/JTA	
Programming Interface	I2C	12C/SPI/JTA	
Operating Voltage	3.3	I2C/SPI/JTA	
Insystem Update Support	Yes		
Package Options	Digital I/Os		
48-pin QFN (7x7)	9		
128-pin TQFP (14x140)		60	
237-ball ftBGA (1mm) (17x17)			106

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2.0 LATTICE PRODUCT QUALIFICATION PROGRAM

Lattice Semiconductor Corp. maintains a comprehensive reliability qualification program to assure that each product achieves its reliability goals. After initial qualification, the continued high reliability of Lattice products is assured through ongoing monitor programs as described in Reliability Monitor Program Procedure (Doc. #70-101667). All product qualification plans are generated in conformance with Lattice Semiconductor's Qualification Procedure (Doc. #70-100164) with failure analysis performed in conformance with Lattice Semiconductor's Failure Analysis Procedure (Doc. #70-100166). Both documents are referenced in Lattice Semiconductor's Quality Assurance Manual, which can be obtained upon request from a Lattice Semiconductor sales office or downloaded from the lattice website at www.latticesemi.com. Figure 2.1 shows the Product Qualification Process Flow.

If failures occur during qualification, an 8-Discipline (8D) process is used to find root cause and eliminate the failure mode from the design, materials, or process. The effectiveness of any fix or change is validated through additional testing as required. Final testing results are reported in the qualification reports.

Failure rates in this reliability report are expressed in FITS. Due to the very low failure rate of integrated circuits, it is convenient to refer to failures in a population during a period of 10^9 device hours; one failure in 10^9 device hours is defined as one FIT.

Product families are qualified based upon the requirements outlined in Table 2.2. In general, Lattice Semiconductor follows the current Joint Electron Device Engineering Council (JEDEC) and Military Standard testing methods. Lattice automotive products are qualified and characterized to the Automotive Electronics Council (AEC) testing requirements and methods. Product family qualification will include products with a wide range of circuit densities, package types, and package lead counts. Major changes to products, processes, or vendors require additional qualification before implementation.

Lattice Semiconductor maintains a regular reliability monitor program. The current Lattice Reliability Monitor Report can be found at Product Reliability Monitor Report.

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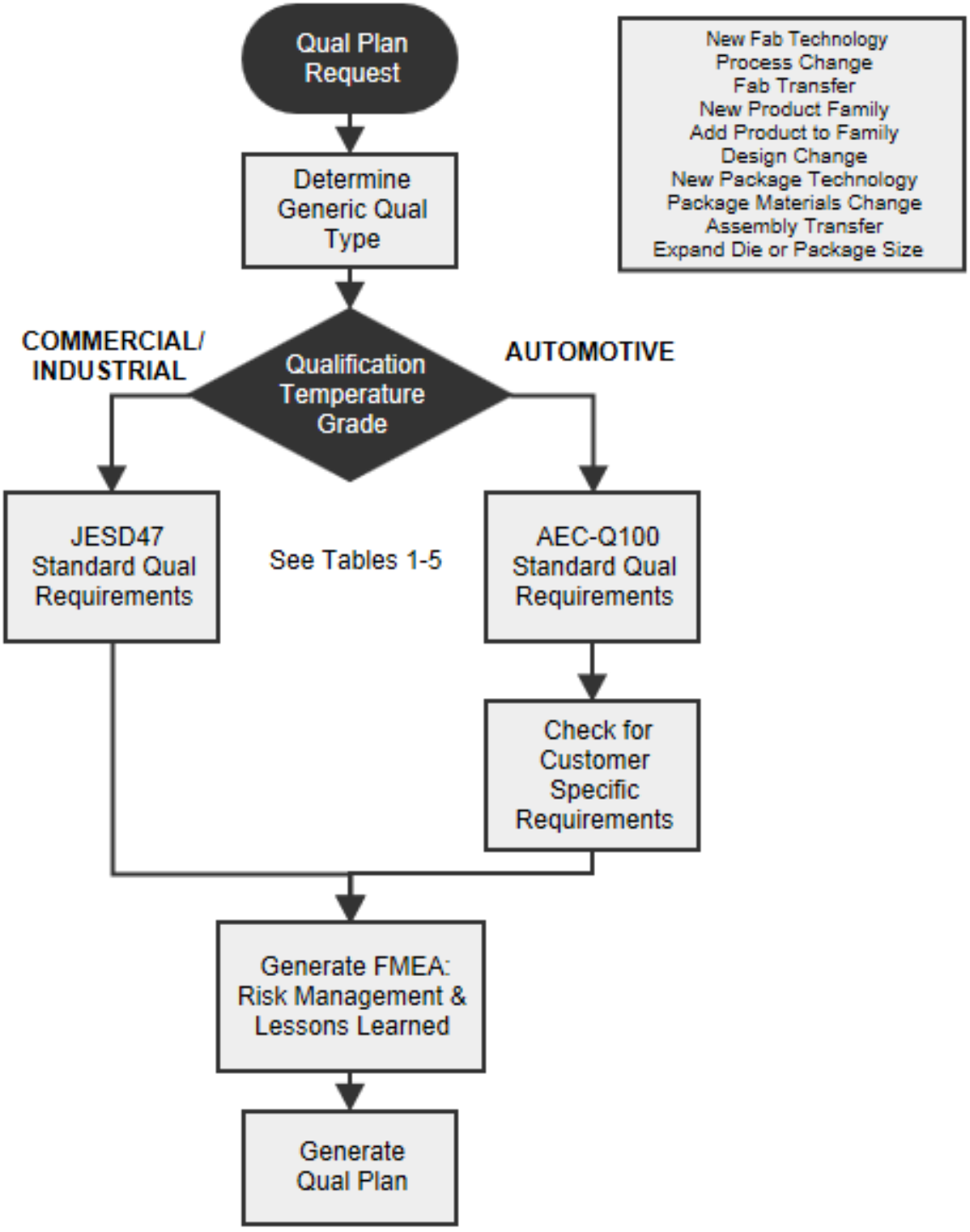
Figure 2.01 Platform Manager 2 Product Qualification Process Flow



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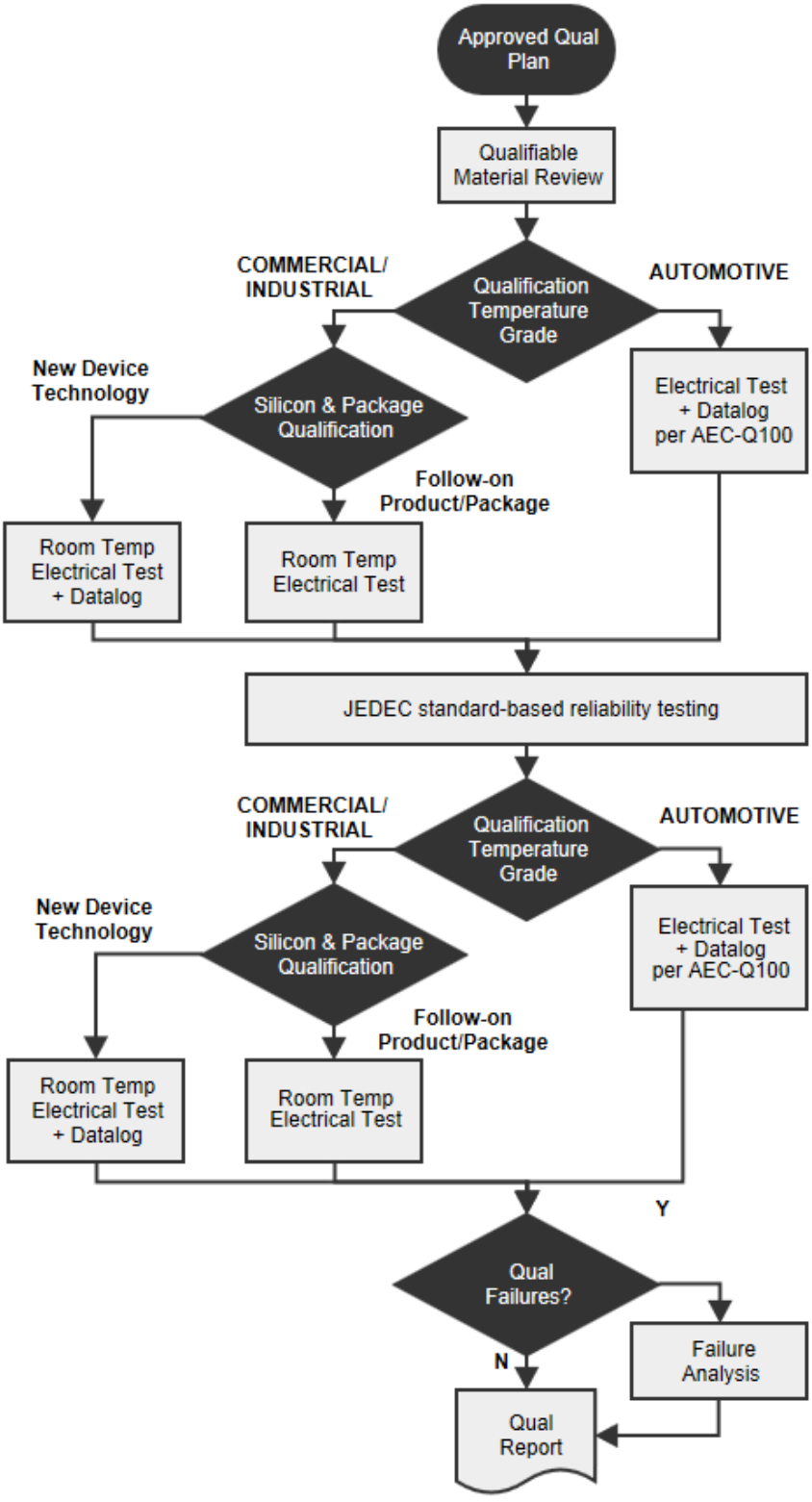

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Table 2.02 Standard Qualification Testing

TEST	STANDARD	TEST CONDITIONS	SAMPLE SIZE (Typical)	PERFORMED ON
High Temperature Operating Life HTOL	Lattice Procedure # 87-101943, MIL-STD-883, Method 1005.8, JESD22-A108 LatticeECP3	125° C, Maximum operating Vcc, 168, 500, 1000, 2000 hrs.	77/lot 2-3 lots	Design, Foundry Process, Package Qualification
High Temp Storage Life HTSL	Lattice Procedure # 87-101925, JESD22-A103 LatticeECP3	150° C, at 168, 500, 1000, 2000 hours.	77/lot 2-3 lots	Design, Foundry Process, Package Qualification
ESD HBM	Lattice Procedure # 70-100844, MIL-STD-883, Method 3015.7 JESD22-A114	Human Body Model	3 parts/lot 1-3 lots typical	Design, Foundry Process
ESD CDM	Lattice Procedure # 70-100844, JESD22-C101	Charged Device model	3 parts/lot 1-2 lots typical	Design, Foundry Process
Latch Up Resistance LU	Lattice Procedure # 70-101570, JESD78	±100 ma on I/O's, Vcc +50% on Power Supplies. (Max operating temp.)	6 parts/lot 1-2 lots typical	Design, Foundry Process
Surface Mount Pre-conditioning SMPC	Lattice Procedure # 70-103467, IPC/JEDEC J-STD-020D.1 JESD-A113 FPGA - MSL 3	10 Temp cycles, 24 hr 125° C Bake 192hr. 30/60 Soak 3 SMT simulation cycles	All units going into Temp Cycling, UHAST, BHAST, 85/85	Plastic Packages only
Temperature Cycling TC	Lattice Procedure #70-101568, MIL-STD- 883, Method 1010, Condition B JESD22-A104	(700 cycles) Repeatedly cycled between -55° C and +125° C in an air environment	45 parts/lot 2-3 lots	Design, Foundry Process, Package Qualification
Power Temperature Cycling PTC		(1000 cycles) Repeatedly cycled between -55° C and +125° C in an air environment with asynchronous power on-off cycling.	45 parts/lot 2-3 lots	Design, Foundry Process, Package Qualification. This test is required only for Automotive-qualified devices with maximum rated power $\geq$ 1 watt or DTJ $\geq$ 40ºC.
Unbiased HAST UHAST	Lattice Procedure # 70-104285 JESD22-A118	2 atm. Pressure, 96 hrs, 130 C, 85% Relative Humidity	45 parts/lot 2-3 lots	Foundry Process, Package Qualification Plastic Packages only

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TEST	STANDARD	TEST CONDITIONS	SAMPLE SIZE (Typical)	PERFORMED ON
Moisture Resistance Temperature Humidity Bias 85/85 THBS or Biased HAST BHAST	Lattice Procedure # 70-101571, JESD22-A101 JESD22-A110	Biased to maximum operating Vcc, 85° C, 85% Relative Humidity, 1000 hours or Biased to maximum operating Vcc, 2atm. Pressure, 96 hrs, 130 C, 85% Relative Humidity	45 devices/lot 2-3 lots	Design, Foundry Process, Package Qualification Plastic Packages only
Physical Dimensions	Lattice Procedure # 70-100211, MIL-STD- 883 Method 2016 or applicable LSC case outline drawings	Measure all dimensions listed on the case outline.	5 devices	Package Qualification
Ball Shear	Lattice Procedure # 70-104056 # 70-100433	Per Package Type	3 devices per package / 30 balls each unit	Package Qualification

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3.0 SILICON QUALIFICATION DATA FOR THE PLATFORM MANAGER 2 PRODUCT FAMILY

The Platform Manager 2 product family combines two proven die solutions assembled into both a stacked die TQFP and a multi-chip module ftBGA package configurations. The Analog section of the Platform Manager 2 is comprised of an Analog Sense Control (ASC) die, which is built on the EE8A process technology. EE8A is a 0.35um Electrically Erasable (E2 cell based) CMOS process at Seiko Epson (SE). This process was also used by the Lattice Power Manager 2 devices (PM2) POWR1220AT8, POWR1014A AND LA-ispPAC-POWR1014A fabricated at Seiko Epson. The FPGA section of a Platform Manager 2 device is a MachXO2HC-1200 die, which is built on CS200F process technology. CS200F is a 65nm Flash CMOS process with low-k dielectric and copper metallization, fabricated by Fujitsu Limited. Both technologies going into the Platform Manager 2 product family were previously qualified and are in volume production. The combined silicon qualifications are shown below.

3.1 CS200F FPGA and EE8A PM2 & ASC Life Test Data (ELFR & HTOL)

High Temperature Operating Life (HTOL) Test

The High Temperature Operating Life test is used to thermally accelerate those wear out and failure mechanisms that would occur as a result of operating the device continuously in a system application. Consistent with JEDEC JESD22-A108 "Temperature, Bias, and Operating Life", a pattern specifically designed to exercise the maximum amount of circuitry is programmed into the device and this pattern is continuously exercised at specified voltages as described in test conditions for each device type.

HTOL Stress Conditions:
Stress Duration: 48, 168, 500, 1000 and 2000 hours
Temperature: 125°C
Stress Voltage: LPTM21, POWR1220AT8, POWR1014A and LA-ispPAC-POWR1014A: V_{CC}= 3.47V
Stress Voltage: MachXO2: V_{CC}=1.3V (E) or 3.6V (C) / V_{CCIO}=3.6V
Method: Lattice Document # 87-101943 and JESD22-A108

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Table 3.1.1 CS200F and EE8A HTOL Results

Product Name	Foundry	Lot #	Qty	48 Hrs Result	168 Hrs Result	500 Hrs Result	1000 Hrs Result	2000 Hrs Result	Cumulative Hours
LPTM21	SE + FJ	Lot #1	80	N/A	0	0	0	0	160,000
LPTM21	SE +FJ	Lot #3	80	N/A	0	0	0	N/A	160,000
LA-ispPAC-POWR1014A	SE	Lot #11	77	N/A	N/A	0	N/A	N/A	38,500
LA-ispPAC-POWR1014A	SE	Lot #12	77	N/A	N/A	N/A	N/A	N/A	38,500
ispPAC-POWR1220AT8	SE	Lot #1	77	N/A	0	0	0	N/A	77,000
ispPAC-POWR1220AT8	SE	Lot #2	77	N/A	0	0	0	N/A	77,000
ispPAC-POWR1220AT8	SE	Lot #3	77	N/A	0	0	0	N/A	77,000
ispPAC-POWR1220AT8	SE	Lot #4	26	N/A	0	0	0	N/A	26,000
ispPAC-POWR1220AT8	SE	Lot #5	26	N/A	0	0	0	N/A	26,000
ispPAC-POWR1220AT8	SE	Lot #6	26	N/A	0	0	0	N/A	26,000
ispPAC-POWR1220AT8	SE	Lot #7	26	N/A	0	0	0	N/A	26,000
ispPAC-POWR1220AT8	SE	Lot #1	796	0	N/A	0	N/A	N/A	38,208
ispPAC-POWR1220AT8	SE	Lot #2	800	0	N/A	0	N/A	N/A	38,400
ispPAC-POWR1220AT8	SE	Lot #3	799	0	N/A	0	N/A	N/A	38,352
LCMXO2-1200ZE	FJ	Lot #6	60	N/A	0	0	0	N/A	60,000
LCMXO2-1200HE	FJ	Lot #6	60	N/A	0	0	0	N/A	60,000
LCMXO2-1200HC	FJ	Lot #6	60	N/A	0	0	0	N/A	60,000
LCMXO2-1200ZE	FJ	Lot #6	48	N/A	0	0	0	N/A	48,000
LCMXO2-1200HE	FJ	Lot #6	49	N/A	0	0	0	N/A	49,000
LCMXO2-1200HC	FJ	Lot #6	50	N/A	0	0	0	N/A	50,000
LCMXO2-7000ZE	FJ	Lot #1	40*	N/A	0	0	0	0	80,000
LCMXO2-7000HE	FJ	Lot #1	40*	N/A	0	0	0	0	80,000
LCMXO2-7000HC	FJ	Lot #1	40*	N/A	0	0	0	0	80,000
LCMXO2-7000ZE	FJ	Lot #1	50	N/A	0	0	0	0	100,000
LCMXO2-7000HE	FJ	Lot #1	48	N/A	0	0	0	0	96,000
LCMXO2-7000HC	FJ	Lot #1	48	N/A	0	0	0	0	96,000
LCMXO2-7000ZE	FJ	Lot #2	40*	N/A	0	0	0	0	80,000
LCMXO2-7000HE	FJ	Lot #2	40*	N/A	0	0	0	0	80,000
LCMXO2-7000HC	FJ	Lot #2	40*	N/A	0	0	0	0	80,000
LCMXO2-7000ZE	FJ	Lot #2	50	N/A	0	0	0	0	100,000
LCMXO2-7000HE	FJ	Lot #2	48	N/A	0	0	0	0	96,000
LCMXO2-7000HC	FJ	Lot #2	48	N/A	0	0	0	0	96,000

* FTG256 packaged units did not receive Flash cell pre-condition cycling prior to stress.

EE8A Cumulative Device Hours = 846,960
EE8A Cumulative Sample Size = 0 / 3,044
EE8A FIT Rate = 14 FIT

CS200F Cumulative Device Hours = 1,551,000
CS200F Cumulative Sample Size = 0 / 1,019
CS200F FIT Rate = 8 FIT

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Early Life Failure Rate (ELFR) Test

The Early Life Failure Rate (ELFR) evaluation is generated using the High Temperature Operating Life test conditions to verify device quality. ELFR is used to thermally accelerate those wear out and failure mechanisms that would occur as a result of operating the device continuously in a system application. Consistent with JEDEC JESD22-A108 "Temperature, Bias, and Operating Life", a pattern specifically designed to exercise the maximum amount of circuitry is programmed into the device and this pattern is continuously exercised at maximum Vcc/Vvcio.

ELFR Stress Conditions:

Stress Duration: 48 or 168 hours

Temperature: 125°C

Stress Voltage: LA-ispPAC-POWR1014A: V_{CC}= 3.6V

Stress Voltage: MachXO2: V_{CC}=1.26V (E) or 3.47V (C) / V_{CCIO}=3.47V

Method: Lattice Document # 87-101943 and JESD22-A108

Table 3.1.2 CS200F and EE8A ELFR Results

Product Name	Foundry	Lot #	Qty	168 Hrs Result
ispPAC-POWR1220AT8	SE	Lot #1	796	0
ispPAC-POWR1220AT8	SE	Lot #2	800	0
ispPAC-POWR1220AT8	SE	Lot #3	799	0
LCMXO2-1200HE	FJ	Lot #6	60	0
LCMXO2-1200HC	FJ	Lot #6	60	0
LCMXO2-1200ZE	FJ	Lot #6	48	0
LCMXO2-1200HE	FJ	Lot #6	49	0
LCMXO2-1200HC	FJ	Lot #6	50	0
LCMXO2-7000ZE	FJ	Lot #1	40*	0
LCMXO2-7000HE	FJ	Lot #1	40*	0
LCMXO2-7000HC	FJ	Lot #1	40*	0
LCMXO2-7000ZE	FJ	Lot #1	50	0
LCMXO2-7000HE	FJ	Lot #1	48	0
LCMXO2-7000HC	FJ	Lot #1	48	0
LCMXO2-7000ZE	FJ	Lot #2	40*	0
LCMXO2-7000HE	FJ	Lot #2	40*	0
LCMXO2-7000HC	FJ	Lot #2	40*	0
LCMXO2-7000ZE	FJ	Lot #2	50	0
LCMXO2-7000HE	FJ	Lot #2	48	0
LCMXO2-7000HC	FJ	Lot #2	48	0

* FTG256 packaged units did not receive Flash cell pre-condition cycling prior to stress.

EE8A ELFR Cumulative Results = 0 / 2,395

C90F ELFR Cumulative Results = 0 / 799

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3.2 CS200F FPGA and EE8A PM2 & ASC NVM High Temperature Data Retention (HTRX)

High Temperature Data Retention (HTRX)

The High Temperature Data Retention test measures the reliability of Non-Volatile Memory cells while the High Temperature Operating Life test is structured to measure functional operating circuitry failure mechanisms. The ASC utilizes an Electrically Erasable (E2) NVM cell, while the FPGA utilizes a Flash NVM cell. The High Temperature Data Retention test is specifically designed to accelerate charge gain on to or charge loss off of the NVM cells in the array. Since the charge on these cells determines the actual pattern and function of the device, this test is a measure of the reliability of the device in retaining programmed information. In High Temperature Data Retention, the NVM cell reliability is determined by monitoring the cell margin after biased static operation at 150°C. All cells in all arrays are life tested in both programmed and erased states.

Data Retention (HTRX) Conditions:

Stress Duration: 168, 500, 1000 hours
Temperature: 150°C
Stress Voltage: POWR1220AT8 and LA-ispPAC-POWR1014A: V_{CC}= 3.6V
Stress Voltage: MachXO2: V_{CC}=1.3V (E) / V_{CCIO}=3.6V
Method: Lattice Document # 87-101925 and JESD22-A103 / JESD22-A117

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Table 3.2.1 CS200F and EE8A High Temperature Data Retention Results

Product Name	Foundry	Lot #	Qty	168 Hrs Result	500 Hrs Result	1000 Hrs Result	Cumulative Hours
LA-ispPAC-POWR1014A	SE	Lot #11	78	0	0	NA	39,000
LA-ispPAC-POWR1014A	SE	Lot #13[A]	39	NA	0	NA	19,500
LA-ispPAC-POWR1014A	SE	Lot #14[B]	39	NA	0	NA	19,500
ispPAC-POWR1220AT8	SE	Lot #1	26	0	0	0	77,000
ispPAC-POWR1220AT8	SE	Lot #2	77	0	0	0	77,000
ispPAC-POWR1220AT8	SE	Lot #3	77	0	0	0	77,000
ispPAC-POWR1220AT8	SE	Lot #8[A]	26	0	0	0	77,000
ispPAC-POWR1220AT8	SE	Lot #9[B]	26	0	0	0	77,000
LCMXO2-1200ZE	FJ	Lot #3	76	0	0	0	76,000
LCMXO2-1200ZE	FJ	Lot #4[A]	26	0	0	0	26,000
LCMXO2-1200ZE	FJ	Lot #4	26	0	0	0	26,000
LCMXO2-1200ZE	FJ	Lot #4[B]	26	0	0	0	26,000
LCMXO2-1200ZE	FJ	Lot #5	80	0	0	0	80,000
LCMXO2-1200ZE	FJ	Lot #6	80	0	0	0	120,000
LCMXO2-1200ZE	FJ	Lot #6	80	0	0	0	120,000
LCMXO2-7000ZE	FJ	Lot #1	80	0	0	0	120,000
LCMXO2-7000ZE	FJ	Lot #2	80	0	0	0	120,000

A = Lot #4, #8 and #13 is a thin tunnel oxide process split.
B = Lot #4, #9 and #14 is a thick tunnel oxide process split.

EE8A Cumulative HTRX Device Hours = 463,000
EE8A Cumulative HTRX Failure Rate = 0 / 388

CS200F Cumulative HTRX Device Hours = 714,000
CS200F Cumulative HTRX Failure Rate = 0 / 554

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3.3 CS200F FPGA and EE8A PM2 & ASC NVM Extended Endurance Cycling

Extended Endurance Cycling (ExtEnd) testing measures the durability of the Non-Volatile Memories (NVM) through program and erase cycles. Endurance testing consists of repeatedly programming and erasing all cells in the array at 25°C to simulate the programming cycles that the user would perform. This test evaluates the integrity of the tunnel oxide through which current passes to program and erase the NVM cells. The PM2/ASC utilizes an Electrically Erasable (E2) NVM cell, while the FPGA utilizes a Flash NVM cell.

NVM ExtEnd Test Conditions:

Temperature: 150°C

Stress Voltage: POWR1220AT8: V_{CC}= 3.6V

Stress Voltage: MachXO2: V_{CC}=1.3V (E) / V_{CCIO}=3.6V

Method: Lattice Document # 70-104633 and JESD22-A117A

Table 3.3.1 EE8A NVM Extended Endurance Cycling Results

Product Name	Lot #	Qty	1K CYC Result	2K CYC Result	3K CYC Result	5K CYC Result	10K CYC Result	Cumulative Cycles
POWR1220AT8	Lot #3	10	0	0	0	0	0	100,000
ispPAC-POWR1220AT8	Lot #1	10	0	NA	NA	NA	NA	10,000
ispPAC-POWR1220AT8	Lot #2	10	0	NA	NA	NA	NA	10,000
ispPAC-POWR1220AT8	Lot #3	10	0	NA	NA	NA	NA	10,000
ispPAC-POWR1220AT8	Lot #8[A]	10	0	NA	NA	NA	NA	10,000
ispPAC-POWR1220AT8	Lot #9[B]	10	0	NA	NA	NA	NA	10,000
ispPAC-POWR1014A	Lot #11	10	0	NA	NA	NA	NA	10,000
ispPAC-POWR1014A	Lot #13[A]	5	0	NA	NA	NA	NA	5,000
ispPAC-POWR1014A	Lot #14[B]	5	0	NA	NA	NA	NA	5,000

A = Lot #8 and #13 is a thin tunnel oxide process split.
B = Lot #9 and #14 is a thick tunnel oxide process split.

EE8A Cumulative Endurance Failure Rate = 0 / 80
EE8A Cumulative Endurance Cycles = 170,000

Table 3.3.2 CS200F NVM Extended Endurance Cycling Results

Product Name	Lot #	Qty	Cycling Temp	1K CYC	10K CYC	20K CYC	50K CYC	100K CYC
LCMXO2-1200ZE	Lot #6	54	25C	0	0	0	0	0
LCMXO2-7000ZE	Lot #1	60	25C	0	0	0	0	0
LCMXO2-7000ZE	Lot #2	60	25C	0	0	0	0	0
LCMXO2-256ZE	Lot #1	30	25C	0	0	0	0	0
LCMXO2-256ZE	Lot #2	30	25C	0	0	0	0	0
LCMXO2-640ZE	Lot #1	30	25C	0	0	0	0	0
LCMXO2-2000ZE	Lot #1	30	25C	0	0	0	0	0
LCMXO2-4000ZE	Lot #1	30	25C	0	0	0	0	0

CS200F Cumulative Endurance Failure Rate = 0 / 324
CS200F Cumulative Endurance Cycles = 32,400,000

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3.4 Platform Manager 2 Product Family – ESD and Latch UP Data

Electrostatic Discharge-Human Body Model:

Platform Manager 2 product family was tested per the JESD22-A114 Electrostatic Discharge (ESD) Sensitivity Testing Human Body Model (HBM) procedure and Lattice Procedure # 70-100844.

All units were tested at 25°C prior to reliability stress and after reliability stress. No failures were observed within the passing classification.

Table 3.4.1 Platform Manager 2 ESD-HBM Data

Product	48QFN	128TQFP	237ftBGA
Platform Manager 2	>1500V	QBS	>1500V

HBM classification for Commercial/Industrial products, per JESD22-A114
All HBM levels indicated are dual-polarity (±)
HBM worst-case performance is the package with the smallest RLC parasitics. All other packages for a given product are qualified by similarity.

Electrostatic Discharge-Charged Device Model:

Platform Manager 2 product family was tested per the JESD22-C101, Field-Induced Charged-Device Model Test Method for Electrostatic-Discharge-Withstand Thresholds of Microelectronic Components procedure and Lattice Procedure # 70-100844.

All units were tested at 25^0C prior to reliability stress and after reliability stress. No failures were observed within the passing Classification.

Table 3.4.2 Platform Manager 2 ESD-CDM Data

Product	48QFN	128TQFP	237ftBGA
Platform Manager 2	>750V	QBS	>750V

CDM classification for Commercial/Industrial products, per JESD22-C101
All CDM levels indicated are dual-polarity (±)
CDM worst-case performance is the package with the largest bulk capacitance. All other packages for a given product are qualified by similarity.

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Latch-Up:

Platform Manager 2 product family was tested per the JEDEC EIA/JESD78 IC Latch-up Test procedure and Lattice Procedure # 70-101570. All Latch-up units are stressed at hot (105^0C)

All units were tested at 25^0C prior to reliability stress and after reliability stress. No failures were observed within the passing classification.

Table 3.4.3 Platform Manager 2 I/O Latch Up Data

Product	48QFN	128TQFP	237ftBGA
Platform Manager 2	>± 100mA	QBS	>± 100mA

I-Test LU classification for Commercial/Industrial products, per JESD78
All IO-LU levels indicated are dual-polarity (±)
IO-LU worst-case performance is the package with access to the most IOs. All other packages for a given product are qualified by similarity.

Table 3.4.4 Platform Manager 2 Vcc Latch Up Data

Product	48QFN	128TQFP	237ftBGA
Platform Manager 2	>1.5x Vcc	QBS	>1.5x Vcc

Vsupply Over-voltage Test LU classification for Commercial/Industrial products, per JESD78
Vcc-LU worst-case performance is the package with access to the most individual power rails. All other packages for a given product are qualified by similarity.

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4.0 PACKAGE QUALIFICATION DATA FOR THE PLATFORM MANAGER 2 PRODUCT FAMILY

Platform Manager 2's are assembled in halogen-free packaging at Advance Semiconductor Engineering Malaysia (ASEM) in the 48-QFN (single die), the 128-TQFP (stacked-die) and 237-ftBGA (multi-chip module) package configurations.

Product Family: LPTM21-1A FTG237, LPTM20-1A TG128 and L-ASC10-1SG48

Packages Offered: LPTM21 (237ftBGA), LPTM20 (128TQFP) and L-ASC10 (48QFN)

4.1 Platform Manager 2 Product Family Surface Mount Preconditioning Testing

The Surface Mount Preconditioning (SMPC) Test is used to model the surface mount assembly conditions during component solder processing. All devices stressed through Temperature Cycling, Un-biased HAST and Biased HAST were preconditioned. This preconditioning is consistent with JEDEC JESD22-A113 "Preconditioning Procedures of Plastic Surface Mount Devices Prior to Reliability Testing", Moisture Sensitivity Level 3 (MSL3) package moisture sensitivity and dry-pack storage requirements.

Consistent with Lattice Semiconductor Corp. document # 25-100164, package reliability testing can be qualified by extension. Once a package outline is qualified within a package grouping as per doc #70-103639, all lower lead count (and smaller body size) packages within that package type and assembly technology are qualified by extension. Additionally, once an assembly technology has been qualified for one package type, that package type shall be qualified by extension to all future fabrication processes as long as those processes continue to use the same critical elements. Those critical elements in this case, are that the process-to-process interlayer dielectric material and thickness differences do not exceed the current production process limits for the qualification vehicle used. For 180nm and older technologies, the critical elements are considered equivalent.

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Surface Mount Preconditioning (SMPC) Stress Conditions (MSL3):

(5 Temperature Cycles between -55°C and 125°C, 24 hours bake @ 125°C, 30°C/60% RH, soak 192 hours, Reflow Simulation, 3 passes) performed before all Platform Manager 2 package tests.

Package Types: LPTM21 (237ftBGA) and L-ASC10 (48QFN)

Method: Lattice Procedure # 70-103467, J-STD-020 and JESD22-A113

Table 4.1.1 Surface Mount Precondition Data

Product Name	Package	Assembly Site	Lot Number	Quantity	# of Fails	Reflow Temperature
LPTM21	237-ftBGA	ASEM	Lot #1	245	0	260°C
LPTM21	237-ftBGA	ASEM	Lot #2	245	0	260°C
LPTM21	237-ftBGA	ASEM	Lot #3	245	0	260°C
L-ASC10	48-QFN	ASEM	Lot #1	245	0	260°C
L-ASC10	48-QFN	ASEM	Lot #2	245	0	260°C
L-ASC10	48-QFN	ASEM	Lot #3	245	0	260°C

237-ftBGA Cumulative SMPC Failure Rate = 0 / 735
48-QFN Cumulative SMPC Failure Rate = 0 / 735

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4.2 High Temperature Storage Life (HTSL)

High Temperature Storage Life (HTSL) test is typically used to determine the effect of time and temperature, under storage conditions, for thermally activated failure mechanisms in the die and package. Units were stressed per JESD22-A103, High Temperature Storage Life. The HTSL units were stressed at 150°C. Prior to HTSL testing, all devices are subjected to Surface Mount Preconditioning.

High Temperature Storage Life (HTSL) Stress Conditions:

Stress Duration: 168, 500, 1000, hours

Temperature: 150°C

Package Types: LPTM21 (237ftBGA) and L-ASC10 (48QFN)

Method: Lattice Document # 87-101925 and JESD22-A103 / JESD22-A117

Table 4.2.1 High Temperature Storage Life Results

Product Name	Package	Assembly Site	Lot Number	Quantity	168 Hrs Result	500 Hrs Result	1000 Hrs Result	2000 Hrs Result	Cumulative Hours
LPTM21	237-ftBGA	ASEM	Lot #1	80	0	0	0	0	160,000
LPTM21	237-ftBGA	ASEM	Lot #2	80	0	0	0	0	160,000
LPTM21	237-ftBGA	ASEM	Lot #3	80	0	0	0	0	160,000
L-ASC10	48-QFN	ASEM	Lot #1	75	0	0	0	0	150,000
L-ASC10	48-QFN	ASEM	Lot #2	75	0	0	0	0	150,000
L-ASC10	48-QFN	ASEM	Lot #3	75	0	0	0	0	150,000

Cumulative HTSL Failure Rate = 0 / 465
Cumulative HTSL Device Hours = 0 / 930,000

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4.3 Platform Manager 2 Product Family Temperature Cycling Data

The Temperature Cycling test is used to accelerate those failures resulting from mechanical stresses induced by differential thermal expansion of adjacent films, layers and metallurgical interfaces in the die and package. Devices are tested at 25°C after exposure to repeated cycling between -55°C and +125°C in an air environment consistent with JEDEC JESD22-A104 "Temperature Cycling", Condition B temperature cycling requirements. Prior to Temperature Cycling testing, all devices are subjected to Surface Mount Preconditioning.

Temperature Cycling (T/C) Stress Conditions:

Stress Duration: 700 cycles

Stress Conditions: Temperature cycling between -55°C to 125°C

Package Types: LPTM21 (237ftBGA) and L-ASC10 (48QFN)

Method: Lattice Procedure # 70-101568 and JESD22-A104

Table 4.3.1 Temperature Cycling Data

Product Name	Package	Assembly Site	Lot Number	Quantity	Qual at 700 Cycles	EOT 1400 Cycles*
LPTM21	237-ftBGA	ASEM	Lot #1	80	0	0
LPTM21	237-ftBGA	ASEM	Lot #2	80	0	0
LPTM21	237-ftBGA	ASEM	Lot #3	80	0	0
L-ASC10	48-QFN	ASEM	Lot #1	80	0	0
L-ASC10	48-QFN	ASEM	Lot #2	80	0	0
L-ASC10	48-QFN	ASEM	Lot #3	80	0	0

*2x Readout quantity = 75 units/lot

Cumulative Temp Cycle Failure Rate = 0 / 480

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4.4 THB: Biased HAST Data

Biased Highly Accelerated Stress Test (BHAST) testing uses both pressure and temperature to accelerate penetration of moisture into the package and to the die surface. The Biased HAST test is used to accelerate threshold shifts in the MOS device associated with moisture diffusion into the gate oxide region as well as electrochemical corrosion mechanisms within the device package. Consistent with JEDEC JESD A110-B "Highly-Accelerated Temperature and Humidity Stress Test (HAST)", the biased HAST conditions are with Vcc bias and alternate pin biasing in an ambient of 110°C, 85% relative humidity, and 2 atmospheres of pressure. Prior to Biased HAST testing, all devices are subjected to Surface Mount Preconditioning.

BHAST Stress Conditions:

Stress Duration: 96 hours

Stress Voltage: Vcc = 3.6V, 130°C / 85% RH, 15 psig

Chamber Conditions: 130°C, 15psig, 85% RH

Package Types: LPTM21 (237ftBGA) and L-ASC10 (48QFN)

Method: Lattice Procedure # 70-101571 and JESD22-A101

Table 4.4.1 Biased HAST Data

Product Name	Package	Assembly Site	Lot Number	Quantity	# of Fails	Stress Duration
LPTM21	237-ftBGA	ASEM	Lot #1	80	0	264 Hrs
LPTM21	237-ftBGA	ASEM	Lot #2	80	0	264 Hrs
LPTM21	237-ftBGA	ASEM	Lot #3	80	0	264 Hrs
L-ASC10	48-QFN	ASEM	Lot #1	80	0	96 Hrs
L-ASC10	48-QFN	ASEM	Lot #2	80	0	96 Hrs
L-ASC10	48-QFN	ASEM	Lot #3	80	0	96 Hrs

Cumulative Biased HAST failure Rate = 0 / 480

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5.0 WAFER FAB PROCESS RELIABILITY

The Platform Manager 2 product family is a two-die solution, in both stacked die TQFP and multi-chip module ftBGA package configurations and is built on two wafer fab technologies. The PM2/ASC die is built on the EE8A process technology. EE8A is a 0.35um Electrically Erasable (E2 cell based) CMOS process at Seiko Epson (SE). The FPGA die is built on CS200F (also known as EE12) process technology. CS200F is a 65nm Flash CMOS process with low-k dielectric and copper metallization, fabricated by Fujitsu Limited. Platform Manager 2 end-of-life is a combination of Wafer Level Reliability (WLR) from both fabs.

5.1 EE8A Process Reliability Wafer Level Review

Several key fabrication process related parameters have been identified by the foundry that would affect the Reliability of the End-Product. These parameters are tested during the Development Phase of the Technology. Passing data (a 10yr lifetime at the reliability junction temperature) must be obtained for three lots minimum for each parameter before release to production. Normal operating conditions are defined in the Electrical Design Rules (EDR). These parameters are:

Hot Carrier Immunity (**HCI**): Effect is a reduction in transistor Idsat. Worst case is low temperature.
Time Dependent Dielectric Breakdown (**TDDB**): Transistor and capacitor oxide shorts or leakage.
Negative Bias Temperature Instability (**NBTI**): Symptom is a shift in Vth (also a reduction in Idsat).
Electromigration Lifetime (**EML**): Symptom is opens within, or shorts between, metal conductors.
Stress Migration (**SM**): Symptom is a void (open) in a metal Via due to microvoid coalescence. SM is not an issue for the EE8A BEOL (etched Al lines, W plug Vias, SiO IMD).

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Table 5.1.1 Wafer Level Reliability Results for EE8A (0.35 um) Process Technology

HCI

Device	LVN	LVP
deltalds	-10%	-10%
Celsius	25	25
Vgstress	Vd/2	0
Vds	3.6	-3.6
DC-HCI TTF >1yr	3 lots ≥ 5.5yr	2 lots ≥ 8.2e3yr

TDDB

Device	LVN	MIM
Celsius	130	130
Vg	3.3	15
Area	8000um^2	2.25e4um^2
0.1% TTF	3 lots ≥ 2.8e3yr	3 lots ≥ 2.1e3yr

EML

Layer	M1	M2	M3
Celsius	130	130	130
Delta R	+20%	+20%	+20%
Jmax	1.0mA/um	1.4mA/um	1.4mA/um
0.1% TTF	3 lots ≥ 22.4yr	3 lots ≥ 30.5yr	3 lots ≥ 16.2yr

Note: Reliability life times are based on listed temperature and used conditions. Detailed WLR test conditions are available upon request.

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5.2 CS200F Process Reliability Wafer Level Review

Several key fabrication process related parameters have been identified by the foundry that would affect the Reliability of the End-Product. These parameters are tested during the Development Phase of the Technology. Passing data (a 10yr lifetime at the reliability junction temperature) must be obtained for three lots minimum for each parameter before release to production. Normal operating conditions are defined in the Electrical Design Rules (EDR). These parameters are:

Hot Carrier Immunity (**HCI**): Effect is a reduction in transistor Idsat. Worst case is low temperature.
Time Dependent Dielectric Breakdown (**TDDB**): Transistor and capacitor oxide shorts or leakage.
Negative Bias Temperature Instability (**NBTI**): Symptom is a shift in Vth (also a reduction in Idsat).
Electromigration Lifetime (**EML**): Symptom is opens within, or shorts between, metal conductors.
Stress Migration (**SM**): Symptom is a void (open) in a metal Via due to microvoid coalescence.

Table 5.2.1 Wafer Level Reliability Results for CS200F (65nm) Process Technology

Mode							
HCI @ 25C	Device	LVN	LVP	MVN	MVP	HVN	HVP
	delta Ids	-10%	-10%	-10%	-10%	-10%	-10%
	Vgstress	Vd/2	Vd	Vd/2	Vd	Vd/2	Vd
	Vds	1.26	-1.26	3.465	-3.465	5.25	-5.25
	TTF	3 lots>34 yr DC	3 lots>71 yr DC	3 lots>20 yr AC*	3 lots>680 yr DC	3 lots>3.5e6s DC**	3 lots>1e9 s DC

TDDB @ 100C	Device	LVN	LVP	MVN	MVN Accum	MVP	Intermed. IMD	Semi-Global IMD
	Vg	1.26	-1.26	3.465	3.465	-3.465	3.465	3.465
	Max Area	2.2 cm^2	22 cm^2	1 cm^2	1 cm^2	2.5 cm^2	L/S=100nm	L/S=200nm
	0.1% TTF	3 lots>2.5e5 yr	3 lots>1.4e3 yr	3 lots>25 yr	3 lots>42 yr	3 lots>390 yr	3 lots>230 yr	3 lots>6600 yr

TDDB @ 100C	Device	HVN	HVN	HVN	HVN Accum	HVN Accum	HVN Accum
	Vg	5.5	6.75	8.8	5.5	6.75	8.8
	Max Area	5e-4 cm^2	2e-4 cm^2	2e-4 cm^2	5e-4 cm^2	2e-4 cm^2	2e-4 cm^2
	0.1% TTF	3 lots>1.3e3 yr	3 lots>134 yr	3 lots>2.3e4 hr***	3 lots>1.2e3 yr	3 lots>128 yr	3 lots>2.3e4 hr***

TDDB @ 100C	Device	HVP	HVP	HVP	HVP Accum	HVP Accum	HVP Accum
	Vg	-5.5	-6.75	-8.8	-5.5	-6.75	-8.8
	Max Area	5e-4 cm^2	2e-4 cm^2	2e-4 cm^2	5e-4 cm^2	2e-4 cm^2	2e-4 cm^2
	0.1% TTF	3 lots>230 yr	3 lots>167 yr	3 lots>9.5e3 hrs***	3 lots>20 yr	3 lots>17 yr	3 lots>1310 hrs***

NBTI @ 100C	Device	LVP	MVP		Device	LVP	MVP
	delta Vth	50mv	100mv		delta Ids	10%	10%
	Vg	-1.26	-3.465		Vg	-1.26	-3.465
	TTF	3 lots>5.8e5 yr	3 lots>4.2e3 yr		TTF	3 lots>1.9e4 yr	3 lots>9.9e5 yr

EML @ 100C	Device	Intermediate	Semi-Global	Global	Top Al
	delta R	+5%	+5%	+5%	+5%
	Jmax	6.65E+05	6.65E+05	6.65E+05	2.85E+05
	0.1% TTF	3 lots>380 yr	3 lots>77 yr	3 lots>22 yr	3 lots>71 yr

SM @ 100C	Device	Intermediate	Semi-Global	Global
	delta R	+100%	+100%	+100%
	TTF	3 lots>2400 yr	3 lots>328 yr	3 lots>1.1e4 yr

All time-to-fail (TTF) data rounded to 2 significant digits
* AC corresponds to 2% Isub duty cycle for inverter which is factor of 50 times DC TTF
** Maximum FLASH Memory Reads are limited to 7.5E13 cycles over the lifetime of the product.
*** 8.8V Vpp TTF is minimum 150 hrs
Note: Reliability life times are based on listed temperature and used conditions. Detailed WLR test conditions are available upon request.

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6.0 PLATFORM MANAGER 2 ADDITIONAL FAMILY DATA

Table 6.01 Package Assembly Data

Package Attributes / Assembly Sites	ASEM		
Die Family (Product Line)	L-ASC10	ASC + FPGA	ASC + FPGA
Wafer Fabrication Process	EE8A	EE8A & CS200F	EE8A & CS200F
+Package Assembly Site	Malaysia	Malaysia	Malaysia
Package Type	QFN	TQFP	ftBGA
Die Configuration	Single Die	Stacked Die	Multi-Chip Module
Pin Count	48	128	237
Die Preparation/Singulation	wafer saw, full cut	wafer saw, full cut	wafer saw, full cut
Die Attach Material	CRM1076DS	FH900 + Si Spacer	Ablestik 2100A
Mold Compound	CEL-9240HF10AK	CEL-9510HFL-U	G2250
Wire Bond Material	Gold (Au) (2N)	Gold (Au) (2N)	Gold (Au) (2N)
Wire Bond Diameter	0.8mil bondwire	0.7mil Au bondwire	0.7mil bondwire
Wire Bond Methods	Thermosonic Ball	Thermosonic Ball	Thermosonic Ball
Lead frame or Substrate Material	C194	A07881-0	Green, AUS308, CL832NX
Lead Finish or Solder Balls	100% Sn	Matte Sn (annealed)	SAC 305
Marking	Laser	Laser	Laser

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7.0 REVISION HISTORY

Table 7.0.1 Platform Manager 2 Product Family Qualification Summary Revisions

Date	Revision	Request	Section	Change Summary
April 2014	A		---	New release
October 2014	B			PTM21-237ftBGA update; remove Jedec revision level from Table 2.2; update Qual Flow chart

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