Lattice M4 / M4A3 / M4A5 Product Family Qualification Summary

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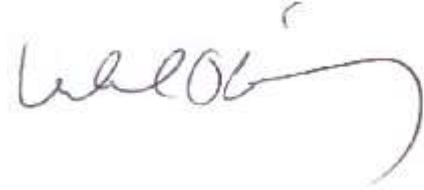
Dear Customer,

Welcome to the Lattice Semiconductor Corp. M4 / M4A3 / M4A5 Product Family Qualification Report. This report reflects our continued commitment to product quality and reliability. The information in this report is drawn from an extensive qualification program of the wafer technology and packaging assembly processes used to manufacture our products. The program adheres to JEDEC and Automotive Industry standards for qualification of the technology and device packaging. This program ensures you only receive product that meets the most demanding requirements for Quality and Reliability.

The information contained in this document is extensive, and represents the entire qualification effort for this device family. Our goal is to provide this information to support your decision making process, and to facilitate the selection and use of our products.

As always, your feedback is valuable to Lattice. Our goal is to continuously improve our systems, including the generation of this report and the data included. Please feel free to forward your comments and suggestions to your local Lattice representative. We will use that feedback carefully and wisely in our effort to maximize customer satisfaction.

Sincerely,



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1.0 INTRODUCTION

The ispMACH™ 4A family from Lattice offers an exceptionally flexible architecture and delivers a superior Complex Programmable Logic Device (CPLD) solution of easy-to-use silicon products and software tools. The overall benefits for users are a guaranteed and predictable CPLD solution, faster time-to-market, greater flexibility and lower cost. The ispMACH 4A devices offer densities ranging from 32 to 512 macrocells with 100% utilization and 100% pin-out retention. The ispMACH 4A families offer 5-V (M4A5-xxx) and 3.3-V (M4A3-xxx) operation.

Table 1.1 Lattice ispMACH™ 4A Product Family Attributes

3.3 V Devices								
Feature	**M4A3-32**	**M4A3-64**	**M4A3-96**	**M4A3-128**	**M4A3-192**	**M4A3-256**	**M4A3-384**	**M4A3-512**
Macrocells	32	64	96	128	192	256	384	512
User I/O options	32	32/64	48	64	96	128/160/192	160/192	160/192/256
t_{PD} (ns)	5.0	5.5	5.5	5.5	6.0	5.5	6.5	7.5
f_{CNT} (MHz)	182	167	167	167	160	167	154	125
t_{COS} (ns)	4.0	4.0	4.0	4.0	4.5	4.0	4.5	5.5
t_{SS} (ns)	3.0	3.5	3.5	3.5	3.5	3.5	3.5	5.0
Static Power (mA)	20	25/52	40	55	85	110/150	149/155	179
JTAG Compliant	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes
PCI Compliant	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes

5 V Devices						
Feature	**M4A5-32**	**M4A5-64**	**M4A5-96**	**M4A5-128**	**M4A5-192**	**M4A5-256**
Macrocells	32	64	96	128	192	256
User I/O options	32	32	48	64	96	128
t_{PD} (ns)	5.0	5.5	5.5	5.5	6.0	6.5
f_{CNT} (MHz)	182	167	167	167	160	154
t_{COS} (ns)	4.0	4.0	4.0	4.0	4.5	5.0
t_{SS} (ns)	3.0	3.5	3.5	3.5	3.5	3.5
Static Power (mA)	20	25	40	55	74	110
JTAG Compliant	Yes	Yes	Yes	Yes	Yes	Yes
PCI Compliant	Yes	Yes	Yes	Yes	Yes	Yes

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2.0 LATTICE PRODUCT QUALIFICATION PROGRAM

Lattice Semiconductor Corp. maintains a comprehensive reliability qualification program to assure that each product achieves its reliability goals. After initial qualification, the continued high reliability of Lattice products is assured through ongoing monitor programs as described in Reliability Monitor Program Procedure (Doc. #70-101667). All product qualification plans are generated in conformance with Lattice Semiconductor's Qualification Procedure (Doc. #70-100164) with failure analysis performed in conformance with Lattice Semiconductor's Failure Analysis Procedure (Doc. #70-100166). Both documents are referenced in Lattice Semiconductor's Quality Assurance Manual, which can be obtained upon request from a Lattice Semiconductor sales office or downloaded from the lattice website at www.latticesemi.com. Figure 2.1 shows the Product Qualification Process Flow.

If failures occur during qualification, an 8-Discipline (8D) process is used to find root cause and eliminate the failure mode from the design, materials, or process. The effectiveness of any fix or change is validated through additional testing as required. Final testing results are reported in the qualification reports.

Failure rates in this reliability report are expressed in FITS. Due to the very low failure rate of integrated circuits, it is convenient to refer to failures in a population during a period of 10^9 device hours; one failure in 10^9 device hours is defined as one FIT.

Product families are qualified based upon the requirements outlined in Table 2.2. In general, Lattice Semiconductor follows the current Joint Electron Device Engineering Council (JEDEC) and Military Standard testing methods. Lattice automotive products are qualified and characterized to the Automotive Electronics Council (AEC) testing requirements and methods. Product family qualification will include products with a wide range of circuit densities, package types, and package lead counts. Major changes to products, processes, or vendors require additional qualification before implementation.

The ispMACH™ 4A product family is built on EE8 which is a 3.3V shallow trench isolated, 0.35um drawn / 0.25um Leff CMOS process with Electrically Erasable cell (E2 cell). This process uses three planarized metal interconnect layers and single layer polysilicon at either United Microelectronics Company (UMC), or Epson Sakata, and assembled at Advance Semiconductor Engineering Malaysia (ASEM), Amkor Korea and UNISEM Group Singapore, in TQFP and QFNS packages.

To verify product reliability, Lattice Semiconductor maintains an active Reliability Monitor program on the ispMACH™ 4A products. Lattice Semiconductor publishes the Reliability Monitor Data quarterly.

Lattice Semiconductor maintains a regular reliability monitor program. The current Lattice Reliability Monitor Report can be found at www.latticesemi.com/lit/docs/qa/product_reliability_monitor.pdf .

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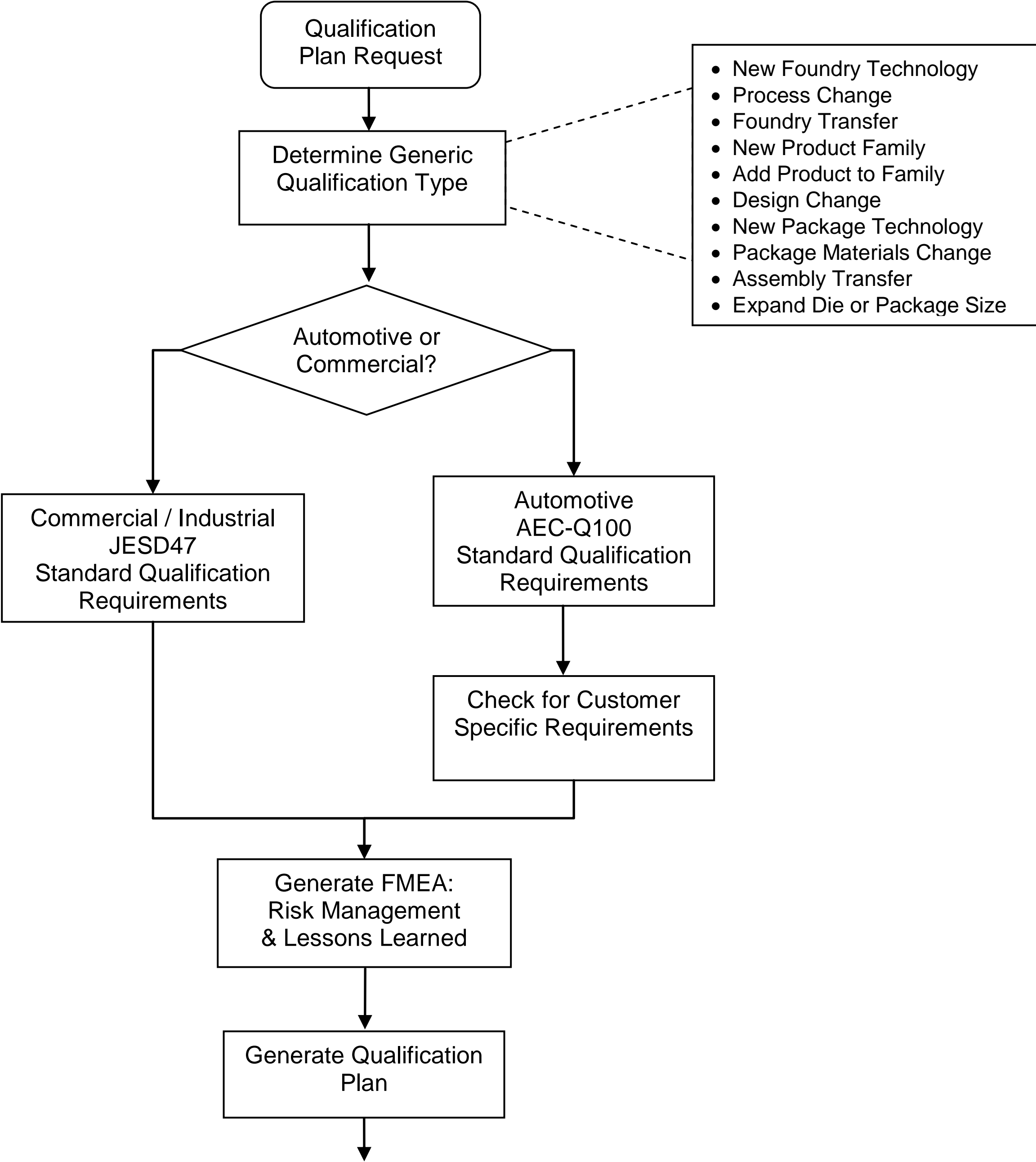
Figure 2.1: ispM4A Product Qualification Process Flow



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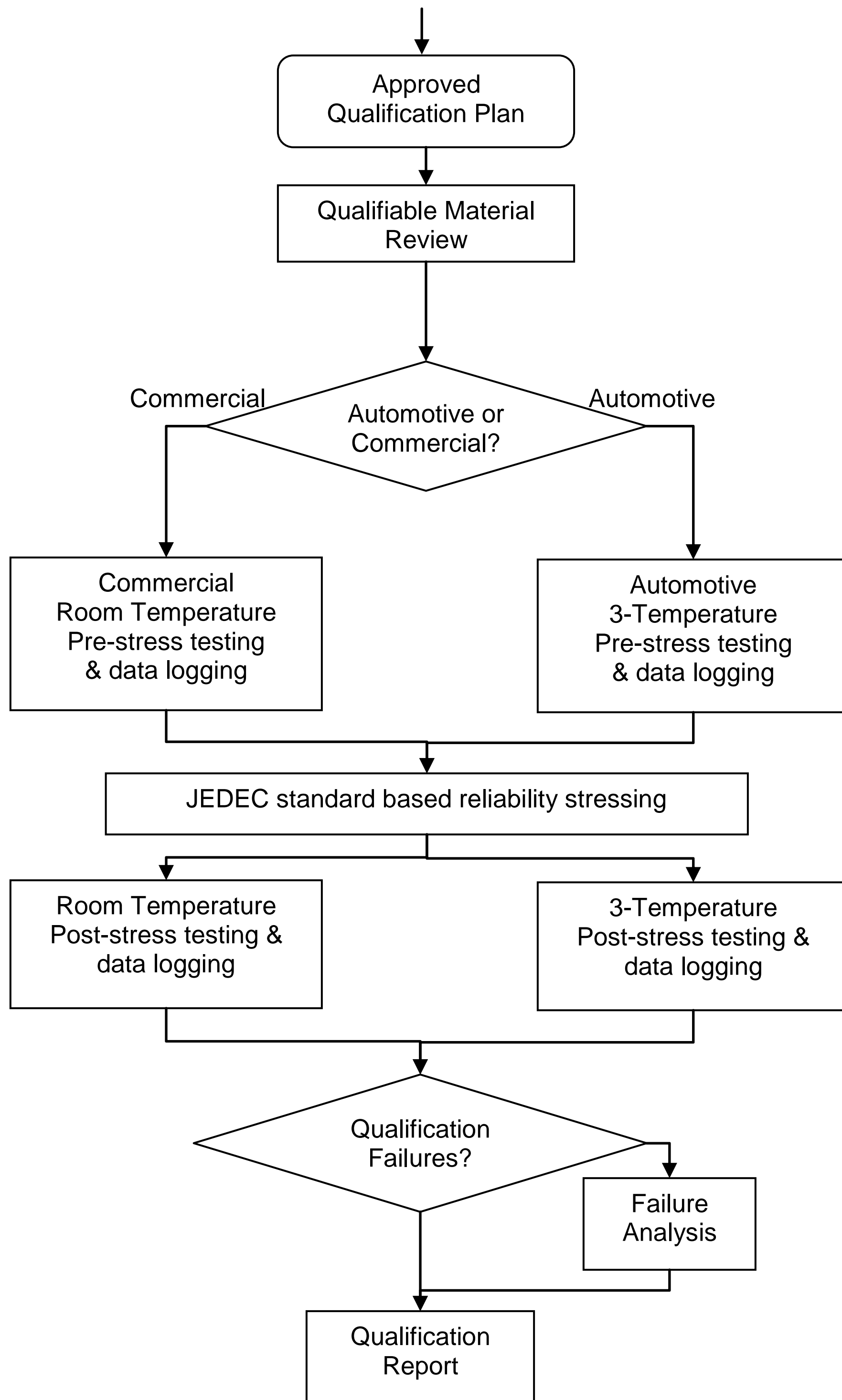

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Table 2.2: Standard Qualification Testing

TEST	STANDARD	TEST CONDITIONS	SAMPLE SIZE (Typ)	PERFORMED ON
High Temperature Operating Life HTOL	Lattice Procedure # 87-101943, MIL-STD-883, Method 1005.8, JESD22-A108D ispMACH 4A	125° C, Maximum operating Vcc, 168, 500, 1000, 2000 hrs. Preconditioned with 100 read/write cycles	77/lot 2-3 lots	Design, Foundry Process, Package Qualification
High Temp Data Retention HTRX	Lattice Procedure # 87-101925, JESD22-A103D JESD22-A117B ispMACH 4A	150° C, Maximum operating Vcc, 168, 500, 1000, 2000 hrs. Preconditioned with 100 read/write cycles	77/lot 2-3 lots	Design, Foundry Process, Package Qualification E^2 Cell Products Flash based Products
High Temp Storage Life HTSL	Lattice Procedure # 87-101925, JESD22-A103D ispMACH 4A	150° C, at 168, 500, 1000, 2000 hours.	77/lot 2-3 lots	Design, Foundry Process, Package Qualification
Endurance - Program/Erase Cycling Non-volatile Products	Lattice Procedure, # 70-104633 JESD22-A117B	Program/Erase devices to 1,000 cycles Program/Erase devices to 10X cycles of data sheet specification	10/lot 2-3 lots typical	Design, Foundry Process, Package Qualification.
ESD HBM	Lattice Procedure # 70-100844, MIL-STD-883, Method 3015.7 JESD22-A114F	Human Body Model (HBM) sweep to 2000 volts – (130nm and older)	3 parts/lot 1-3 lots typical	Design, Foundry Process
ESD CDM	Lattice Procedure # 70-100844, JESD22-C101E	Charged Device model (CDM) sweep to 1000 volts (130nm and older)	3 parts/lot 1-3 lots typical	Design, Foundry Process
Latch Up Resistance LU	Lattice Procedure # 70-101570, JESD78C	±100 ma on I/O's, Vcc +50% on Power Supplies. (Max operating temp.)	6 parts/lot 1-3 lots typical	Design, Foundry Process
Surface Mount Pre-conditioning SMPC	Lattice Procedure # 70-103467, IPC/JEDEC J-STD-020D.1 JESD-A113F CPLD/FPGA - MSL 3	10 Temp cycles, 24 hr 125° C Bake 192hr. 30/60 Soak 3 SMT simulation cycles	All units going into Temp Cycling, UHAST, BHAST, 85/85	Plastic Packages only
Temperature Cycling TC	Lattice Procedure #70-101568, MIL-STD- 883, Method 1010, Condition B JESD22-A104D	(1000 cycles) Repeatedly cycled between -55° C and +125° C in an air environment	45 parts/lot 2-3 lots	Design, Foundry Process, Package Qualification
Unbiased HAST UHAST	Lattice Procedure # 70-104285 JESD22-A118	2 atm. Pressure, 96 hrs, 130 C, 85% Relative Humidity	45 parts/lot 2-3 lots	Foundry Process, Package Qualification Plastic Packages only

TEST	STANDARD	TEST CONDITIONS	SAMPLE SIZE (Typ)	PERFORMED ON
Moisture Resistance Temperature Humidity Bias 85/85 THBS or Biased HAST BHAST	Lattice Procedure # 70-101571, JESD22-A101C JESD22-A110C	Biased to maximum operating Vcc, 85° C, 85% Relative Humidity, 1000 hours or Biased to maximum operating Vcc, 2atm. Pressure, 96 hrs, 130 C, 85% Relative Humidity	45 devices/lot 2-3 lots	Design, Foundry Process, Package Qualification Plastic Packages only
Wire Bond Strength	Lattice Procedure # 70-100220	Per package type	15 devices per pkg. per year	Design, Foundry Process, Package Qualification

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3.0 SILICON QUALIFICATION DATA FOR ispMACH™ 4A Product Family

The ispMACH™ 4A product family is built on EE8 which is a 3.3V shallow trench isolated, 0.35um drawn / 0.25um Leff CMOS process with Electrically Erasable (E2) cells. This process uses three planarized metal interconnect layers and single layer polysilicon fabricated at either United Microelectronics Company (UMC), or Epson Sakata, and assembled at Advance Semiconductor Engineering Malaysia (ASEM), Amkor Korea and UNISEM Group Singapore, in TQFP packages. To verify product reliability, Lattice Semiconductor maintains an active Reliability Monitor program on the ispMACH™ 4A products. Lattice Semiconductor publishes the Reliability Monitor Data quarterly.

Product Family: MACH4, ispMACH4A
Packages offered: 100 TQFP, 84 PLCC
Process Technology Node: 0.35um drawn / 0.25um Leff CMOS

3.1 Product Family Life Data

High Temperature Operating Life (HTOL) Test

The High Temperature Operating Life test is used to thermally accelerate those wear out and failure mechanisms that would occur as a result of operating the device continuously in a system application. Consistent with JEDEC JESD22-A108 “Temperature, Bias, and Operating Life”, a pattern specifically designed to exercise the maximum amount of circuitry is programmed into the device and this pattern is continuously exercised at specified voltages as described in test conditions for each device type.

M4A3/M4A5 Life Test (HTOL) Conditions:

Stress Duration: 168, 500, 1000 hours.
Temperature: 125°C
Stress Voltage ispMACH 4A: V_{CC}= 3.6V or 5.5V
Preconditioned with 100 read/write cycles
Method: Lattice Document # 87-101943 and JESD22-A108

Table 3.1.1: EE8 Product Family HTOL Results

Product Name	Foundry	Lot #	Qty	168 Hrs Result	500 Hrs Result	1000 Hrs Result	2000 Hrs Result	Cumulative Hours
ispM4A5-128/64	Seiko Sakata	Lot #1	78*	0	0	0	0	156000
ispM4A5-128/64	Seiko Sakata	Lot #2	78*	0	0	0	0	154000
ispM4A5-128/64	Seiko Sakata	Lot #3	77	0	0	0	0	154000

*Lot #1 with CD process splits
*Lot #2 with Vt process splits

EE8 Cumulative Device Hours = 464,000
EE8 Cumulative Sample Size = 0 / 233
EE8 FIT Rate = 55 FIT

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3.2 High Temperature Data Retention (HTRX)

High Temperature Data Retention (HTRX)

The High Temperature Data Retention test measures the Electrically Erasable cell (E2 cell) reliability while the High Temperature Operating Life test is structured to measure functional operating circuitry failure mechanisms. The High Temperature Data Retention test is specifically designed to accelerate charge gain on to or charge loss off of the floating gates in the device's array. Since the charge on these gates determines the actual pattern and function of the device, this test is a measure of the reliability of the device in retaining programmed information. In High Temperature Data Retention, the E2 cell reliability is determined by monitoring the cell margin after biased static operation at 150°C. All cells in all arrays are life tested in both programmed and erased states.

Data Retention (HTRX) Conditions:

Stress Duration: 168, 500, 1000 hours.
Temperature: 150°C
Preconditioned with 100 read/write cycles
Method: Lattice Document # 87-101925 and JESD22-A103 / JESD22-A117

Table 3.2.1: ispMACH 4A High Temperature Data Retention Results

Product Name	Foundry	Lot #	Qty	168 Hrs Result	500 Hrs Result	1000 Hrs Result	2000 Hrs Result	Cumulative Hours
ispM4A5-128/64	Seiko Sakata	Lot #1	77	0	0	0	0	154000
ispM4A5-128/64	Seiko Sakata	Lot #2	77	0	0	0	0	154000
ispM4A5-128/64	Seiko Sakata	Lot #3	78*	0	0	0	0	154000

*Lot #3 with tunnel oxide process splits

Cumulative HTRX Failure Rate = 0 / 232
Cumulative HTRX Device Hours = 462,000

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3.3 Extended Endurance (EE)

Extended Endurance (EE)
Extended Endurance testing measures the durability of the device through programming and erase cycles. Extended Endurance testing consists of repeatedly programming and erasing all E2 cells in the array at 25°C to simulate programming cycles the user would perform. This test evaluates the integrity of the thin tunnel oxide through which current passes to program the floating gate in each cell of the array.

Extended Endurance (EE) Conditions:
Stress Duration: 1000 cycles.
Temperature: 25°C
Method: Lattice Document # 70-104633 and JESD22-A117

Table 3.3.1: ispMACH 4A Extended Endurance Results

Product Name	Foundry	Lot #	Qty	0 Cycles Result	1000 Cycles Result
ispM4A5-128/64	Seiko Sakata	Lot #1	10	0	0
ispM4A5-128/64	Seiko Sakata	Lot #2	10	0	0
ispM4A5-128/64	Seiko Sakata	Lot #3	10	0	0
ispM4A5-128/64	Seiko Sakata	Lot #4	10	0	0
ispM4A5-128/64	Seiko Sakata	Lot #5	10	0	0

*Lot #4 is a thin tunnel oxide process split

*Lot #5 is a thick tunnel oxide process split

Cumulative EE Failure Rate = 0 / 50

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3.4 High Temperature Data Retention (HTDR)

High Temperature Data Retention (HTDR)
High Temperature Data Retention measures the ability of the E2 cell to meet the company's retention goal of >10 years at Tjrel, including the effect of Write-Erase cycling to the product specification. HTDR is a wafer-level test.

High Temperature Data Retention (HTDR) Conditions:
Stress Duration: 1000 hours.
Temperature: 250°C
Preconditioned with 100 read/write cycles.
Method: Lattice Document # 87-106567 and JESD22-A117

Table 3.4.1: ispMACH 4A High Temperature Data Retention Results

Product Name	Foundry	Wafer #	Split	Die Qty	0 Hour Result	1000 Hour Result
ispM4A5-128/64	Seiko Sakata	Wafer #1	Thick Oxide	15	0	0
ispM4A5-128/64	Seiko Sakata	Wafer #2	Thin Oxide	20	0	0
ispM4A5-128/64	Seiko Sakata	Wafer #3	Nominal	18	0	0

All splits pass >>10 years lifetime at Tjrel = 130°C

Cumulative HTDR Failure Rate = 0 / 53

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3.5 Product Family – ESD and Latch UP Data

Electrostatic Discharge-Human Body Model:

ispMACH 4A product family fabricated at Seiko Sakata was tested per the JESD22-A114 Electrostatic Discharge (ESD) Sensitivity Testing Human Body Model (HBM) procedure and Lattice Procedure # 70-100844. All units were tested at 25^{0}C prior to reliability stress and after reliability stress. No failures were observed within the passing classification.

Table 3.5.1 ispMACH 4A Seiko Sakata ESD-HBM Data

Product	100-TQFP	100-csBGA	100-PQFP	84-PLCC
ispM4A3-64/64	>2000V Class 2			
ispM4A5-128/64	>2000V Class 2	>2000V Class 2	>2000V Class 2	
ispM4A3-128/64	>2000V Class 2	>2000V Class 2	>2000V Class 2	
M4-128N				>2000V Class 2

HBM classification for Commercial/Industrial products, per JESD22-A114

Electrostatic Discharge-Charged Device Model:

ispMACH 4A product family fabricated at Seiko Sakata was tested per the JESD22-C101, Field-Induced Charged-Device Model Test Method for Electrostatic-Discharge-Withstand Thresholds of Microelectronic Components procedure and Lattice Procedure # 70-100844.

All units were tested at 25^{0}C prior to reliability stress and after reliability stress. No failures were observed within the passing Classification.

Table 3.5.2 ispMACH 4A Seiko Sakata ESD-CDM Data

Product	100-TQFP	100-csBGA	100-PQFP	84-PLCC
ispM4A3-64/64	>1000V Class IV			
ispM4A5-128/64	>1000V Class IV	>1000V Class IV	>1000V Class IV	
ispM4A3-128/64	>1000V Class IV	>1000V Class IV	>1000V Class IV	
M4-128N				>1000V Class IV

CDM classification for Commercial/Industrial products, per JESD22-C101

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Latch-Up:

The ispMACH 4A product family was tested per the JEDEC EIA/JESD78 IC Latch-up Test procedure and Lattice Procedure # 70-101570.

All units were tested at 25^{0}C prior to reliability stress and after reliability stress. No failures were observed within the passing Classification.

Table 3.5.3 ispMACH 4A I/O Latch-Up >100mA @ HOT (105°C) Data

Product	100-TQFP	100-csBGA	100-PQFP	84-PLCC
ispM4A3-64/64	>+/- 100mA Class II, Level A			
ispM4A5-128/64	>+/- 100mA Class II, Level A	>+/- 100mA Class II, Level A	>+/- 100mA Class II, Level A	
ispM4A3-128/64	>+/- 100mA Class II, Level A	>+/- 100mA Class II, Level A	>+/- 100mA Class II, Level A	
M4-128N				>+/- 100mA Class II, Level A

Table 3.5.4 ispMACH 4A Vcc Latch-Up >1.5X @ HOT (105°C) Data

Product	100-TQFP	100-csBGA	100-PQFP	84-PLCC
ispM4A3-64/64	>1.5x Vccmax			
ispM4A5-128/64	>1.5x Vccmax	>1.5x Vccmax	>1.5x Vccmax	
ispM4A3-128/64	>1.5x Vccmax	>1.5x Vccmax	>1.5x Vccmax	
M4-128N				>1.5x Vccmax

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4.0 PACKAGE QUALIFICATION DATA FOR M4A3/M4A5-128/64 Products

The primary package for the ispM4A3-128/64 and ispM4A5-128/64 is the 100TQFP assembled at ASE Malaysia. Package qualification tests include Surface Mount Preconditioning (SMPC), Temperature Cycling (T/C), Un-biased HAST (UHAST) and Biased HAST (BHAST). Mechanical evaluation tests include Scanning Acoustic Tomography (SAT) and visual package inspection.

Table 4.0 Product-Package Qualification-By-Extension Matrix

Products	Stress Test	Advanced Semiconductor Engineering, Malaysia (ASEM)			
		100-TQFP	**100-csBGA**	**100-PQFP**	**84-PLCC**
M4A3-64	SMPC T/C BHAST UHAST HTSL	(1)	Package not offered	Package not offered	Package not offered
M4A3-128	SMPC T/C BHAST UHAST HTSL	(1)	No package BOM changes	No package BOM changes	Package not offered
M4A5-128	SMPC	MSL3 260°C	No package BOM changes	No package BOM changes	Package not offered
	T/C	1000 cycles			
	BHAST	96 hours			
	UHAST	96 hours			
	HTSL	1000 hours			
M4-128	SMPC T/C BHAST UHAST HTSL	Packages not offered			No package BOM changes

Notes:

1 – Qualified by extension from Lattice ispM4A5-128 testing.

4.1 Surface Mount Preconditioning Testing

The Surface Mount Preconditioning (SMPC) Test is used to model the surface mount assembly conditions during component solder processing. All devices stressed through Temperature Cycling, Un-biased HAST and Biased HAST were preconditioned. This preconditioning is consistent with JEDEC JESD22-A113 "Preconditioning Procedures of Plastic Surface Mount Devices Prior to Reliability Testing", Moisture Sensitivity Level 3 (MSL3) package moisture sensitivity and dry-pack storage requirements.

Consistent with Lattice Semiconductor Corp. document # 25-100164, package reliability testing can be qualified by extension. Once a package outline is qualified within a package grouping as per doc #70-103639, all lower lead count (and smaller body size) packages within that package type and assembly technology are qualified by extension. Additionally, once an assembly technology has been qualified for one package type, that package type shall be qualified by extension to all future fabrication processes as long as those processes continue to use the same critical elements. Those critical elements in this case, are that the process-to-process interlayer dielectric material and thickness differences do not exceed the current production process limits for the qualification vehicle used. For 180nm and older technologies, the critical elements are considered equivalent.

Surface Mount Preconditioning (MSL3)
(10 Temperature Cycles between -55°C and 125°C, 24 hours bake @ 125°C, 30°C/60% RH, soak 192 hours, Reflow Simulation, 3 passes) performed before all ispMach4A package tests.
MSL3 Package: TQFP

Table 4.1.1 Surface Mount Precondition Data

Product Name	Package	Assembly Site	Lot Number	Quantity	# of Fails	Reflow Temperature
ispM4A5-128/64	100 TQFP	ASEM	Lot #1	314	0	260°C
ispM4A5-128/64	100 TQFP	ASEM	Lot #2	314	0	260°C
ispM4A5-128/64	100 TQFP	ASEM	Lot #3	397	0	260°C

Cumulative SMPC Failure Rate = 0 / 1,025

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4.2 High Temperature Storage Life (HTSL) Data

High Temperature Storage Life (HTSL)

High Temperature storage test is typically used to determine the effect of time and temperature, under storage conditions, for thermally activated failure mechanisms of solid state electronic devices. Units were stressed per JESD22-A103, High Temperature Storage Life. Prior to High Temperature Storage Life testing, all devices are subjected to Surface Mount Preconditioning. The High Temperature Storage Life units were stressed at 150°C.

High Temperature Storage Life (HTSL) Conditions:
Stress Duration: 168, 500, 1000, hours.
Temperature: 150°C
Method: Lattice Document # 87-101925 and JESD22-A103 / JESD22-A117

Table 4.2.1: High Temperature Storage Life Results

Product Name	Assembler	Package	Lot #	Qty	168 Hrs Result	500 Hrs Result	1000 Hrs Result	Cumulative Hours
ispM4A5-128/64	ASEM	100 TQFP	Lot #1	77	0	0	0	77000
ispM4A5-128/64	ASEM	100 TQFP	Lot #2	77	0	0	0	77000
ispM4A5-128/64	ASEM	100 TQFP	Lot #3	77	0	0	0	77000

Cumulative HTSL Failure Rate = 0 / 231
Cumulative HTSL Device Hours = 231,000

4.3 Temperature Cycling Data

The Temperature Cycling test is used to accelerate those failures resulting from mechanical stresses induced by differential thermal expansion of adjacent films, layers and metallurgical interfaces in the die and package. Devices are tested at 25°C after exposure to repeated cycling between -55°C and +125°C in an air environment consistent with JEDEC JESD22-A104 “Temperature Cycling”, Condition B temperature cycling requirements. Prior to Temperature Cycling testing, all devices are subjected to Surface Mount Preconditioning.

MSL3 Packages: TQFP
Stress Duration: 1000 cycles
Stress Conditions: Temperature cycling between -55°C to 125°C
Method: Lattice Procedure # 70-101568 and JESD22-A104

Table 4.3.1: Temperature Cycling Data

Product Name	Package	Assembly Site	Lot Number	Quantity	250 Cycles	500 Cycles	1000 Cycles
ispM4A5-128/64	100 TQFP	ASEM	Lot #1	83	0	0	0
ispM4A5-128/64	100 TQFP	ASEM	Lot #2	83	0	0	0
ispM4A5-128/64	100 TQFP	ASEM	Lot #3	84	0	0	0

Cumulative Temp Cycle Failure Rate = 0 / 250

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4.4 Unbiased HAST Data

Unbiased Highly Accelerated Stress Test (HAST) testing uses both pressure and temperature to accelerate penetration of moisture into the package and to the die surface. The Unbiased HAST test is designed to detect ionic contaminants present within the package or on the die surface, which can cause chemical corrosion. Consistent JEDEC JESD22-A118, "Accelerated Moisture Resistance - Unbiased HAST," the Unbiased HAST conditions are 96 hour exposure at 130°C, 85% relative humidity, and 2 atmospheres of pressure. Prior to Unbiased HAST testing, all devices are subjected to Surface Mount Preconditioning.

MSL3 Package: TQFP
Stress Duration: 96 Hrs
Stress Conditions: 130°C, 15psig, 85% RH
Method: Lattice Procedure # 70-104285 and JESD22-A118

Table 4.3.1: Unbiased HAST Data

Product Name	Package	Assembly Site	Lot Number	Quantity	# of Fails	Stress Duration
ispM4A5-128/64	100 TQFP	ASEM	Lot #1	77	0	96 Hrs
ispM4A5-128/64	100 TQFP	ASEM	Lot #2	77	0	96 Hrs
ispM4A5-128/64	100 TQFP	ASEM	Lot #3	77	0	96 Hrs

Cumulative Unbiased HAST failure Rate = 0 / 231

4.5 THB: Biased HAST Data

Highly Accelerated Stress Test (HAST) testing uses both pressure and temperature to accelerate penetration of moisture into the package and to the die surface. The Biased HAST test is used to accelerate threshold shifts in the MOS device associated with moisture diffusion into the gate oxide region as well as electrochemical corrosion mechanisms within the device package. Consistent with JEDEC JESD A110-B "Highly-Accelerated Temperature and Humidity Stress Test (HAST)", the biased HAST conditions are with Vcc bias and alternate pin biasing in an ambient of 130°C, 85% relative humidity, and 2 atmospheres of pressure. Prior to Biased HAST testing, all devices are subjected to Surface Mount Preconditioning.

MSL3 Packages: TQFP
Stress Conditions: ispMACH 4A5-128/64 Vcc= 5.5 V, 130°C / 85% RH, 15 psig
Stress Duration: 96 hours
Method: Lattice Procedure # 70-101571 and JESD22-A101

Table 4.4.1: Biased HAST Data

Product Name	Package	Assembly Site	Lot Number	Quantity	# of Fails	Stress Duration
ispM4A5-128/64	100 TQFP	ASEM	Lot #1	77	0	96 Hrs
ispM4A5-128/64	100 TQFP	ASEM	Lot #2	77	0	96 Hrs
ispM4A5-128/64	100 TQFP	ASEM	Lot #3	77	0	96 Hrs

Cumulative BHAST failure Rate = 0 / 1,124

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5.0 Seiko-Sekata EE8 Fab Process – Wafer Level Reliability

Several key fabrication process related parameters have been identified by the foundry that would affect the Reliability of the End-of-Life Product. These parameters are tested during the Development Phase of the Technology. Passing data (a 10yr lifetime at the reliability junction temperature) must be obtained for three lots minimum for each parameter before release to production. Normal operating conditions are defined in the Electrical Design Rules (EDR). These parameters are:

Hot Carrier Immunity (**HCI**): Effect is a reduction in transistor Idsat. Worst case is low temperature.
Time Dependent Dielectric Breakdown (**TDDB**): Transistor and capacitor oxide shorts or leakage.
Negative Bias Temperature Instability (NBTI): Degradation of P channel transistors at negative Vg.
Electromigration Lifetime (**EML**): Symptom is opens within, or shorts between, metal conductors.
Stress Migration (SM): Microscopic voids may exist in Tungsten plug-Aluminum CMP-SiO2 IMD structures.

Table 5.1 – Wafer Level Reliability Results for EE8 (0.35um) Process Technology

HCI

Device	LVN	LVP	HVN	HVP
delta Ids	-10%	-10%	-10%	-10%
Celsius	25	25	25	25
Vgstress	Vd/2	Vd	Vd/2	Vd
Vds	3.6	-3.6	5.5	-5.5
TTF	3 lots>58yr AC	lots>5.4e4yr DC	2 lots>525yr DC	2 lots>5.5e8yr DC

TDDB

Device	LVN	LVP	HVN	HVP
Celsius	130	130	130	130
Vg	3.6	-3.6	5.5	-5.5
0.1% TTF	3 lots>2750 yr	2 lots>4.1e4yr	3 lots>2.1e3yr	2 lots>1.8e3yr

NBTI

Device	LVP	HVP
delta Vth	100mv	100mv
Celsius	130	130
Vg	-3.6	-5.5
TTF	2 lots>13.4 yr	2 lots>1840yr

EML

Device	M1	M2	M3
Celsius	130	130	130
delta R	+10%	+10%	+10%
Jmax	2.00E+05	2.00E+05	2.00E+05
0.1% TTF	3 lots>18 yr	3 lots>30 yr	3 lots>17 yr

SM

Device	M1	M2	M3
delta R	+10%	+10%	+10%
condition	175C-1000hr	175C-1000hr	175C-1000hr
TTF	2 lots Pass	2 lots Pass	2 lots Pass

Note: Reliability life times are based on listed temperature and used conditions. Detailed WLR test conditions are available upon request.

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6.0 PACKAGE ASSEMBLY INTEGRITY TESTS

6.1 Wire Bond Pull

This procedure is used to measure the wire bond strength at the ball joints and stitch bonds. For product evaluation 12 bonds from a minimum of five devices for each package lot were used for Wire Bond Pull. Requirement for 0.8 mil gold wire is >3 grams pre-stress, and >0.5 grams post-stress.

WIRE BOND PULL RESULTS:

All bond pull observations post 1000-hours HTSL >4.3 grams.
All bond pull observations post 1000-temp cycles >4.9 grams.

The average measured wire bond pull results for TQFP were Cpk of > 2.

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7.0 ADDITIONAL FAMILY DATA

Table 7.1: ispMACH 4A Package Assembly Data- TQFP

Package Attributes / Assembly Sites	ASEM
Die Family (Product Line)	ispMACH 4A
Fabrication Process Technology	EE8 (0.35um CMOS)
Package Assembly Site	Malaysia
Package Type	TQFP
Pin Count	100
Die Preparation/Singulation	wafer saw, full cut
Die Attach Material - TQFP	Ablebond 3230
Mold Compound Supplier/ID - TQFP	Hitachi CEL9220HF Series
Wire Bond Material	Gold (Au)
Wire Bond Methods	Thermosonic Ball
Lead frame Material	Cu Alloy
Lead Finish	Matte Sn (annealed)
Marking	Laser or Ink

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