Lattice ispPAC-POWR Product Family Qualification Summary

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Dear Customer,

Enclosed is Lattice Semiconductor's ispPAC-POWR Product Family Qualification Summary Product Family Qualification Report.

This report was created to assist you in the decision making process of selecting and using our products. The information contained in this report represents the entire qualification effort for this device family.

The information is drawn from an extensive qualification program of the wafer technology and packaging assembly processes used to manufacture our products. The program adheres to JEDEC and Automotive Industry standards for qualification of the technology and device packaging. This program ensures you only receive product that meets the most demanding requirements for Quality and Reliability.

Your feedback is valuable to Lattice. If you have suggestions to improve this report, or the data included, we encourage you to contact your Lattice representative.

Sincerely,

James M. Orr
Vice President,
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1.0 INTRODUCTION

Lattice ispPAC-POWR devices provide highly accurate, flexible, and low cost solutions for circuit board power supply and processor/DSP supply management. By integrating a versatile PLD core with Analog-to-Digital (ADC) converter, Digital-to-Analog Converters (DAC), differential sense analog monitors, I2C communication, and in-system programmability (isp), Lattice power management devices increase board reliability, decrease component count, and help cut costs. Two power management families: ProcessorPM and Power Manager II address a variety of applications – all in a single low-cost chip.

The ispPAC-POWR product family is built on EE8A which is a 3.3V shallow trench isolated, 0.35um drawn / 0.25um Leff CMOS process with Electrically Erasable (E2) cells. This process uses three planarized metal interconnect layers and single layer polysilicon fabricated at either United Microelectronics Company (UMC) wafer fab, or Epson wafer fab at Sakata, and assembled at Advance Semiconductor Engineering Malaysia (ASEM), Amkor Korea and UNISEM Group Singapore, in TQFP and QFNS packages. To verify product reliability, Lattice Semiconductor maintains an active Early Life and Inherent Life Reliability Monitor program on the ispPAC-POWR products. Lattice Semiconductor publishes the Reliability Monitor Data quarterly.

Table 1.1 Lattice ispPAC-POWR Product Family Attributes

Family	Power Manager II				ProcessorPM
Device Types / Parameter	POWR1220AT8	POWR1014 /A LA-POWR1014/A*	POWR6AT6	POWR607	POWR605
Analog Input Pins	12	10	6	6	6
No. of Programmable Threshold Comparators	24	20	-	6	6
Trip Points per Input	368	368	-	192	192
Typical Precision	0.20%	0.30%	-	0.50%	0.50%
Lowest Supply Voltage Monitored	0.67V	0.67V	-	0.67V	0.67V
Power-Off Detection	75 mV	75 mV	-	75 mV	75 mV
CPLD Macrocells	48	24	-	16	16
No. of Outputs	20 & 8	14	6 trim outputs	7	5
No. of FET Drivers	4	2	-	2	-
Trim Outputs (DACs)	8	-	6	-	-
ADC Support	Yes (10 bit)	Yes (10 bit)* +	Yes (10 bit)	No	No
I2C Interface	Yes	Yes	Yes	No	No
Operating Voltage	2.8V to 3.9V	2.8V to 3.9V	2.8V to 3.9V	2.6V to 3.9V	2.6V to 3.9V
Process Technology	0.35um CMOS	0.35um CMOS	0.35um CMOS	0.35um CMOS	0.35um CMOS
Die Metallization	Al – 0.5% Cu	Al – 0.5% Cu	Al – 0.5% Cu	Al – 0.5% Cu	Al – 0.5% Cu
Die Interconnect Dielectric	Plasma-enhanced TEOS	Plasma-enhanced TEOS	Plasma-enhanced TEOS	Plasma-enhanced TEOS	Plasma-enhanced TEOS
Pins/Packages	100 TQFP (Pb and Pb-Free)	48 TQFP (Pb and Pb-Free)	32 QFNS (Pb and Pb-Free)	32 QFNS (Pb and Pb-Free)	24 QFNS (Pb-Free)

* LA-POWR1014/A is an Automotive product offering.
+ Available only in isPAC-POWR1014A.

Power Manager II devices are Lattice's second generation of fully-programmable power management devices specifically designed for power supply sequencing and monitoring of various power supplies.

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2.0 LATTICE PRODUCT QUALIFICATION PROGRAM

Lattice Semiconductor Corp. maintains a comprehensive reliability qualification program to assure that each product achieves its reliability goals. After initial qualification, the continued high reliability of Lattice products is assured through ongoing monitor programs as described in Reliability Monitor Program Procedure (Doc. #70-101667). All product qualification plans are generated in conformance with Lattice Semiconductor's Qualification Procedure (Doc. #70-100164) with failure analysis performed in conformance with Lattice Semiconductor's Failure Analysis Procedure (Doc. #70-100166). Both documents are referenced in Lattice Semiconductor's Quality Assurance Manual, which can be obtained upon request from a Lattice Semiconductor sales office or downloaded from the lattice website at www.latticesemi.com. Figure 2.1 shows the Product Qualification Process Flow.

If failures occur during qualification, an 8-Discipline (8D) process is used to find root cause and eliminate the failure mode from the design, materials, or process. The effectiveness of any fix or change is validated through additional testing as required. Final testing results are reported in the qualification reports.

Failure rates in this reliability report are expressed in FITS. Due to the very low failure rate of integrated circuits, it is convenient to refer to failures in a population during a period of 10^9 device hours; one failure in 10^9 device hours is defined as one FIT.

Product families are qualified based upon the requirements outlined in Table 2.2. In general, Lattice Semiconductor follows the current Joint Electron Device Engineering Council (JEDEC) and Military Standard testing methods. Lattice automotive products are qualified and characterized to the Automotive Electronics Council (AEC) testing requirements and methods. Product family qualification will include products with a wide range of circuit densities, package types, and package lead counts. Major changes to products, processes, or vendors require additional qualification before implementation.

The ispPAC-POWR product family is built on the 0.35um EE8A Electrically Erasable (E2 cell based) CMOS process at either United Microelectronics Company (UMC) wafer fab, or Epson wafer fab at Sakata, and assembled at Advance Semiconductor Engineering Malaysia, (ASEM), Amkor Technology, Korea and UNISEM Group, Indonesia, in TQFP and QFNS packages. To verify product reliability, Lattice Semiconductor maintains an active Early Life and Inherent Life Reliability Monitor program on the ispPAC-POWR products.

Lattice Semiconductor maintains a regular reliability monitor program. The current Lattice Reliability Monitor Report can be found at www.latticesemi.com/lit/docs/qa/product_reliability_monitor.pdf .

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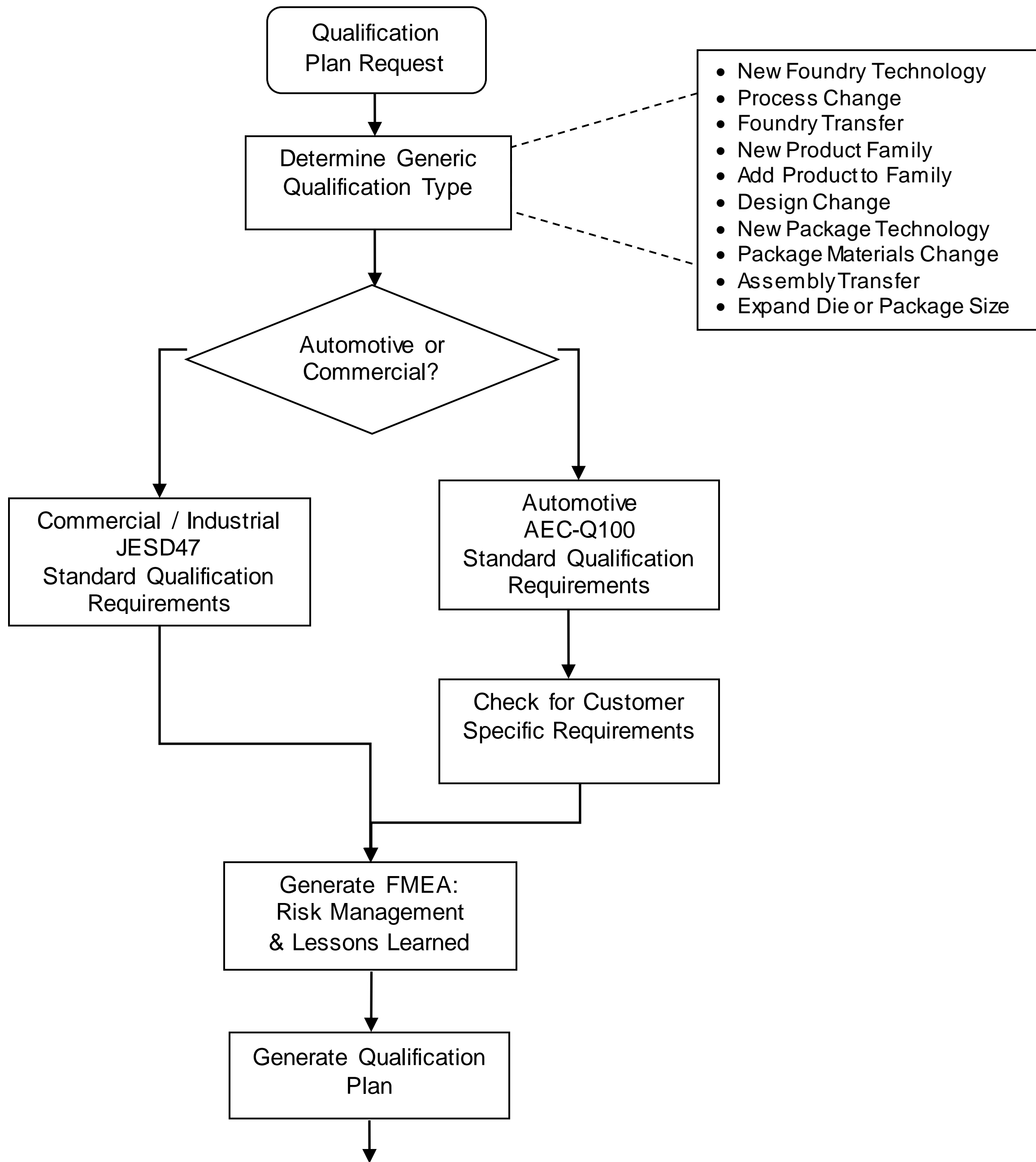
Figure 2.1 ispPAC-POWR Product Qualification Process Flow



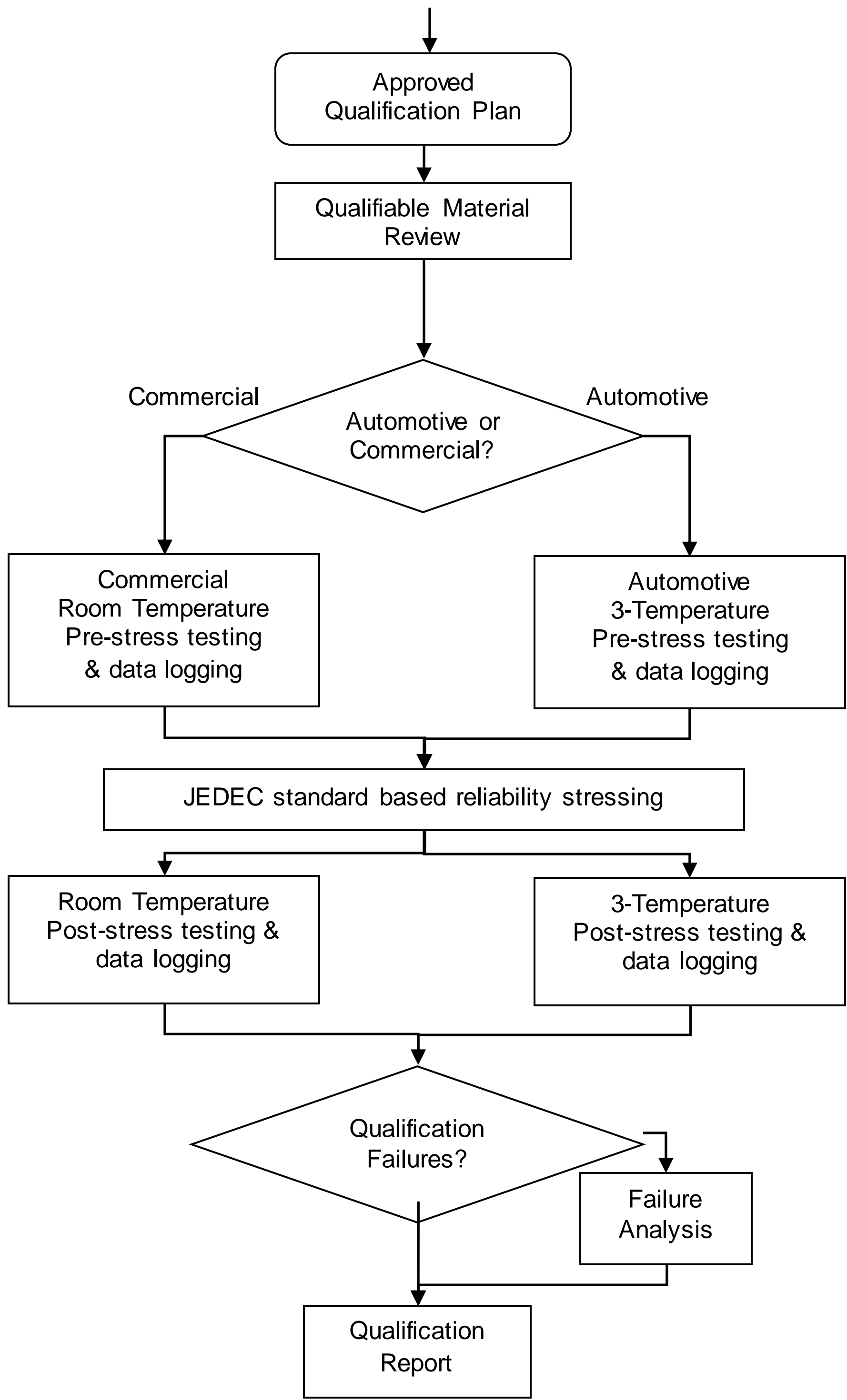


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Table 2.2 Standard Qualification Testing

TEST	STANDARD	TEST CONDITIONS	SAMPLE SIZE (Typ)	PERFORMED ON
High Temperature Operating Life HTOL	Lattice Procedure # 87-101943, MIL-STD-883, Method 1005.8, JESD22-A108C	125° C, Maximum operating Vcc, 168, 500, 1000 hours Preconditioned with 100 program/erase cycles	77/lot 2-3 lots	Product Design and Foundry Process Qualification
High Temp Data Retention HTRX	Lattice Procedure # 87-101925, JESD22-A103C JESD22-A117A	150° C, Maximum operating Vcc, 168, 500, 1000 hours Preconditioned with 100 program/erase cycles	100/lot 2-3 lots	Product Design and Foundry Process Qualification E^2 Cell Products
Endurance - Program/Erase Cycling E^2 Cell Products	Lattice Procedure, # 70-104633 JESD22-A117B	Program/Erase devices to 1000 cycles Program/Erase devices to 10X cycles of data sheet specification	10/lot 2-3 lots typical	Product Design and Foundry Process Qualification
ESD HBM	Lattice Procedure # 70-100844, MIL-STD-883, Method 3015.7 JESD22-A114E	Human Body Model (HBM) sweep to 2000 volts – (130nm and older)	3 parts/lot 1-3 lots typical	Product Design and Foundry Process Qualification
ESD CDM	Lattice Procedure # 70-100844, JESD22-C101D	Charged Device model (CDM) sweep to 1000 volts (130nm and older)	3 parts/lot 1-3 lots typical	Product Design and Foundry Process Qualification
Latch Up Resistance LU	Lattice Procedure # 70-101570, JESD78A	±100 ma on I/O's, Vcc +50% on Power Supplies. (Max operating temp.)	6 parts/lot 1-3 lots typical	Product Design and Foundry Process Qualification
Surface Mount Pre-conditioning SMPC	Lattice Procedure # 70-103467, IPC/JEDEC J-STD-020D.1 JESD-A113F CPLD/FPGA - MSL 3	10 Temp cycles, 24 hr 125° C Bake 192hr. 30/60 Soak 3 SMT simulation cycles	All units going into Temp Cycling, UHAST, BHAST, 85/85	Plastic Packages only
Temperature Cycling TC	Lattice Procedure #70-101568, MIL-STD- 883, Method 1010, Condition B JESD22-A104C	(1000 cycles) Repeatedly cycled between -55° C and +125° C in an air environment	45 parts/lot 2-3 lots	Design, Foundry Process, Package Qualification
High Temp Storage Life HTSL	Lattice Procedure # 87-101925, JESD22-A103C	150° C, at 168, 500, 1000 hours	77/lot 2-3 lots	Design, Foundry Process, Package Qualification
Unbiased HAST UHAST	Lattice Procedure # 70-104285 JESD22-A118	2 atm. Pressure, 96 hrs, 130 C, 85% Relative Humidity	45 parts/lot 2-3 lots	Foundry Process, Package Qualification Plastic Packages only

TEST	STANDARD	TEST CONDITIONS	SAMPLE SIZE (Typ)	PERFORMED ON
Moisture Resistance Temperature Humidity Bias 85/85 THBS or Biased HAST BHAST	Lattice Procedure # 70-101571, JESD22-A101B JESD22-A110B	Biased to maximum operating Vcc, 85° C, 85% Relative Humidity, 1000 hours or Biased to maximum operating Vcc, 2atm. Pressure, 96 hrs, 130 C, 85% Relative Humidity	45 devices/lot 2-3 lots	Design, Foundry Process, Package Qualification Plastic Packages only
Physical Dimensions	Lattice Procedure # 70-100211, MIL-STD- 883 Method 2016 or applicable LSC case outline drawings	Measure all dimensions listed on the case outline.	5 devices	Package Qualification
Wire Bond Strength	Lattice Procedure # 70-100220	Per package type	15 devices per pkg. per year	Design, Foundry Process, Package Qualification
Solderability	Lattice Procedure # 70-100212, MIL-STD-883, Method 2003	Steam Pre-conditioning 4-8 hours. Solder dip at 245°C+5°C	22 leads/ 3 devices/ Package family	All packages except BGAs

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3.0 QUALIFICATION DATA FOR ispPAC-POWR PRODUCT FAMILY

The ispPAC-POWR product family is built on the 0.35um EE8A Electrically Erasable (E2 cell based) CMOS process at United Microelectronics Company (UMC) and assembled at ASEM, Amkor and UNISEM, in TQFP and QFNS packages. To verify product reliability, Lattice Semiconductor maintains an active Early Life and Inherent Life Reliability Monitor program on the ispPAC-POWR products.

3.1 ispPAC-POWR Product Family Life Data

High Temperature Operating Life (HTOL) Test

The High Temperature Operating Life test is used to thermally accelerate those wear out and failure mechanisms that would occur as a result of operating the device continuously in a system application. Consistent with JEDEC JESD22-A108 "Temperature, Bias, and Operating Life", a pattern specifically designed to exercise the maximum amount of circuitry is programmed into the device and this pattern is continuously exercised at specified voltages as described in test conditions for each device type.

EE8A Life Test (HTOL) Conditions:
Stress Duration: 168, 500, 1000 hours
Temperature: 125°C
Stress Voltage ispPAC-POWR: Vcc= 3.6V
Preconditioned: 100 program/erase cycles
Method: Lattice Document # 87-101943 and JESD22-A108C

Table 3.1.1 ispPAC-POWR Product Family HTOL Results

Product Name	Foundry	Lot #	Qty	24 Hrs Result	48 Hrs Result	168 Hrs Result	500 Hrs Result	1000 Hrs Result	Cumulative Hours
LA-ispPAC-POWR1014A	UMC	Lot #1	76			0	0	0	76,000
LA-ispPAC-POWR1014A	UMC	Lot #5	77			0	0	0	77,000
LA-ispPAC-POWR1014A	UMC	Lot #7	77			0			12,936
LA-ispPAC-POWR1014A	UMC	Lot #8	77			0	0	0	77,000
LA-ispPAC-POWR1014A	UMC	Lot #9	75			0	0	0	75,000
LA-ispPAC-POWR1014A	UMC	Lot #10	77			0	0	0	77,000
LA-ispPAC-POWR1014A	UMC	Lot #1	799	0					19,176
LA-ispPAC-POWR1014A	UMC	Lot #5	797	0					19,128
LA-ispPAC-POWR1014A	UMC	Lot #7	813	0					19,512
LA-ispPAC-POWR1014A	Epson	Lot #11	77				0		38,500
LA-ispPAC-POWR1014A	Epson	Lot #12	77				0		38,500
ispPAC-POWR1220AT8	Epson	Lot #1	77			0	0	0	77,000
ispPAC-POWR1220AT8	Epson	Lot #2	77			0	0	0	77,000
ispPAC-POWR1220AT8	Epson	Lot #3	77			0	0	0	77,000
ispPAC-POWR1220AT8	Epson	Lot #4	26			0	0	0	26,000
ispPAC-POWR1220AT8	Epson	Lot #5	26			0	0	0	26,000
ispPAC-POWR1220AT8	Epson	Lot #6	26			0	0	0	26,000
ispPAC-POWR1220AT8	Epson	Lot #7	26			0	0	0	26,000
ispPAC-POWR1220AT8	Epson	Lot #1	796		0				38,208
ispPAC-POWR1220AT8	Epson	Lot #2	800		0				38,400
ispPAC-POWR1220AT8	Epson	Lot #3	799		0				38,352

EE8A Cumulative Device Hours = 927,712
EE8A Cumulative Sample Size = 0 / 5,752

UMC EE8A Cumulative Device Hours = 452,752
UMC EE8A FIT Rate = 26 FIT (55C, 0.7ev, 60%UCL)
UMC EE8A ELFR Cumulative Results = 0 / 2,868

Epson EE8A Cumulative Device Hours = 526,960
Epson EE8A FIT Rate = 22 FIT (55C, 0.7ev, 60%UCL)
Epson EE8A ELFR Cumulative Results = 0 / 2,884

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3.2 ispPAC-POWR Product Family High Temperature Data Retention (HTRX)

High Temperature Data Retention (HTRX)

The High Temperature Data Retention test measures the Electrically Erasable cell (E2 cell) reliability while the High Temperature Operating Life test is structured to measure functional operating circuitry failure mechanisms. The High Temperature Data Retention test is specifically designed to accelerate charge gain on to or charge loss off of the floating gates in the device's array. Since the charge on these gates determines the actual pattern and function of the device, this test is a measure of the reliability of the device in retaining programmed information. In High Temperature Data Retention, the E2 cell reliability is determined by monitoring the cell margin after biased static operation at 150°C. All cells in all arrays are life tested in both programmed and erased states.

Data Retention (HTRX) Conditions:
Stress Duration: 168, 500, 1000 hours
Temperature: 150°C
Stress Voltage ispPAC-POWR: V_{CC}= 3.6V
Preconditioned with 100 program/erase cycles
Method: Lattice Document # 87-101925 and JESD22-A103C/JESD22-A117A

Table 3.2.1 ispPAC-POWR High Temperature Data Retention (HTRX) Results

Product Name	Foundry	Lot #	Qty	168 Hrs Result	500 Hrs Result	1000 Hrs Result	Cumulative Hours
LA-ispPAC-POWR1014A	UMC	Lot #1	77	0	0	0	77,000
LA-ispPAC-POWR1014A	UMC	Lot #2	77	0	0	0	77,000
LA-ispPAC-POWR1014A	UMC	Lot #3	77	0	0	0	77,000
LA-ispPAC-POWR1014A	Epson	Lot #11	78	0	0		39,000
LA-ispPAC-POWR1014A	Epson	Lot #13[A]	39		0		19,500
LA-ispPAC-POWR1014A	Epson	Lot #14[B]	39		0		19,500
ispPAC-POWR1220AT8	Epson	Lot #1	26	0	0	0	77,000
ispPAC-POWR1220AT8	Epson	Lot #2	77	0	0	0	77,000
ispPAC-POWR1220AT8	Epson	Lot #3	77	0	0	0	77,000
ispPAC-POWR1220AT8	Epson	Lot #8[A]	26	0	0	0	77,000
ispPAC-POWR1220AT8	Epson	Lot #9[B]	26	0	0	0	77,000

A) Lot #8 and #13 is a thin tunnel oxide process split.
B) Lot #9 and #14 is a thick tunnel oxide process split.

Cumulative HTRX Failure Rate = 0 / 618
Cumulative HTRX Device Hours = 540,000

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3.3 ispPAC-POWR Product Family Extended Endurance (EE)

Extended Endurance (EE)
Extended Endurance testing measures the durability of the device through programming and erase cycles. Extended Endurance testing consists of repeatedly programming and erasing all E2 cells in the array at 25°C to simulate programming cycles the user would perform. This test evaluates the integrity of the thin tunnel oxide through which current passes to program the floating gate in each cell of the array..

Extended Endurance (EE) Conditions:
Stress Duration: 1000 cycles
Temperature: 25°C
Stress Voltage ispPAC-POWR: V_{CC}= 3.6V
Method: Lattice Document # 70-104633 and JESD22-A117B

Table 3.3.1 ispPAC-POWR Extended Endurance (EE) Results

Product Name	Foundry	Lot #	Quantity	0 Cycles Result	1000 Cycles Result
ispPAC-POWR1220AT8	Epson	Lot #1	10	0	0
ispPAC-POWR1220AT8	Epson	Lot #2	10	0	0
ispPAC-POWR1220AT8	Epson	Lot #3	10	0	0
ispPAC-POWR1220AT8	Epson	Lot #8[A]	10	0	0
ispPAC-POWR1220AT8	Epson	Lot #9[B]	10	0	0
ispPAC-POWR1014A	Epson	Lot #11	10	0	0
ispPAC-POWR1014A	Epson	Lot #13[A]	5	0	0
ispPAC-POWR1014A	Epson	Lot #14[B]	5	0	0

A) Lot #8 and #13 is a thin tunnel oxide process split.
B) Lot #9 and #14 is a thick tunnel oxide process split.

Cumulative EE Failure Rate = 0 / 70

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3.4 ispPAC-POWR Product Family - ESD and Latch UP Data

Electrostatic Discharge-Human Body Model:

ispPAC-POWR product family was tested per the JESD22-A114E Electrostatic Discharge (ESD) Sensitivity Testing Human Body Model (HBM) procedure and Lattice Procedure # 70-100844.
All units were tested at 25^0C prior to reliability stress and after reliability stress. No failures were observed within the passing classification.

Table 3.4.1 ispPAC-POWR ESD-HBM Data

Product	Foundry	24-QFNS	32-QFNS	48-TQFP	100-TQFP
POWR1220AT8	UMC	N/A	N/A	N/A	>2000V Class 2
POWR1014A	UMC	N/A	N/A	>2000V Class 2	N/A
POWR1014	UMC	N/A	N/A	>2000V Class 2	N/A
POWR6AT6	UMC	N/A	>2000V Class 2	N/A	N/A
POWR607	UMC	N/A	>2000V Class 2	N/A	N/A
POWR605	UMC	>2000V Class 2	N/A	N/A	N/A

HBM classification for Commercial/Industrial products, per JESD22-A114E

Product	Foundry	24-QFNS	32-QFNS	48-TQFP	100-TQFP
POWR607	Epson	N/A	>2000V Class 2	N/A	N/A
POWR1014	Epson	N/A	N/A	>2000V Class 2	N/A
POWR1220AT8	Epson	N/A	N/A	N/A	>2000V Class 2

HBM classification for Commercial/Industrial products, per JESD22-A114E

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Electrostatic Discharge-Charged Device Model:

ispPAC-POWR product family was tested per the JESD22-C101D, Field-Induced Charged-Device Model Test Method for Electrostatic-Discharge-Withstand Thresholds of Microelectronic Components procedure and Lattice Procedure # 70-100844.

All units were tested at 250C prior to reliability stress and after reliability stress. No failures were observed within the passing Classification.

Table 3.4.2 ispPAC-POWR ESD-CDM Data

Product	Foundry	24-QFNS	32-QFNS	48-TQFP	100-TQFP
POWR1220AT8	UMC	N/A	N/A	N/A	>1000V Class IV
POWR1014A	UMC	N/A	N/A	>1000V Class IV	N/A
POWR1014	UMC	N/A	N/A	>1000V Class IV	N/A
POWR6AT6	UMC	N/A	>1000V Class IV	N/A	N/A
POWR607	UMC	N/A	>1000V Class IV	N/A	N/A
POWR605	UMC	>1000V Class IV	N/A	N/A	N/A

CDM classification for Commercial/Industrial products, per JESD22-C101D

Product	Foundry	24-QFNS	32-QFNS	48-TQFP	100-TQFP
POWR607	Epson	N/A	>1000V Class IV	N/A	N/A
POWR1014A	Epson	N/A	N/A	>1000V Class IV	N/A
POWR1220AT8	Epson	N/A	N/A	N/A	>1000V Class IV

CDM classification for Commercial/Industrial products, per JESD22-C101D

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Latch-Up:

ispPAC-POWR product family was tested per the JEDEC EIA/JESD78A IC Latch-up Test procedure and Lattice Procedure # 70-101570.

All units were tested at 25⁰C and +105⁰C prior to reliability stress and after reliability stress. No failures were observed within the passing classification.

Earlier latch-up testing at Lattice was hardware limited to room temperature testing. Additionally, maximum-rated ambient temperature latch-up testing is generally considered to be approximately 2X worse than the trigger values found at room temperature. In order to guard band our room temperature IO latch-up testing the standard was 4X, or +/- 400mA trigger current. Therefore, the previous Lattice I/O LU standard was >400mA at room temperature, while the present standard is >100mA at maximum-rated ambient temperature.

Table 3.4.3 ispPAC-POWR I/O Latch Up Data

Product	Foundry	24-QFNS	32-QFNS	48-TQFP	100-TQFP
POWR1220AT8	UMC	N/A	N/A	N/A	>+/- 400mA at room temp
POWR1014A	UMC	N/A	N/A	>+/- 100mA Class II, Level A	N/A
POWR1014	UMC	N/A	N/A	>+/- 100mA Class II, Level A	N/A
POWR6AT6	UMC	N/A	>+/- 400mA at room temp	N/A	N/A
POWR607	UMC	N/A	>+/- 400mA at room temp	N/A	N/A
POWR605	UMC	>+/- 400mA at room temp	N/A	N/A	N/A

Product	Foundry	24-QFNS	32-QFNS	48-TQFP	100-TQFP
POWR607	Epson		>+/- 100mA Class II, Level A		
POWR1014A	Epson			>+/- 100mA Class II, Level A	
POWR1220AT8	Epson	N/A	N/A	N/A	>+/- 100mA Class II, Level A

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4.0 PACKAGE QUALIFICATION DATA FOR ispPAC-POWR PRODUCT FAMILY

The ispPAC-POWR product family is offered in TQFP and QFNS packages. To cover the range of die in the largest package types for this product family, different package and die combinations were chosen as the generic qualification vehicles for all the package qualification tests including, Temperature Cycling (T/C), Un-biased HAST (UHAST)and Biased HAST (BHAST). Mechanical evaluation tests include Scanning Acoustic Tomography (SAT) and visual package inspection.

The generation and use of generic data is applied across a family of products or packages emanating from one base wafer foundry or assembly process is a Family Qualification, or Qualification By Extension. For the package stresses BHAST and UHAST, these are considered generic for a given Package Technology. T/C is considered generic up to an evaluated die size + package size + 10%, for a given Package Technology. Surface Mount Pre-Conditioning (SMPC) is considered generic up to an evaluated Peak Reflow temperature, for a given Package Technology. The following table demonstrates the package qualification matrix.

Table 4.1 ispPAC-POWR Product-Package Qualification-By-Extension Matrix

Product-Package Qualification Matrix		Unisem		ASEM / Amkor / Unisem	
Product	Stress Test	24-QFNS	32-QFNS	48-TQFP	100-TQFP
POWR1220AT8	SMPC	Package not offered		Package not offered	MSL3, 260C
	Temp Cycle				1000 cycles
	BHAST				96 hours
	UHAST				96 hours
	(5) HTSL				1000 hours
POWR1014A	SMPC	Package not offered		MSL3, 260C	Package not offered
	Temp Cycle			1000 cycles	
	BHAST			96 hours	
	UHAST			96 hours	
	(5) HTSL			1000 hours	
POWR1014	SMPC	Package not offered		(2) By Extension	Package not offered
	Temp Cycle			(2) By Extension	
	BHAST			(2) By Extension	
	UHAST			(2) By Extension	
	(5) HTSL			(2) By Extension	
POWR6AT6	SMPC	Package not offered	MSL1, 260C	Package not offered	
	Temp Cycle		1000 cycles		
	BHAST		(3) By Extension		
	UHAST		96 hours		
	HTSL		(3) By Extension		
POWR607	SMPC	Package not offered	(4) By Extension	Package not offered	
	Temp Cycle		(4) By Extension		
	BHAST		(3) By Extension		
	UHAST		(3) By Extension		
	HTSL		(3) By Extension		
POWR605	SMPC	(4) By Extension	Package not offered	Package not offered	
	Temp Cycle	(4) By Extension			
	BHAST	(3) By Extension			
	UHAST	(3) By Extension			
	HTSL	(3) By Extension			

Note: (1) By Extension from LA-Mach4000, 144-TQFP.
(2) By Extension from POWR1014A, 48TQFP.
(3) By Extension from GAL22V10D, 32QFNS.
(4) By Extension from POWR6AT6, 32-QFNS.
(5) Some HTSL data covered by extension from various HTOL data.

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4.1 ispPAC-POWR Product Family Surface Mount Preconditioning Testing

The Surface Mount Preconditioning (SMPC) Test is used to model the surface mount assembly conditions during component solder processing. All devices stressed through Temperature Cycling, Un-biased HAST and Biased HAST were preconditioned. This preconditioning is consistent with JEDEC JESD22-A113F "Preconditioning Procedures of Plastic Surface Mount Devices Prior to Reliability Testing", Moisture Sensitivity Level 3 (MSL3) package moisture sensitivity and dry-pack storage requirements.

Consistent with Lattice Semiconductor Corp. document # 25-100164, package reliability testing can be qualified by extension. Once a package outline is qualified within a package grouping as per doc #70-103639, all lower lead count (and smaller body size) packages within that package type and assembly technology are qualified by extension. Additionally, once an assembly technology has been qualified for one package type, that package type shall be qualified by extension to all future fabrication processes as long as those processes continue to use the same critical elements. Those critical elements in this case, are that the process-to-process interlayer dielectric material and thickness differences do not exceed the current production process limits for the qualification vehicle used. For 180nm and older technologies, the critical elements are considered equivalent.

Surface Mount Preconditioning (MSL3)
(10 Temperature Cycles between -55°C and 125°C, 24 hours bake @ 125°C, 30°C/60% RH, soak 192 hours, Reflow Simulation, 3 passes) performed before all EE9 package tests.
MSL3 Packages: TQFP

Surface Mount Preconditioning (MSL1)
(10 Temperature Cycles between -55°C and 125°C, 24 hr. bake @ 125°C, 85°C/85%RH soak, 168 hrs, 260C Reflow Simulation, 3 passes)
MSL1 Packages: QFNS
Method: Lattice Procedure # 70-103467, J-STD-020D.1 and JESD22-A113F

Table 4.1.1 Surface Mount Precondition Data

Product Name	Package	Assembly Site	Lot Number	Quantity	# of Fails	Reflow Temperature
LA-ispPAC-POWR1014A	48 TQFP	ASEM	Lot #1	81	0	260°C
LA-ispPAC-POWR1014A	48 TQFP	ASEM	Lot #2	81	0	260°C
LA-ispPAC-POWR1014A	48 TQFP	ASEM	Lot #3	81	0	260°C
LA-ispPAC-POWR1014A	48 TQFP	ASEM	Lot #4	156	0	260°C
LA-ispPAC-POWR1014A	48 TQFP	ASEM	Lot #5	156	0	260°C
LA-ispPAC-POWR1014A	48 TQFP	ASEM	Lot #6	156	0	260°C
LA-ispPAC-POWR1014A	48 TQFP	ASEM	Lot #11	77	0	260°C
LA-ispPAC-POWR1014A	48 TQFP	ASEM	Lot #12	77	0	260°C
ispPAC-POWR1208	44 TQFP	ASEM	Lot #1	45	0	260°C
ispPAC-POWR1208	44 TQFP	ASEM	Lot #2	45	0	260°C
ispPAC-POWR604	44 TQFP	ASEM	Lot #1	48	0	260°C
ispPAC-POWR604	44 TQFP	ASEM	Lot #2	48	0	260°C
GAL22V10D	32 QFNS	Unisem	Lot #1	154	0	260°C
GAL22V10D	32 QFNS	Unisem	Lot #2	154	0	260°C
GAL22V10D	32 QFNS	Unisem	Lot #3	154	0	260°C
POWR6AT6	32 QFNS	Unisem	Lot #4	77	0	260°C
POWR6AT6	32 QFNS	Unisem	Lot #5	77	0	260°C
ispPAC-POWR1208	44 TQFP	Unisem	Lot #1	77	0	260°C
ispPAC-POWR1208	44 TQFP	Unisem	Lot #1	77	0	260°C
ispPAC-POWR1208	44 TQFP	Unisem	Lot #1	77	0	260°C
ispMACH 4512	176TQFP	Unisem	Lot#1	99	0	260°C

Product Name	Package	Assembly Site	Lot Number	Quantity	# of Fails	Reflow Temperature
ispMACH 4512	176TQFP	Unisem	Lot#2	98	0	260°C
ispMACH 4512	176TQFP	Unisem	Lot#3	75	0	260°C
LA4128V	144 TQFP	ASEM	Lot #1	234	0	260°C
LA4128V	144 TQFP	ASEM	Lot #2	231	0	260°C
LA4128V	144 TQFP	ASEM	Lot #3	234	0	260°C
LA4128V	144 TQFP	Amkor	Lot #1	81	0	260°C
LA4128V	144 TQFP	Amkor	Lot #2	82	0	260°C
LA4128V	144 TQFP	Amkor	Lot #3	78	0	260°C
LA4128V	144 TQFP	Amkor	Lot #4	162	0	260°C
LA4128V	144 TQFP	Amkor	Lot #5	200	0	260°C
LA4128V	144 TQFP	Amkor	Lot #6	200	0	260°C
ispPAC-POWR1220AT8	100 TQFP	ASEM	Lot #1	314	0	260°C
ispPAC-POWR1220AT8	100 TQFP	ASEM	Lot #2	314	0	260°C
ispPAC-POWR1220AT8	100 TQFP	ASEM	Lot #3	314	0	260°C

Cumulative SMPC Failure Rate = 0 / 4,614

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4.2 ispPAC-POWR Product Family Temperature Cycling Data

The Temperature Cycling test is used to accelerate those failures resulting from mechanical stresses induced by differential thermal expansion of adjacent films, layers and metallurgical interfaces in the die and package. Devices are tested at 25°C after exposure to repeated cycling between -55°C and +125°C in an air environment consistent with JEDEC JESD22-A104C "Temperature Cycling", Condition B temperature cycling requirements. Prior to Temperature Cycling testing, all devices are subjected to Surface Mount Preconditioning.

MSL3 Packages: TQFP
MSL1 Packages: QFNS
Stress Duration: 1000 cycles
Stress Conditions: Temperature cycling between -55°C to 125°C
Method: Lattice Procedure # 70-101568 and JESD22-A104C

Table 4.2.1 Temperature Cycling Data

Product Name	Package	Assembly Site	Lot Number	Quantity	250 Cycles	500 Cycles	1000 Cycles
LA-ispPAC-POWR1014A	48 TQFP	ASEM	Lot #4	77	0	0	0
LA-ispPAC-POWR1014A	48 TQFP	ASEM	Lot #5	77	0	0	0
LA-ispPAC-POWR1014A	48 TQFP	ASEM	Lot #6	77	0	0	0
LA-ispPAC-POWR1014A	48 TQFP	ASEM	Lot #11	77		0	
LA-ispPAC-POWR1014A	48 TQFP	ASEM	Lot #12	76[B]		0	
ispPAC-POWR1208	44 TQFP	ASEM	Lot #1	42	0	0	0
ispPAC-POWR1208	44 TQFP	ASEM	Lot #2	45	0	0	0
ispPAC-POWR604	44 TQFP	ASEM	Lot #1	48	0	0	0
ispPAC-POWR604	44 TQFP	ASEM	Lot #2	48	0	0	0
POWR6AT6	32 QFNS	Unisem	Lot #4	77	0	0	0
POWR6AT6	32 QFNS	Unisem	Lot #5	77	0	0	0
ispPAC-POWR1208	44 TQFP	Unisem	Lot #1	77	0	0	0
ispPAC-POWR1208	44 TQFP	Unisem	Lot #1	77	0	0	0
ispPAC-POWR1208	44 TQFP	Unisem	Lot #1	77	0	0	0
ispMACH 4512	176TQFP	Unisem	Lot#1	50	0	0	0
ispMACH 4512	176TQFP	Unisem	Lot#2	49	0	0	0
ispMACH 4512	176TQFP	Unisem	Lot#3	45	0	0	0
LA4128V	144 TQFP	ASEM	Lot #1	77	0	0	0
LA4128V	144 TQFP	ASEM	Lot #2	77	0	0	0
LA4128V	144 TQFP	ASEM	Lot #3	77	0	0	0
LA4128V	144 TQFP	Amkor	Lot #1	81	0	0	0
LA4128V	144 TQFP	Amkor	Lot #2	82	0	0	0
LA4128V	144 TQFP	Amkor	Lot #3	78	0	0	0
ispPAC-POWR1220AT8	100 TQFP	ASEM	Lot #1	83			0
ispPAC-POWR1220AT8	100 TQFP	ASEM	Lot #2	83			0
ispPAC-POWR1220AT8	100 TQFP	ASEM	Lot #3	83			1[A]

A) 1 unit fails margin & checkerboard for adjacent bit failure. Not package stress related.
B) 1 unit lost by handler. Sample size reduced by one.

Cumulative Temp Cycle Failure Rate = 1 / 1,817

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4.3 Unbiased HAST Data

Unbiased Highly Accelerated Stress Test (HAST) testing uses both pressure and temperature to accelerate penetration of moisture into the package and to the die surface. The Unbiased HAST test is designed to detect ionic contaminants present within the package or on the die surface, which can cause chemical corrosion. Consistent JEDEC JESD22-A118, "Accelerated Moisture Resistance - Unbiased HAST," the Unbiased HAST conditions are 96 hour exposure at 130°C, 85% relative humidity, and 2 atmospheres of pressure. Prior to Unbiased HAST testing, all devices are subjected to Surface Mount Preconditioning.

MSL3 Packages: TQFP
MSL1 Packages: QFNS
Stress Duration: 96 Hrs
Stress Conditions: 130°C, 15psig, 85% RH
Method: Lattice Procedure # 70-104285 and JESD22-A118

Table 4.3.1 Unbiased HAST Data

Product Name	Package	Assembly Site	Lot Number	Quantity	# of Fails	Stress Duration
LA-ispPAC-POWR1014A	48 TQFP	ASEM	Lot #4	77	0	96 Hrs
LA-ispPAC-POWR1014A	48 TQFP	ASEM	Lot #5	77	0	96 Hrs
LA-ispPAC-POWR1014A	48 TQFP	ASEM	Lot #6	77	0	96 Hrs
GAL22V10D	32 QFNS	Unisem	Lot #1	77	0	96 Hrs
GAL22V10D	32 QFNS	Unisem	Lot #2	77	0	96 Hrs
GAL22V10D	32 QFNS	Unisem	Lot #3	77	0	96 Hrs
ispMACH 4512	176TQFP	Unisem	Lot#1	49	0	96 Hrs
ispMACH 4512	176TQFP	Unisem	Lot#2	49	0	96 Hrs
ispMACH 4512	176TQFP	Unisem	Lot#3	30	0	96 Hrs
LA4128V	144 TQFP	ASEM	Lot #1	77	0	96 Hrs
LA4128V	144 TQFP	ASEM	Lot #2	75	0	96 Hrs
LA4128V	144 TQFP	ASEM	Lot #3	77	0	96 Hrs
LA4128V	144 TQFP	Amkor	Lot #4	81	0	96 Hrs
LA4128V	144 TQFP	Amkor	Lot #5	100	0	96 Hrs
LA4128V	144 TQFP	Amkor	Lot #6	100	0	96 Hrs
ispPAC-POWR1220AT8	100 TQFP	ASEM	Lot #1	77	0	96 Hrs
ispPAC-POWR1220AT8	100 TQFP	ASEM	Lot #2	77	0	96 Hrs
ispPAC-POWR1220AT8	100 TQFP	ASEM	Lot #3	77	0	96 Hrs

Cumulative Unbiased HAST failure Rate = 0 / 1,331

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4.4 THB: Biased HAST Data

Highly Accelerated Stress Test (HAST) testing uses both pressure and temperature to accelerate penetration of moisture into the package and to the die surface. The Biased HAST test is used to accelerate threshold shifts in the MOS device associated with moisture diffusion into the gate oxide region as well as electrochemical corrosion mechanisms within the device package. Consistent with JEDEC JESD22-A110B "Highly-Accelerated Temperature and Humidity Stress Test (HAST)", the biased HAST conditions are with Vcc bias and alternate pin biasing in an ambient of 130°C, 85% relative humidity, and 2 atmospheres of pressure. Prior to Biased HAST testing, all devices are subjected to Surface Mount Preconditioning.

MSL3 Packages: TQFP
MSL1 Packages: QFNS
Stress Conditions: ispPAC-POWR **-** Vcc= 4.0 V, 130°C / 85% RH, 15 psig
Stress Conditions: GAL22V10D **-** Vcc= 5.0 V, 130°C / 85% RH, 15 psig
Stress Duration: 96 hours
Method: Lattice Procedure # 70-101571 and JESD22-A110B

Table 4.4.1 Biased HAST Data

Product Name	Package	Assembly Site	Lot Number	Quantity	# of Fails	Stress Duration
LA-ispPAC-POWR1014A	48 TQFP	ASEM	Lot #4	80	0	96 Hrs
LA-ispPAC-POWR1014A	48 TQFP	ASEM	Lot #5	80	0	96 Hrs
LA-ispPAC-POWR1014A	48 TQFP	ASEM	Lot #6	80	0	96 Hrs
GAL22V10D	32 QFNS	Unisem	Lot #1	77	0	96 Hrs
GAL22V10D	32 QFNS	Unisem	Lot #2	77	0	96 Hrs
GAL22V10D	32 QFNS	Unisem	Lot #3	77	0	96 Hrs
LA4128V	144 TQFP	ASEM	Lot #1	80	0	96 Hrs
LA4128V	144 TQFP	ASEM	Lot #2	77	0	96 Hrs
LA4128V	144 TQFP	ASEM	Lot #3	80	0	96 Hrs
LA4128V	144 TQFP	Amkor	Lot #4	81	0	96 Hrs
LA4128V	144 TQFP	Amkor	Lot #5	100	0	96 Hrs
LA4128V	144 TQFP	Amkor	Lot #6	100	0	96 Hrs
ispPAC-POWR1220AT8	100 TQFP	ASEM	Lot #1	77	0	96 Hrs
ispPAC-POWR1220AT8	100 TQFP	ASEM	Lot #2	77	0	96 Hrs
ispPAC-POWR1220AT8	100 TQFP	ASEM	Lot #3	77	0	96 Hrs

Cumulative BHAST failure Rate = 0 / 1,220

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4.5 HTSL: High Temperature Storage Life Data

High Temperature storage test is typically used to determine the effect of time and temperature, under storage conditions, for thermally activated failure mechanisms of solid state electronic devices. Units were stressed per JESD22-A103C, High Temperature Storage Life. Prior to Unbiased HAST testing, all Pb-free devices are subjected to Surface Mount Preconditioning.

The High Temperature Storage Life units were stressed at 150°C.

High Temperature Storage Life (HTSL) Conditions:
Stress Duration: 168, 500, 1000, hours.
Temperature: 150°C
Method: Lattice Document # 87-101925 and JESD22-A103C

Table 4.5.1 High Temperature Storage Life Results

Product Name	Assembler	Package	Lot #	Qty	168 Hrs Result	500 Hrs Result	1000 Hrs Result	Cumulative Hours
LA-ispPAC-POWR1014A	ASEM	100 TQFP	Lot #2	50	0	0	0	50000
LA-ispPAC-POWR1014A	ASEM	100 TQFP	Lot #4	77	0	0	0	77000
LA-ispPAC-POWR1014A	ASEM	100 TQFP	Lot #5	77	0	0	0	77000
LA-ispPAC-POWR1014A	ASEM	100 TQFP	Lot #8	77	0	0	0	77000
LA-ispPAC-POWR1014A	ASEM	100 TQFP	Lot #9	77	0	0	0	77000
LA-ispPAC-POWR1014A	ASEM	100 TQFP	Lot #10	77	0	0	0	77000
GAL22V10D	UNISEM	32 QFNS	Lot #1	77			0	77000
GAL22V10D	UNISEM	32 QFNS	Lot #2	77			0	77000
GAL22V10D	UNISEM	32 QFNS	Lot #3	77			0	77000
ispPAC-POWR1220AT8	ASEM	100 TQFP	Lot #1	77			0	77,000
ispPAC-POWR1220AT8	ASEM	100 TQFP	Lot #2	77			0	77,000
ispPAC-POWR1220AT8	ASEM	100 TQFP	Lot #3	77			0	77,000

Cumulative HTSL Failure Rate = 0 / 897
Cumulative HTSL Device Hours = 897,000

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5.0 ispPAC-POWR PROCESS RELIABILITY WAFER LEVEL REVIEW

The ispPAC-POWR product family is built on EE8A which is a 3.3V shallow trench isolated, 0.35um drawn / 0.25um Leff CMOS process with Electrically Erasable (E2) cells. This process uses three planarized metal interconnect layers and single layer polysilicon fabricated at either United Microelectronics Company (UMC), or Epson Sakata.

Several key fabrication process related parameters have been identified by the foundry that would affect the Reliability of the End-Product. These parameters are tested during the Development Phase of the Technology. Passing data (a 10yr lifetime at the reliability junction temperature) must be obtained for three lots minimum for each parameter before release to production. Normal operating conditions are defined in the Electrical Design Rules (EDR). These parameters are:

Hot Carrier Immunity (**HCI**): Effect is a reduction in transistor Idsat. Worst case is low temperature.
Time Dependent Dielectric Breakdown (**TDDB**): Transistor and capacitor oxide shorts or leakage.
Negative Bias Temperature Instability (**NBTI**): Symptom is a shift in Vth (also a reduction in Idsat).
Electromigration Lifetime (**EML**): Symptom is opens within, or shorts between, metal conductors.
Stress Migration (**SM**): Symptom is a void (open) in a metal Via due to microvoid coalescence. SM is not an issue for the EE8A BEOL (etched Al lines, W plug Vias, SiO IMD).

Table 5.1 UMC Foundry Wafer Level Reliability Results for EE8A (0.35um) Process Technology

HCI

Device	LVN	LVP
deltaIds	-10%	-10%
Celsius	25	25
Vgstress	Vd/2	0
Vds	3.6	-3.6
DC-HCI TTF >1yr	5 lots ≥ 32 yr	1 lot ≥ 1e6yr

TDDB

Device	LVN	MIM
Celsius	130	130
Vg	3.3	20
Area	8000um^2	2.25e4um^2
0.1% TTF	1.4e5yr	>1e6yr

EML

Layer	M1	M2	M3
Celsius	130	130	130
Delta R	+20%	+20%	+20%
Jmax	1.0mA/um	1.4mA/um	1.4mA/um
0.1% TTF	3 lots ≥ 11yr	3 lots ≥ 11yr	2 lots ≥ 16yr

Note: Reliability life times are based on listed temperature and use conditions. Detailed WLR test conditions are available upon request.

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Hot Carrier Immunity (**HCI**): Effect is a reduction in transistor Idsat. Worst case is low temperature.
Time Dependent Dielectric Breakdown (**TDDB**): Transistor and capacitor oxide shorts or leakage.
Negative Bias Temperature Instability (**NBTI**): Symptom is a shift in Vth (also a reduction in Idsat).
Electromigration Lifetime (**EML**): Symptom is opens within, or shorts between, metal conductors.
Stress Migration (**SM**): Symptom is a void (open) in a metal Via due to microvoid coalescence. SM is not an issue for the EE8A BEOL (etched Al lines, W plug Vias, SiO IMD).

Table 5.2 Epson Foundry Wafer Level Reliability Results for EE8A (0.35um) Process Technology

HCI

Device	LVN	LVP
deltaIds	-10%	-10%
Celsius	25	25
Vgstress	Vd/2	0
Vds	3.6	-3.6
DC-HCI TTF >1yr	3 lots ≥ 5.5yr	2 lots ≥ 8.2e3yr

TDDB

Device	LVN	MIM
Celsius	130	130
Vg	3.3	15
Area	8000um^2	2.25e4um^2
0.1% TTF	3 lots ≥ 2.8e3yr	3 lots ≥ 2.1e3yr

EML

Layer	M1	M2	M3
Celsius	130	130	130
Delta R	+20%	+20%	+20%
Jmax	1.0mA/um	1.4mA/um	1.4mA/um
0.1% TTF	3 lots ≥ 22.4yr	3 lots ≥ 30.5yr	3 lots ≥ 16.2yr

Note: Reliability life times are based on listed temperature and use conditions. Detailed WLR test conditions are available upon request.

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6.0 ispPAC-POWR PACKAGE ASSEMBLY INTEGRITY TESTS

6.1 Wire Bond Shear Test

This procedure is used to measure the wire bond strength at the ball joints. Thirty bonds from a minimum of five devices were used for Wire Bond Shear.

WIRE BOND SHEAR TEST RESULTS: All bond shear observations were > 20 grams for TQFP packages tested.

The average measured bond shear results for TQFP were Cpk of > 4.76 and Ppk of > 4.8.

6.2 Wire Bond Pull

This procedure is used to measure the wire bond strength at the ball joints and stitch bonds.
For products evaluation thirty bonds from a minimum of five devices were used for and Wire Bond Pull. Test conditions for these tests were 6 grams minimum for 1.0 mil gold wire

WIRE BOND PULL RESULTS: All bond pull observations were >4 grams for TQFP packages tested.

The average measured wire bond pull results for TQFP were Cpk of > 1.39.

6.3 Solderability

This procedure is used to evaluate the solderability of device terminals normally joined by a soldering operation. An accelerated aging test is included in this test method, which simulates natural aging under a combination of various storage conditions that have deleterious effects. Units are exposed to a 8 hour steam preconditioning followed a flux exposure for 7 seconds and a dip in Pb-free solder alloy @ 260 °C ± 5°C for 5 seconds. Minimum of 22 leads from 3 devices per lot were tested with zero failure acceptance.

No failures were observed for TQFP packages. All the tested units passed. There was less than 5% pitting and dewetting on the solder covered area.

No failures were observed for QFNS packages. All the tested units passed. There was less than 5% pitting and dewetting on the solder covered area.

6.4 Physical Dimensions

Devices were measured using the appropriate Lattice Semiconductor case outline drawings.

The 10 devices of TQFP from 3 different lots were measured with no failures found. The calculated Cpk on this small sample is Cpk > 2.0.

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7.0 ispPAC-POWR ADDITIONAL FAMILY DATA

Table 7.1 ispPAC-POWR Package Assembly Data- TQFP/QFNS

Package Attributes / Assembly Sites	**ASEM**	**Amkor**	**Unisem**
Die Family (Product Line)	ispPAC-POWR	ispPAC-POWR	ispPAC-POWR
Fabrication Process Technology	EE8A (0.35um CMOS)	EE8A (0.35um CMOS)	EE8A (0.35um CMOS)
Package Assembly Site	Malaysia	Korea	Indonesia
Package Type	TQFP	TQFP	TQFP / QFNS
Pin Count	48/100	48/100	48/100 24/32
Die Preparation/Singulation	wafer saw, full cut	wafer saw, full cut	wafer saw, full cut
Die Attach Material - TQFP	Ablebond 3230	Ablebond 3230	CRM1076NS
Die Attach Material - QFNS	N/A	N/A	CRM 1066 Series
Mold Compound Supplier/ID - TQFP	Hitachi CEL9220HF Series	KTMC 5700TQ Series	Sumitomo G700 Series
Mold Compound Supplier/ID - QFNS	N/A	N/A	Sumitomo G770 Series
Wire Bond Material	Gold (Au)	Gold (Au)	Gold (Au)
Wire Bond Methods	Thermosonic Ball	Thermosonic Ball	Thermosonic Ball
Lead frame Material	Cu Alloy	Cu Alloy	Cu Alloy
Lead Finish	Matte Sn (annealed)	Matte Sn (annealed)	Matte Sn (annealed)
Marking	Laser	Laser	Laser

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8.0 REVISION HISTORY

Table 8.1 Lattice ispPAC-POWR Product Family Qualification Summary revisions

Date	Revision	Section	Change Summary
August 2009	A	---	Initial document release.
January 2010	B	4.1 SMPC	Added Amkor QFNS MSL1 SMPC data.
November 2011	C	Qualification data sections 3, 4 & 5	Added Qualification data in support of PCN# 01A-12 in sections 3, 4 and 5: • In Section 3, see all data records for Product Name = ispPAC-POWR1220AT8 and Foundry = Epson • In Section 4, see all data records for Product Name = ispPAC-POWR1220AT8 and Assembly Site = ASEM • In Section 5, see all Wafer Level Reliability data in Table 5.2 = Epson Foundry
December 2011	D	Revision History	Added revision history as a standard section.
January 2012	E	Table 3.1	Updated ispPAC-POWR1220AT8 HTOL device hours
August 2012	F	Qualification data sections 3 & 4	Continuance Qualification data in support of PCN# 01A-12 in sections 3, 4
October 2012	G		Administrative change to internal document.
March 2013	H	Table 2.2	Update program/erase cycles typo and Customer letter.

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