ECP5 Product Family Qualification Summary

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Dear Customer,

Enclosed is Lattice Semiconductor's ECP5 FPGA Product Family Qualification Summary Report.

This report was created to assist you in the decision making process of selecting and using our products. The information contained in this report represents the entire qualification effort for this device family.

The information is drawn from an extensive qualification program of the wafer technology and packaging assembly processes used to manufacture our products. The program adheres to JEDEC Industry standards for qualification of the technology and device packaging. This program ensures you only receive product that meets the most demanding requirements for Quality and Reliability.

Your feedback is valuable to Lattice. If you have suggestions to improve this report, or the data included, we encourage you to contact your Lattice representative.

Sincerely,

James M. Orr
Vice President,
Corporate Quality
Lattice Semiconductor Corporation

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1.0 INTRODUCTION

The ECP5 family of FPGA devices is optimized to deliver high performance features such as an enhanced DSP architecture, high speed SERDES and high speed source synchronous interfaces in an economical FPGA fabric. This combination is achieved through advances in device architecture and the use of 40nm technology making the devices suitable for high-volume, high-speed, low-cost applications.

The ECP5 device family covers look-up-table (LUT) capacity to 84K logic elements and supports up to 365 user I/Os. The ECP5 device family also offers up to 156 18 x 18 multipliers and a wide range of parallel I/O standards.

The ECP5 FPGA fabric is optimized high performance with low power and low cost in mind. The ECP5 devices utilize reconfigurable SRAM logic technology and provide popular building blocks such as LUT-based logic, distributed and embedded memory, Phase Locked Loops (PLLs), Delay Locked Loops (DLLs), pre-engineered source synchronous I/O support, enhanced sysDSP slices and advanced configuration support, including encryption and dual-boot capabilities.

The pre-engineered source synchronous logic implemented in the ECP5 device family supports a broad range of interface standards, including DDR2/3, LPDDR2/3, XGMII and 7:1 LVDS.

The ECP5 device family also features high speed SERDES with dedicated PCS functions. High jitter tolerance and low transmit jitter allow the SERDES plus PCS blocks to be configured to support an array of popular data protocols including PCI Express, SMPTE, Ethernet (XAUI, GbE, and SGMII) and CPRI. Transmit De-emphasis with pre- and post-cursors, and Receive Equalization settings make the SERDES suitable for transmission and reception over various forms of media.

The ECP5 devices also provide flexible, reliable and secure configuration options, such as dual-boot capability, bitstream encryption, and TransFR field upgrade features.

The Lattice Diamond™ design software allows large complex designs to be efficiently implemented using the ECP5 FPGA family. Synthesis library support for ECP5 devices is available for popular logic synthesis tools. The Diamond tools use the synthesis tool output along with the constraints from its floor planning tools to place and route the design in the ECP5 device. The tools extract the timing from the routing and back-annotate it into the design for timing verification.

Lattice provides many pre-engineered IP (Intellectual Property) modules for the ECP5 family. By using these configurable soft core IPs as standardized blocks, designers are free to concentrate on the unique aspects of their design, increasing their productivity.

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Table 1.0.1 ECP5 Product Family Attributes

PRODUCT NAME	LFE5UM/5G-25	LFE5UM/5G-45	LFEUM/5G-85	LFE5U-25	LFE5U-45	LFE5U-85
LUTs (K)	24	44	84	24	44	84
Packages I/O						
0.5 mm Spacing I/O Count / SERDES						
285 csfBGA (10x10 mm)	118 / 2	118 / 2	118 / 2	118 / 0	118 / 0	118 / 0
0.8 mm Spacing I/O Count / SERDES						
381 caBGA (17x17 mm)	197 / 2	203 / 4	205 / 4	197 / 0	203 / 0	205 / 0
554 caBGA (23x23 mm)		245 / 4	259 / 4		245 / 0	259 / 0
756 caBGA (27x27 mm)			365 / 4			365 / 0

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2.0 LATTICE PRODUCT QUALIFICATION PROGRAM

Lattice Semiconductor Corp. maintains a comprehensive reliability qualification program to assure that each product achieves its reliability goals. After initial qualification, the continued high reliability of Lattice products is assured through ongoing monitor programs as described in Lattice Semiconductor's Reliability Monitor Program Procedure (Doc. #70-101667). All product qualification plans are generated in conformance with Lattice Semiconductor's Qualification Procedure (Doc. #70-100164) with failure analysis performed in conformance with Lattice Semiconductor's Failure Analysis Procedure (Doc. #70-100166). Both documents are referenced in Lattice Semiconductor's Quality Assurance Manual, which can be obtained upon request from a Lattice Semiconductor sales office. Figure 2.1 shows the Product Qualification Process Flow.

If failures occur during qualification, an 8D process is used to find root cause and eliminate the failure mode from the design, materials, or process. The effectiveness of any fix or change is validated through additional testing as required. Final testing results are reported in the qualification reports.

Failure rates in this reliability report are expressed in FITs. Due to the very low failure rate of integrated circuits, it is convenient to refer to failures in a population during a period of 10^9 device hours; one failure in 10^9 device hours is defined as one FIT.

Product families are qualified based upon the requirements outlined in Table 2.0.2. In general, Lattice Semiconductor follows the current Joint Electron Device Engineering Council (JEDEC) and Military Standard testing methods. Lattice automotive products are qualified and characterized to the Automotive Electronics Council (AEC) testing requirements and methods. Product family qualification will include products with a wide range of circuit densities, package types, and package lead counts. Major changes to products, processes, or vendors require additional qualification before implementation.

The ECP5 family is the fourth generation FPGA product family and first United Microelectronics Corporation (UMC) 40nm (LP40-9M) SRAM only technology based product offering. The Lattice Semiconductor ECP5 FPGA product family qualification efforts are based on the first ECP5 devices in the family per the Lattice Semiconductor Qualification Procedure, doc#70-100164.

Lattice Semiconductor maintains a regular reliability monitor program. The current Lattice Reliability Monitor Report can be found at Product Reliability Monitor Report.

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Figure 2.0.1 Lattice Standard Product Qualification Process Flow

This diagram represents the standard qualification flow used by Lattice to qualify new Product Families. The target end market for the Product Family determines which flow options are used. The ECP5 Product Family was qualified using the Commercial / Industrial Qualification Option.

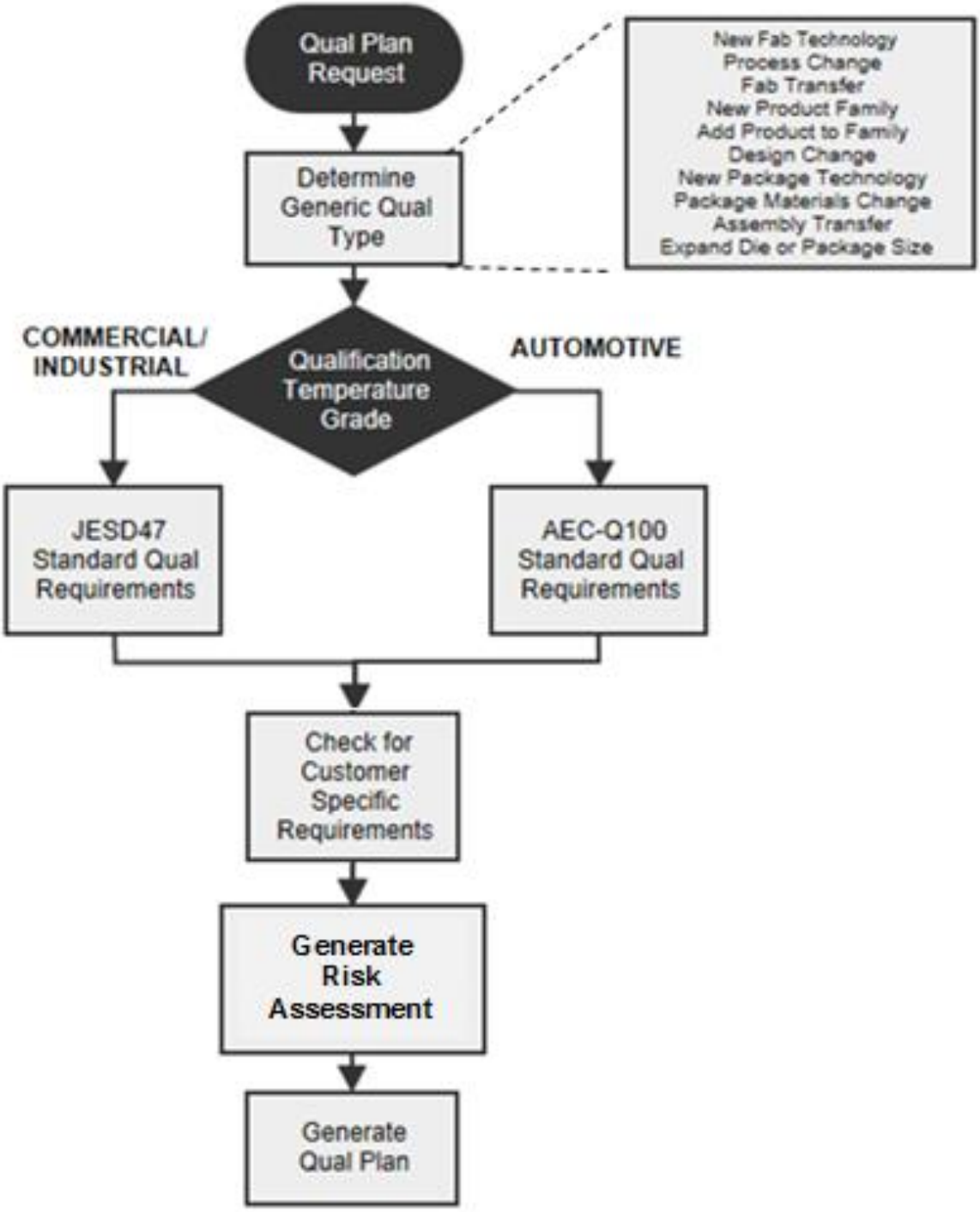

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Figure 2.0.1 Lattice Standard Product Qualification Process Flow (cont.)

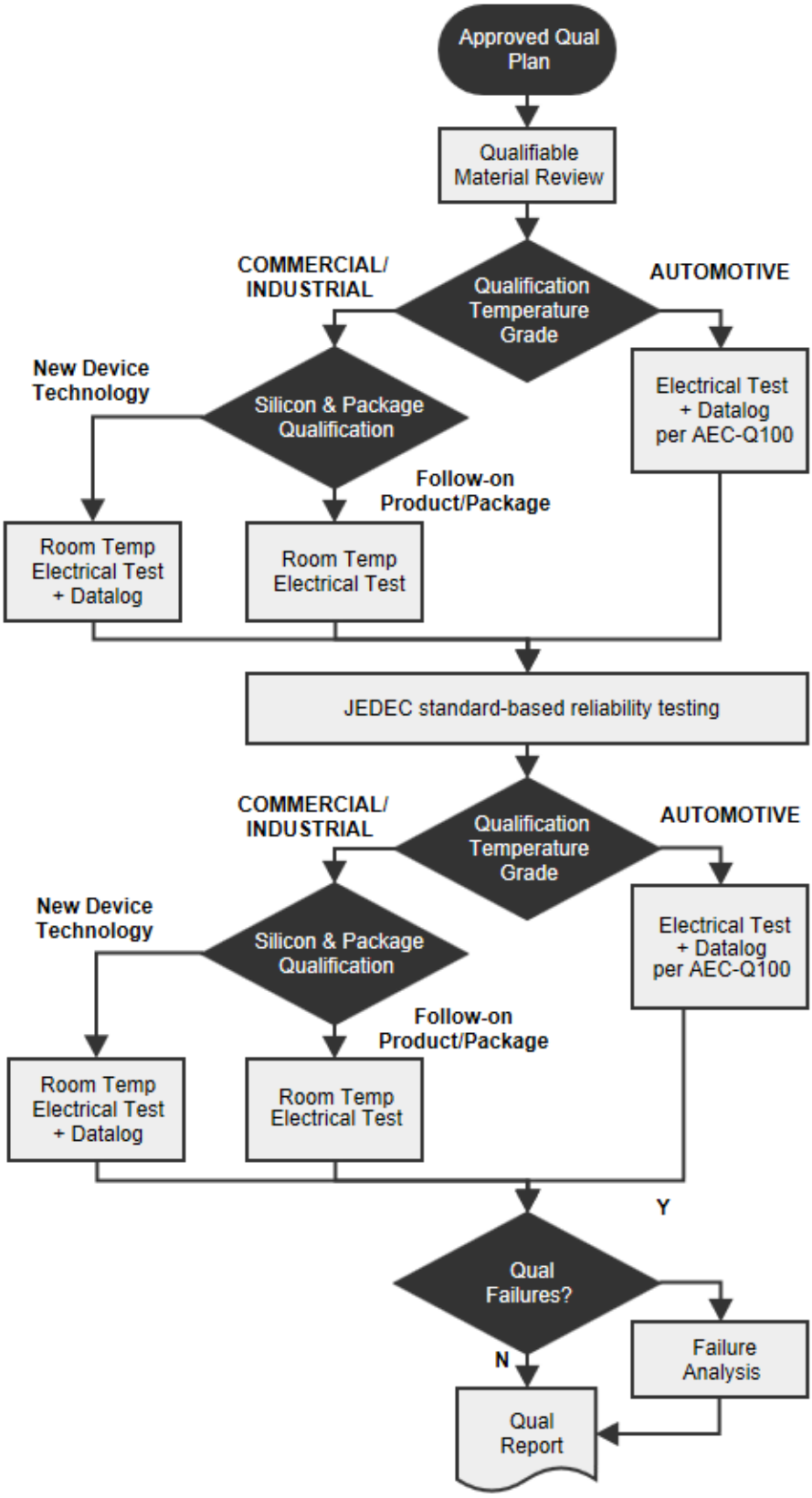

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Table 2.0.2 Standard Qualification Testing

TEST	STANDARD	TEST CONDITIONS
High Temperature Operating Life (HTOL)	JESD22-A108	≥125°C Tj and max operating supplies
Electrostatic Discharge - Human Body Model (HBM)	JS-001	25°C (Technology/Device dependent Performance Targets)
Electrostatic Discharge - Charged Device Model (CDM)	JESD22-C101	25°C (Technology/Device dependent Performance Targets)
Latch-Up (LU)	JESD78	Class II, +/-100mA trigger current and AMR operating supplies
Accelerated Soft Error Testing (ASER)	JESD89	25°C, Nominal operating supplies
Surface Mount Pre-conditioning (SMPC)	IPC/JEDEC J-STD-020	Per appropriate MSL level per J-STD-020
High Temp Storage Life (HTSL)	JESD22-A103	Condition B
Temperature Cycling (TC)	JESD22-A104	Condition B, soak mode 2 (typical)
Temperature Humidity Bias, THB (85/85) or	JESD22-A101	85°C, 85% RH, max operating supplies or
Biased Highly Acclerated Stress Test (HAST)	JESD22-A110	110°C, 85% RH, max operating supplies or
		130°C, 85% RH, max operating supplies
Unbiased Highly Acclerated Stress Test (uHAST)	JESD22-A118	110°C, 85% RH or 130°C, 85% RH

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3.0 QUALIFICATION DATA FOR ECP5 PRODUCT FAMILY

The ECP5 family is the fourth generation FPGA product family and first nine-layer metal 40nm SRAM only Technology based product offering. The ECP5 product family is used as the primary technology qualification vehicle.

Product Family: ECP5
Packages offered: csfBGA and caBGA
Process Technology Node: 40nm

3.1 ECP5 Product Family Life Data

The High Temperature Operating Life (HTOL) test is used to thermally accelerate those wear out and failure mechanisms that would occur as a result of operating the device continuously in a system application. Consistent with JESD22-A108D "Temperature, Bias, and Operating Life", a pattern specifically designed to exercise the maximum amount of circuitry is programmed into the device and this pattern is continuously exercised at specified voltages as described in test conditions for each device type.

The Early Life Failure Rate (ELFR) test uses large samples sizes for a short duration (48hrs ≤ t ≤ 168 hrs) HTOL stress to determine the infant mortality rate of a device family.

ECP5 Life Test (HTOL) Conditions:

Stress Duration: 168, 500, 1000 hours

Stress Conditions: ECP5 (LFE5) max operating supplies, $T_{JUNCTION}$ = 125°C

Method: JESD22-A108D

Table 3.1.1 ECP5 Product Family Life Results

Product Name	Package	Lot #	Qty	168 Hrs Result	500 Hrs Result	1000 Hrs Result	Cumulative Hours
LFE5UM-25	381 caBGA	Lot #1	106	0	0	0	106,000
LFE5UM-45	381 caBGA	Lot #1	71	0	0	0	71,000
LFE5UM-45	381 caBGA	Lot #2	43*	0	0	0	43,000
LFE5UM-85	381 caBGA	Lot #1a	24	0	0	0	24,000
LFE5UM-85	381 caBGA	Lot #1b	23	0	0	0	23,000
LFE5UM-85	381 caBGA	Lot #1c	24	0	0	0	24,000
LFE5UM-85	381 caBGA	Lot #2	106	0	0	0	106,000

* Units damaged by handling. Units removed from sample size.

ECP5 Cumulative Life Testing Device Hours = 397,000
ECP5 Cumulative Result / Sample Size = 0 / 397
ECP5 FIT Rate = 30 FIT
FIT Assumptions: CL=60%, AE=0.7eV, Tjref=55C

ECP5 ELFR (168 Hrs) Cumulative Result / Sample Size = 0 / 397
ECP5 HTOL (500 Hrs) Cumulative Result / Sample Size = 0 / 397
ECP5 HTOL (1000 Hrs) Cumulative Result / Sample Size = 0 / 397
Test Chip Cumulative Sample Size = 0 / 397

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3.2 ECP5 Product Family – ESD and Latch Up Data

Electrostatic Discharge-Human Body Model

The ECP5 product family was tested per JS-001-2014 Electrostatic Discharge (ESD) Sensitivity Testing Human Body Model (HBM) procedure.

All units were tested at room ambient prior to reliability stress and after reliability stress. No failures were observed within the passing classification.

Table 3.2.1 ECP5 ESD-HBM Data

Product Type	285 csfBGA	381 caBGA	554 caBGA	756 caBGA
LFE5UM-25	QBS	>1000V Class 1C	Packages not offered	Package not offered
LFE5UM-45	QBS	QBS	>1000V Class 1C	Package not offered
LFEUM-85	QBS	QBS	>1000V Class 1C	QBS
LFE5UM5G-25	QBS	QBS	Packages not offered	Package not offered
LFE5UM5G-45	QBS	QBS	QBS	Package not offered
LFEUM5G-85	QBS	QBS	QBS	QBS
LFE5U-25	QBS	QBS	Packages not offered	Package not offered
LFE5U-45	QBS	QBS	QBS	Package not offered
LFE5U-85	QBS	QBS	QBS	QBS

HBM classification for Commercial/Industrial products, per JS-001-2014.
All HBM levels indicated are dual-polarity (±).
HBM worst-case performance is the package with the smallest RLC parasitics. All other packages for a given product are qualified-by-similarity (QBS).

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Electrostatic Discharge-Charged Device Model

The ECP5 product family was tested per the JS-002-2014, Field-Induced Charged-Device Model Test Method for Electrostatic-Discharge-Withstand Thresholds of Microelectronic Components procedure.
All units were tested at room ambient prior to reliability stress and after reliability stress. No failures were observed within the passing classification.

Table 3.2.2 ECP5 ESD-CDM Data

Product Type	285 csfBGA	381 caBGA	554 caBGA	756 caBGA
LFE5UM-25	QBS	>500V Class C2a	Package not offered	Package not offered
LFE5UM-45	QBS	QBS	>500V Class C2a	Package not offered
LFEUM-85	QBS	QBS	QBS	>250V (SerDes pins) Class C1 >500V (all other pins) Class C2a
LFE5UM5G-25	QBS	QBS	Package not offered	Package not offered
LFE5UM5G-45	QBS	QBS	QBS	Package not offered
LFEUM5G-85	QBS	QBS	QBS	QBS to LFEUM-85
LFE5U-25	QBS	QBS	Package not offered	Package not offered
LFE5U-45	QBS	QBS	QBS	Package not offered
LFE5U-85	QBS	QBS	QBS	>500V Class C2a

CDM classification for Commercial/Industrial products, per JS-002-2014.
All CDM levels indicated are dual-polarity (±).
CDM worst-case performance is the package with the largest bulk capacitance. All other packages for a given product are qualified-by-similarity (QBS).

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Latch-Up

The ECP5 product family was tested per the JESD78D IC Latch-up Test procedure.

All units were tested at room ambient prior to reliability stress and after reliability stress. No failures were observed within the passing classification.

Table 3.2.3 ECP5 Latch-up I-Test Data

Product Type	285 csfBGA	381 caBGA	554 caBGA	756 caBGA
LFE5UM-25	QBS	>100mA @ 105°C Class II	Package not offered	Package not offered
LFE5UM-45	QBS	QBS	>100mA @ 105°C Class II	Package not offered
LFEUM-85	QBS	QBS	>100mA @ 105°C Class II	QBS
LFE5UM5G-25	QBS	QBS	Package not offered	Package not offered
LFE5UM5G-45	QBS	QBS	QBS	Package not offered
LFEUM5G-85	QBS	QBS	QBS	QBS
LFE5U-25	QBS	QBS	Package not offered	Package not offered
LFE5U-45	QBS	QBS	QBS	Package not offered
LFE5U-85	QBS	QBS	QBS	QBS

I-Test classification for Commercial/Industrial products, per JESD78D.
All I-Test levels indicated are dual-polarity (±).
I-Test worst-case performance is the package with access to the most IOs. All other packages for a given product are qualified-by-similarity (QBS).

Table 3.2.4 ECP5 Vsupply Over-voltage Test Data

Product Type	285 csfBGA	381 caBGA	554 caBGA	756 caBGA
LFE5UM-25	QBS	AMR operating supply @ 105°C Class II	Package not offered	Package not offered
LFE5UM-45	QBS	QBS	AMR operating supply @ 105°C Class II	Package not offered
LFEUM-85	QBS	QBS	AMR operating supply @ 105°C Class II	QBS
LFE5UM5G-25	QBS	QBS	Package not offered	Package not offered
LFE5UM5G-45	QBS	QBS	QBS	Package not offered
LFEUM5G-85	QBS	QBS	QBS	QBS
LFE5U-25	QBS	QBS	Package not offered	Package not offered
LFE5U-45	QBS	QBS	QBS	Package not offered
LFE5U-85	QBS	QBS	QBS	QBS

Vsupply Over-voltage Test classification for Commercial/Industrial products, per JESD78D.
Vsupply Over-voltage Test worst-case performance is the package with access to the most individual power rails. All other packages for a given product are qualified-by-similarity (QBS).

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4.0 PACKAGE QUALIFICATION DATA FOR ECP5 PRODUCT FAMILY

The ECP5 product family is offered in csfBGA and caBGA packages. This report details the package qualification results of the initial ECP5 product introductions. Package qualification tests include Temperature Cycling (TC), Unbiased HAST (UHAST), Biased HAST (HAST) and High Temperature Storage (HTSL). Mechanical evaluation tests include Scanning Acoustic Tomography (SAT) and visual package inspection.

The generation and use of generic data is applied across a family of products or packages emanating from one base wafer foundry or assembly process is a Family Qualification, or Qualification-by-Similarity. For the package stresses HAST, UHAST and HTSL, these are considered generic for a given Package Technology. Surface Mount Pre-Conditioning (SMPC) is considered generic up to an evaluated Peak Reflow temperature, for a given Package Technology. The following table demonstrates the package qualification matrix.

Table 4.0.1 Product-Package Qualification-By-Similarity Matrix

<table>
<tr><th rowspan="2">Products</th><th rowspan="2">Stress Test</th><th>Advanced Semiconductor Engineering, Taiwan (ASET)</th><th colspan="3">Advanced Semiconductor Engineering, Malaysia (ASEM)</th></tr>
<tr><th>285 csfBGA</th><th>381 caBGA</th><th>554 caBGA</th><th>756 caBGA</th></tr>
<tr><td rowspan="5">LFE5UM-25</td><td>SMPC</td><td>MSL3 260°C</td><td>MSL3 260°C</td><td rowspan="5">Package not offered</td><td rowspan="5">Package not offered</td></tr>
<tr><td>TC</td><td>700 cycles</td><td>700 cycles</td></tr>
<tr><td>HAST</td><td>264 hours</td><td>QBS</td></tr>
<tr><td>UHAST</td><td>264 hours</td><td>QBS</td></tr>
<tr><td>HTSL</td><td>1000 hours</td><td>QBS</td></tr>
<tr><td rowspan="5">LFE5UM-45</td><td>SMPC</td><td>MSL3 260°C</td><td>MSL3 260°C</td><td>MSL3 260°C</td><td rowspan="5">Package not offered</td></tr>
<tr><td>TC</td><td>700 cycles</td><td>700 cycles</td><td>700 cycles</td></tr>
<tr><td>HAST</td><td>264 hours</td><td>264 hours</td><td>QBS</td></tr>
<tr><td>UHAST</td><td>264 hours</td><td>264 hours</td><td>QBS</td></tr>
<tr><td>HTSL</td><td>1000 hours</td><td>1000 hours</td><td>QBS</td></tr>
<tr><td rowspan="5">LFE5UM-85</td><td>SMPC</td><td rowspan="5">Q1’18</td><td>MSL3 260°C</td><td rowspan="5">QBS</td><td>MSL3 260°C</td></tr>
<tr><td>TC</td><td>700 cycles</td><td>700 cycles</td></tr>
<tr><td>HAST</td><td>QBS</td><td>264 hours</td></tr>
<tr><td>UHAST</td><td>QBS</td><td>264 hours</td></tr>
<tr><td>HTSL</td><td>QBS</td><td>1000 hours</td></tr>
<tr><td rowspan="5">LFE5UM5G-25</td><td>SMPC</td><td rowspan="5">QBS</td><td rowspan="5">QBS</td><td rowspan="5">Package not offered</td><td rowspan="5">Package not offered</td></tr>
<tr><td>TC</td></tr>
<tr><td>HAST</td></tr>
<tr><td>UHAST</td></tr>
<tr><td>HTSL</td></tr>
<tr><td rowspan="5">LFE5UM5G-45</td><td>SMPC</td><td rowspan="5">QBS</td><td rowspan="5">QBS</td><td rowspan="5">QBS</td><td rowspan="5">Package not offered</td></tr>
<tr><td>TC</td></tr>
<tr><td>HAST</td></tr>
<tr><td>UHAST</td></tr>
<tr><td>HTSL</td></tr>
<tr><td rowspan="5">LFE5UM5G-85</td><td>SMPC</td><td rowspan="5">Q1’18</td><td rowspan="5">QBS</td><td rowspan="5">QBS</td><td rowspan="5">QBS</td></tr>
<tr><td>TC</td></tr>
<tr><td>HAST</td></tr>
<tr><td>UHAST</td></tr>
<tr><td>HTSL</td></tr>
</table>

Products	Stress Test	Advanced Semiconductor Engineering, Taiwan (ASET)	Advanced Semiconductor Engineering, Malaysia (ASEM)		
		285 csfBGA	381 caBGA	554 caBGA	756 caBGA
LFE5U-25	SMPC	QBS	QBS	Package not offered	Package not offered
	TC				
	HAST				
	UHAST				
	HTSL				
LFE5U-45	SMPC	QBS	QBS	QBS	Package not offered
	TC				
	HAST				
	UHAST				
	HTSL				
LFE5U-85	SMPC	Q1’18	QBS	QBS	QBS
	TC				
	HAST				
	UHAST				
	HTSL				

4.1 Surface Mount Preconditioning Testing

The Surface Mount Preconditioning (SMPC) Test is used to model the surface mount assembly conditions during component solder processing. All devices stressed through Temperature Cycling, Unbiased HAST and Biased HAST were preconditioned. This preconditioning is consistent with JESD22-A113F "Preconditioning Procedures of Plastic Surface Mount Devices Prior to Reliability Testing", Moisture Sensitivity Level 3 (MSL3) package moisture sensitivity and dry-pack storage requirements.

Surface Mount Preconditioning (MSL3)

(5 Temperature Cycles Condition B, 24 hours bake @ 125°C, 30°C/60% RH, soak 192 hours, 260 °C Reflow Simulation, 3 passes) performed before all package tests.

MSL3 Packages: csfBGA, caBGA

Method: J-STD-020D.1 and JESD22-A113F

Table 4.1.1 Surface Mount Precondition Data

Product Name	Package	Assembly Site	Lot Number	Moisture Soak Level	3X Reflow Temperature	Quantity	# of Fails
LFE5UM-25	381 caBGA	ASEM	Lot #1	MSL3	260°C	360	0
LFE5UM-45	381 caBGA	ASEM	Lot #1	MSL3	260°C	329	2[A]
LFE5UM-45	381 caBGA	ASEM	Lot #2	MSL3	260°C	329	0
LFE5UM-45	381 caBGA	ASEM	Lot #3	MSL3	260°C	329	2[A]
LFE5UM-45	381 caBGA	ASEM	Lot #4	MSL3	260°C	330	0
LFE5UM-45	381 caBGA	ASEM	Lot #5	MSL3	260°C	330	0
LFE5UM-45	381 caBGA	ASEM	Lot #6	MSL3	260°C	330	0
LFE5UM-85	381 caBGA	ASEM	Lot #1	MSL3	260°C	30	0
LFE5UM-85	381 caBGA	ASEM	Lot #2	MSL3	260°C	30	0
LFE5UM-85	381 caBGA	ASEM	Lot #3	MSL3	260°C	30	0
LFE5UM-85	381 caBGA	ASEM	Lot #4	MSL3	260°C	350	3[A]
LFE5UM-45	554 caBGA	ASEM	Lot #1	MSL3	260°C	84	0
LFE5UM-45	554 caBGA	ASEM	Lot #2	MSL3	260°C	85	0
LFE5UM-45	554 caBGA	ASEM	Lot #3	MSL3	260°C	85	1[A]
LFE5UM-45	554 caBGA	ASEM	Lot #4	MSL3	260°C	350	0
LFE5UM-85	756 caBGA	ASEM	Lot #1	MSL3	260°C	117	0
LFE5UM-85	756 caBGA	ASEM	Lot #2	MSL3	260°C	110	0
LFE5UM-85	756 caBGA	ASEM	Lot #3	MSL3	260°C	110	0
LFE5UM-25	285 csfBGA	ASEM	Lot #1	MSL3	260°C	320	0
LFE5UM-25	285 csfBGA	ASEM	Lot #2	MSL3	260°C	320	0
LFE5UM-25	285 csfBGA	ASEM	Lot #3	MSL3	260°C	320	0
LFE5UM-45	285 csfBGA	ASEM	Lot #1	MSL3	260°C	330	0
LFE5UM-45	285 csfBGA	ASEM	Lot #2	MSL3	260°C	330	0
LFE5UM-45	285 csfBGA	ASEM	Lot #3	MSL3	260°C	330	0

A = FAR #1521: Open contact fails due to lifted ball bonds. Chlorine contamination found on affected pad. CA/PA in place.

Cumulative SMPC Failure Rate ECP5 = 8/5,668

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4.2 Temperature Cycling Data

The Temperature Cycling test is used to accelerate those failures resulting from mechanical stresses induced by differential thermal expansion of adjacent films, layers and metallurgical interfaces in the die and package. Devices are tested at 25°C after exposure to repeated cycling between -55°C and +125°C in an air environment consistent with JESD22-A104D “Temperature Cycling”, Condition B temperature cycling requirements. Prior to Temperature Cycling testing, all devices are subjected to Surface Mount Preconditioning.

MSL3 Packages: csfBGA, caBGA

Stress Duration: 700 cycles

Stress Conditions: Temperature cycling between -55°C to 125°C

Method: JESD22-A104D Condition B

Table 4.2.1 Temperature Cycling Data

Product Name	Package	Assembly Site	Lot Number	Stress Temperature	Stress Duration	Quantity	# of Fails
LFE5UM-25	381 caBGA	ASEM	Lot #1	-55°C to 125°C	700 cycles	350	1[A]
LFE5UM-45	381 caBGA	ASEM	Lot #1	-55°C to 125°C	700 cycles	80	0
LFE5UM-45	381 caBGA	ASEM	Lot #2	-55°C to 125°C	700 cycles	79	0
LFE5UM-45	381 caBGA	ASEM	Lot #3	-55°C to 125°C	700 cycles	80	0
LFE5UM-85	381 caBGA	ASEM	Lot #1	-55°C to 125°C	700 cycles	30	0
LFE5UM-85	381 caBGA	ASEM	Lot #2	-55°C to 125°C	700 cycles	30	0
LFE5UM-85	381 caBGA	ASEM	Lot #3	-55°C to 125°C	700 cycles	30	0
LFE5UM-85	381 caBGA	ASEM	Lot #3	-55°C to 125°C	700 cycles	347	1[A]
LFE5UM-45	554 caBGA	ASEM	Lot #1	-55°C to 125°C	700 cycles	80	0
LFE5UM-45	554 caBGA	ASEM	Lot #2	-55°C to 125°C	700 cycles	80	0
LFE5UM-45	554 caBGA	ASEM	Lot #3	-55°C to 125°C	700 cycles	80	0
LFE5UM-85	756 caBGA	ASEM	Lot #1	-55°C to 125°C	700 cycles	30	0
LFE5UM-85	756 caBGA	ASEM	Lot #2	-55°C to 125°C	700 cycles	30	0
LFE5UM-85	756 caBGA	ASEM	Lot #3	-55°C to 125°C	700 cycles	30	0
LFE5UM-25	285 csfBGA	ASEM	Lot #1	-55°C to 125°C	700 cycles	80	0
LFE5UM-25	285 csfBGA	ASEM	Lot #2	-55°C to 125°C	700 cycles	80	0
LFE5UM-25	285 csfBGA	ASEM	Lot #3	-55°C to 125°C	700 cycles	80	0
LFE5UM-45	285 csfBGA	ASEM	Lot #1	-55°C to 125°C	700 cycles	90	0
LFE5UM-45	285 csfBGA	ASEM	Lot #2	-55°C to 125°C	700 cycles	90	0
LFE5UM-45	285 csfBGA	ASEM	Lot #3	-55°C to 125°C	700 cycles	90	0

A = FAR #1521: Open contact fails due to lifted ball bonds. Chlorine contamination found on affected pad. CA/PA in place.

Cumulative Temp Cycle Failure Rate ECP5 = 2 / 1,866

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4.3 Unbiased HAST Data

Unbiased Highly Accelerated Stress Test (UHAST) testing uses both pressure and temperature to accelerate penetration of moisture into the package and to the die surface. The Unbiased HAST test is designed to detect ionic contaminants present within the package or on the die surface, which can cause chemical corrosion. Consistent with JESD22-A118A, "Accelerated Moisture Resistance - Unbiased HAST," the Unbiased HAST condition is 264 hours exposure at 110°C and 85% relative humidity. Prior to Unbiased HAST testing, all devices are subjected to Surface Mount Preconditioning.

MSL3 Packages: csfBGA, caBGA
Stress Duration: 264 Hours
Stress Conditions: 110°C/85% RH
Method: JESD22-A118 A

Table 4.3.1 Unbiased HAST Data

Product Name	Package	Assembly Site	Lot Number	Stress Temperature	Stress Duration	Quantity	# of Fails
LFE5UM-45	381 caBGA	ASEM	Lot #1	110°C	264 hours	80	0
LFE5UM-45	381 caBGA	ASEM	Lot #2	110°C	264 hours	80	0
LFE5UM-45	381 caBGA	ASEM	Lot #3	110°C	264 hours	80	0
LFE5UM-85	756 caBGA	ASEM	Lot #1	110°C	264 hours	30	0
LFE5UM-85	756 caBGA	ASEM	Lot #2	110°C	264 hours	25	0
LFE5UM-85	756 caBGA	ASEM	Lot #3	110°C	264 hours	25	0
LFE5UM-25	285 csfBGA	ASEM	Lot #1	110°C	264 hours	80	0
LFE5UM-25	285 csfBGA	ASEM	Lot #2	110°C	264 hours	80	0
LFE5UM-25	285 csfBGA	ASEM	Lot #3	110°C	264 hours	80	0
LFE5UM-45	285 csfBGA	ASEM	Lot #1	110°C	264 hours	80	0
LFE5UM-45	285 csfBGA	ASEM	Lot #2	110°C	264 hours	80	0
LFE5UM-45	285 csfBGA	ASEM	Lot #3	110°C	264 hours	80	0

Cumulative Unbiased HAST failure Rate ECP5 = 0 / 800

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4.4 THB: Biased HAST Data

Biased Highly Accelerated Stress Test (HAST) testing uses both pressure and temperature to accelerate penetration of moisture into the package and to the die surface. The Biased HAST test is used to accelerate threshold shifts in the MOS device associated with moisture diffusion into the gate oxide region as well as electrochemical corrosion mechanisms within the device package. Consistent with JESD22-A110D "Highly-Accelerated Temperature and Humidity Stress Test (HAST)", the biased HAST conditions are with supply rails biased and alternate pin biasing in an ambient of 110°C, 85% relative humidity, and 2 atmospheres of pressure. Prior to Biased HAST testing, all devices are subjected to Surface Mount Preconditioning.

MSL3 Packages: csfBGA, caBGA
Stress Conditions: Maximum Operating Supplies and 110°C / 85% RH, 15 psig
Stress Duration: 264 hours
Method: JESD22-A110D

Table 4.4.1 Biased HAST Data

Product Name	Package	Assembly Site	Lot Number	Stress Temperature	Stress Duration	Quantity	# of Fails
LFE5UM-45	381 caBGA	ASEM	Lot #1	110°C	264 hours	84	0
LFE5UM-45	381 caBGA	ASEM	Lot #2	110°C	264 hours	84	0
LFE5UM-45	381 caBGA	ASEM	Lot #3	110°C	264 hours	84	0
LFE5UM-85	756 caBGA	ASEM	Lot #1	110°C	264 hours	27	0
LFE5UM-85	756 caBGA	ASEM	Lot #2	110°C	264 hours	25	0
LFE5UM-85	756 caBGA	ASEM	Lot #3	110°C	264 hours	24*	0
LFE5UM-25	285 csfBGA	ASEM	Lot #1	110°C	264 hours	77	0
LFE5UM-25	285 csfBGA	ASEM	Lot #2	110°C	264 hours	77	0
LFE5UM-25	285 csfBGA	ASEM	Lot #3	110°C	264 hours	77	0
LFE5UM-45	285 csfBGA	ASEM	Lot #1	110°C	264 hours	77	0
LFE5UM-45	285 csfBGA	ASEM	Lot #2	110°C	264 hours	77	0
LFE5UM-45	285 csfBGA	ASEM	Lot #3	110°C	264 hours	77	0

* Unit damaged by handling. Unit removed from sample size.

Cumulative HAST failure Rate ECP5 = 0 / 766

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4.5 High Temperature Storage Life (HTSL)

The High Temperature Storage Life test is used to determine the effect of time and temperature, under storage conditions, for thermally activated failure mechanisms. Consistent with JESD22-A103D, the devices are subjected to high temperature storage Condition B: +150 (-0/+10) °C for 1000 hours. Prior to High Temperature Storage, all ECP5 devices are subjected to Surface Mount Preconditioning as mentioned in Table 4.1.1. This is a relatively new requirement consistent with JESD47F for Pb-free, wirebonded packages.

MSL3 Packages: csfBGA, caBGA
Stress Duration: 168, 500, 1000 hours
Temperature: 150°C (ambient)
Method: JESD22-A103D

Table 4.5.1 ECP5 High Temperature Storage Life Results

Product Name	Package	Assembly Site	Lot Number	Stress Temperature	Stress Duration	Quantity	# of Fails
LFE5UM-45	381 caBGA	ASEM	Lot #1	150°C	1000 hours	80	0
LFE5UM-45	381 caBGA	ASEM	Lot #2	150°C	1000 hours	80	0
LFE5UM-45	381 caBGA	ASEM	Lot #3	150°C	1000 hours	80	1[A]
LFE5UM-85	756 caBGA	ASEM	Lot #1	150°C	1000 hours	30	0
LFE5UM-85	756 caBGA	ASEM	Lot #2	150°C	1000 hours	30	0
LFE5UM-85	756 caBGA	ASEM	Lot #3	150°C	1000 hours	30	1[A]
LFE5UM-25	285 csfBGA	ASEM	Lot #1	150°C	1000 hours	80	0
LFE5UM-25	285 csfBGA	ASEM	Lot #2	150°C	1000 hours	80	0
LFE5UM-25	285 csfBGA	ASEM	Lot #3	150°C	1000 hours	80	0
LFE5UM-45	285 csfBGA	ASEM	Lot #1	150°C	1000 hours	80	0
LFE5UM-45	285 csfBGA	ASEM	Lot #2	150°C	1000 hours	80	0
LFE5UM-45	285 csfBGA	ASEM	Lot #3	150°C	1000 hours	80	0

A = FAR #1521: Open contact fails due to lifted ball bonds. Chlorine contamination found on affected pad. CA/PA in place.

ECP5 Cumulative HTSL Failure Rate = 2 / 810

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5.0 ECP5 PRODUCT FAMILY SEU AND SEL

Soft Error Rate testing is conducted to characterize the sensitivity of SRAM storage and device logic elements to high energy neutron and alpha particle radiation. Charge induced by the impact of these particles can collect at sensitive nodes in the device, and result in changes in the internal electrical states of the device. While these changes do not cause immediate damage to the device, they can cause a logical error in device operation.

Lattice Semiconductor characterizes neutron sensitivity by testing at the LANSCE Facility at Los Alamos National Laboratories or at the TRIUMF facility in Vancouver, British Columbia, Canada. The neutron beams at these facilities closely match the energy distribution of neutrons occurring due to cosmic ray collisions in the atmosphere. Neutron testing conforms to JESD89 requirements.

Alpha particles originate in the packaging materials used to surround the silicon circuit. Impurities in the mold compound and in interconnect materials emit alpha particles as part of radioactive decay. The range of penetration of alpha particles in silicon is limited. Only alpha particles generated in the package materials and interconnect can reach the die surface and cause upsets.

Lattice Semiconductor characterizes alpha particle sensitivity using calibrated sources. Americium-241 is used to model the decay products of Po-210 and Pb-210 in the lead solder die-package interconnects. Thorium-232 is used to model the decay products of Th-232, Th-228, Ra-226, U-238, etc. from impurities in the packaging materials. Alpha particle testing is done at the Lattice factory and conforms to JESD89.

Soft Error Tests:

Neutron SRAM SER Rate – This characteristic is the rate of upset of Configuration RAM and Embedded Block RAM cells during neutron testing. Devices are configured with a logic pattern, exposed to measured neutron doses, and the device configuration was read back from the device. Changed bits are identified through pattern comparison. Neutron testing is normalized to the published neutron flux rate for New York City (NYC) at sea level. This rate is measured as Failures in Time (FITs) normalized per million bits in the device to allow for translation across the device families densities.

Neutron SRAM SEL Rate – This test looks for evidence of latch up due to soft error upsets. The test is conducted at maximum VCC and temperature conditions. Devices are configured with a logic pattern, exposed to measured neutron doses, and the device configuration was read back from the device. Voltage and current is monitored. Devices are check for functional recovery after exposure. This consists of verification that the devices reconfigure correctly with or without a power cycle. It is considered a failure if the part cannot recover. Neutron testing is normalized to the published neutron flux rate for New York City at sea level. This rate is measured as Failures in Time (FITs) normalized per million bits in the device to allow for translation across the device families densities.

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Alpha SRAM SER Rate – This characteristic is the rate of upset of Configuration RAM and Embedded Block RAM (EBR) cells during alpha particle testing. Devices are configured with a logic pattern, exposed for a fixed time period to a calibrated alpha particle source, and the device configuration was read back from the device. Changed bits are identified through pattern comparison. Alpha particle testing is normalized to a background rate of 0.001alpha/cm2-hr based on characterization of packaging materials. This rate is measured at Failures in Time (FITs) normalized per million bits in the device to allow for translation across the device families densities as Failures in Time (FITs) normalized per million bits in the device to allow for translation across the device families densities.

Environmental Consideration:

The neutron failure rate observed in the field is affected by the shape and strength of the Magnetosphere. It is affected by the operating altitude. It is affected by any material intervening between the part and the atmosphere. Lattice Semiconductor uses the NYC standard (14 N/cm^2*hrs) to normalize the data. Customers will need to adjust the numbers if the use conditions are significantly different than NYC.

Device utilization also has a measurable impact on the observed failure rate. A SEU event in an unused circuit is very unlikely to disturb operation. Lattice Semiconductor assumed 100% utilization to calculate the FIT rate and MTBFF data in the following tables. The FIT rate experienced by the customer will be less due to the reduced utilization of the device resources.

For devices that support SED and applications that use the SED (Soft Error Detect) circuits, there is no de-rating because all the SRAM cells are scanned whether they are utilized or not in the customer application.

Neutron Testing:

The parts were tested at the TRIUMF facility in Vancouver, BC, Canada. A neutron particle beam was used to accelerate the Soft Error failure rate due to neutron collisions in the semiconductor devices. The neutron beam at TRIUMF correlates to the energy distribution found around the globe. Both static and dynamic patterns were used to generate the SEU (Soft Error Upset) rate and test for SEL (Soft Error Latch-up).

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Neutron SEL Test Conditions:

Device: LFE5UM-85

Stress Duration: Thirty-eight test samples at 3 minutes duration each. (3 minutes is equivalent to 1,170 years of exposure vs. the NYC standard of 14 N/cm^2*hr.)

Temperature: >85°C

Voltage: 1.26 volts (max operating voltage)

Method: JESD89

Table 5.0.1 ECP5 SEL Data

Product	Permanent functional failure observed?	Voltage excursions observed (>20%)	Failure to reprogram	Power cycles required to recover operation	Average number of configuration SEU events
LFE5UM-85	None	None	None	None	88

Calculated FIT rate with 60% confidence = 0.2 FITs

Neutron SEU Test Conditions:

Device: LFE5UM-85

Stress Duration: Forty-two test samples at 3 minutes average duration each. (3 minutes is equivalent to 1,170 years of exposure vs. the NYC standard of 14 N/cm^2*hr.)

Temperature: Ambient

Voltage: 1.20 volts (nominal operating voltage)

Method: JESD89

Table 5.0.2 ECP5 Neutron SEU Data

Product	Configuration FITs/Mb	EBR FITs/Mb	Average number of configuration SEU events	Average number of EBR SEU events
LFE5UM-85	156	not measured	78	not measured
StDev	29			

Table 5.0.3 ECP5 Neutron MTBFF Data

Device	Configuration	EBR	Configuration	EBR	1 Part
	Usable bit count	Usable bit count	FITs	FITs	MTBFF (in years)
LFE5UM-85	15,101,984	3,744K	406	0	281
LFE5UM-45	8,011,620	1,944K	216	0	530
LFE5UM-25	4,476,704	1,008K	120	0	948

The MTBFF numbers assume EBR is mitigated by ECC.
The FIT and MTBFF data assumes 100% utilization.
The functional upset derating assumes 6/1.

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Alpha Testing:

The parts were tested at Lattice Semiconductor. Several alpha radiation sources were used to accelerate the soft error failure rate due to alpha particles from the package material used in the semiconductor devices. The radiation sources correlate to the known sources of alpha particles in package materials. Both static and dynamic patterns were used to generate the SEU (Soft Error Upset) rate.

Neutron SEU Test Conditions:

Device: LFE5UM-85
Stress Duration: Fourteen test samples at twenty minutes average duration each. (equivalent years of exposure depends on the package material)
Temperature: Ambient
Voltage: 1.20 volts (nominal operating voltage)
Method: JESD89

Table 5.0.4 ECP5 Alpha SEU Data

Product	Wire Bond Packages (WBP) Ultra low mold material (0.001 Alpha/hr)		Flip Chip Underfill and SnAgCu (0.0004 Alpha/hr)		Average number of configuration SEU events	Average number of EBR SEU events
	Configuration (FITs/Mb)	EBR (FITs/Mb)	Configuration (FITs/Mb)	EBR (FITs/Mb)		
LFE5UM-85	32	not measured	13	not measured	36	not measured
StDev	14		6			

Table 5.0.5 ECP5 Alpha MTBFF Data

Device	Configuration	EBR	Wire Bond Packages (WBP)			Flip Chip		
			Configuration	EBR	1 Part	Configuration	EBR	1 Part
	Usable bit count	Usable bit count	FITs	FITs	MTBFF (in years)	FITs	FITs	MTBFF (in years)
LFE5UM-85	15,101,984	3,744K	74	0	1,541	30	0	3,851
LFE5UM-45	8,011,620	1,944K	39	0	2,904	16	0	7,260
LFE5UM-25	4,476,704	1,008K	22	0	5,197	9	0	12,992

The MTBFF numbers assume EBR is mitigated by ECC.
The FIT and MTBFF data assumes 100% utilization.
The functional upset derating assumes 6/1.

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6.0 ADDITIONAL PACKAGE FAMILY DATA

Table 6.0.1 ECP5 Package Assembly Data

Package Attributes / Assembly Sites	**ASEM**			
Fabrication Process Technology	UMC 40nm CMOS (LP40-9M)			
Package Assembly Site	Malaysia			
Package Type	caBGA			
Ball Counts	381/554/756			
Material Description		**LBGA/MBGA**		
Package Body (mm)		17x17	23x23	27x27
Wafer	Thickness (mil)	8.0 +/- 0.5		
Die Attach	Epoxy Vendor	Henkel		
	Epoxy Type	Ablebond 2100A		
	Epoxy Specifc Formation	Silver		
Wire Bond	Wire Vendor	Nippon Micrometal		
	Wire Diameter	Lattice Spec 84-106034		
	Wire Type	Pd Coated Cu Wire		
	Wire Impurity	0.8-2.7%		
Mold	Compound Vendor	Sumitomo		
	Compound Type	EMEG750SE		
	Mold Thickness (mm)	0.8		
	Compound Specific Formation	RoHS & Ultra Low Alpha		
Top Marking (option		Laser Mark		
Solder Ball Mount	Solder Ball Vendor	Senju		
	Solder Ball Size (mm)	0.4		
	Solder Ball Composition	SAC305		
Flux	Flux Vendor	Cooksoon Electronics		
	Flux Type	Alphametals WS9180-M7		
	Flux Part Number	2160000096		
Package Attributes / Assembly Sites	**ASET**			
Fabrication Process Technology	UMC 40nm CMOS (LP40-9M)			
Package Assembly Site	Taiwan			
Package Type	csfBGA			
Ball Counts	285			
Material Description		**FCCSP**		
Package Body (mm)		10x10		
Wafer	**Thicknes (mil)**	14		
	Diameter (mm)	300mm		
Bump/Cu Pillar	**Pitch (um)**	63		
	Total Height (um)	60		
	Composition	Sn 98.2/Ag 1.8		
Underfill	**Composition**	UA-26		
Mold Compound	**Composition**	EME-G760 Type SW		
Substrate	**Technology**	1-2-1 HDI		
	Finish	OSP		
Solder Ball	**Composition**	LF35		
	Diameter (mm)	0.3		
	Pitch (mm)	0.5		

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7.0 REVISION HISTORY

Table 7.0.1 ECP5 Product Family Qualification Summary Revisions

Date	Revision	Change Summary
April 2015	A	New release using LFE5UM-45 and LFE5UM-85 qualification data.
July 2015	B	Update LFE5UM-45 and LFE5UM-85 Q2 data.
September 2015	C	Update LFE5UM-45 and LFE5UM-85 Q2 data; add 25H and 85H data.
August 2016	D	Correct typo in Table 3.1.1 to reflect correct process name.
November 2017	E	Update LFE5UM5G QBS data and 285csfBGA package qualification data.

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