Sensors in Smartphones

Sensors are changing the landscape of today’s smartphones. According to IMS Research, “Sensors are poised to enable the next stage of mobile handset evolution. Various sensor types now show the potential to alter user input methods, user interfaces, and to enable new genres of use cases for mobile handsets.” Sensors not only enhance the user interface to smartphones but are also used to monitor environmental conditions such as battery life, temperature, and ambient light. In fact, today’s high-end smartphones can contain anywhere from 10 to 20 different sensors.

Processor Bottleneck

Most sensors available on the market today use I2C and/or SPI as the interface to the processors, with I2C being the primary choice. However, many mobile processors lack true I2C or SPI master controllers. They heavily rely on GPIO to emulate I2C/SPI communication for sensor connectivity. This creates two problems:

- Unable to meet performance requirements
- GPIO shortage

Lattice Bridging Solutions

There are several ways to facilitate sensor expansion in the handset:

- Bridges from a processor external bus to offer additional I2C master controllers (see Figure 3)
- Bridges from a processor external bus to offer additional SPI master controllers (see Figure 4)
- Bridges from a processor SPI port to offer additional I2C master controllers
- Bridges from a processor UART for either I2C or SPI master controllers

All of these methods can be implemented using an iCE40™ ultra low density FPGA as a bridge chip for a mobile processor. Because the iCE40 FPGA uses a flexible, programmable fabric, it is ideally suited to interfaces with different processors and can be customized to support additional functions as required. Furthermore, the hardware can be customized to support the software implementation optimizing development time. Figure 2 illustrates the possible interfaces that can be used to communicate with a mobile processor.
Qualcomm EBI2 to I²C Masters
Lattice has created a reference example that implements an EBI2 to Triple I²C Master Controller in an iCE40 FPGA. It supports the following features:

- EBI2 asynchronous interface with access time of <50ns
- Three I²C compliant masters support 100KHz (standard mode) and 400KHz (fast mode)
- Independent I²C master operation
- I²C master clock stretching and repeated start operation
- I²C master FIFOs (256 bytes deep)
- Interrupt-driven or polling software interfaces
- Implemented in a 4x4 mm ucBGA package
- Standby current as low as 40µA

Qualcomm EBI2 to SPI Master
Lattice has created a reference example that implements an EBI2 to SPI master controller in an iCE40 FPGA. It supports the following features:

- Supports Full Duplex mode
- Programming operating mode (CPOL and CPHA)
- Programmable timing and SCLK frequency
- Programmable LSB/MSB first modes of data transfer
- Read and write FIFOs, each of 256x16-bit size
- Four independent slave selects
- Supports interrupt driven or polling software interfaces
- Up to 100MHz system clock and 35MHz SPI clock frequency on –T speed grade

Sensor Expansion – Bridging Demo Board
The Bridging Demo Board from Lattice demonstrates the capabilities of:

- Freescale mini-Flexbus to dual I²C masters/dual SPI master controllers
- Touch key pad
- Accelerometer
- Battery Gauge (I²C only)

- Supports on-board Flash and flex cable (external) Flash configuration

The Bridging Demo Board is available only through Lattice sales representatives. Contact your local Lattice sales representative for more information and to schedule a demo.