

## ORCA<sup>®</sup> OR3LxxxB Series Field-Programmable Gate Arrays

### Features

- High-performance, cost-effective, 0.25  $\mu\text{m}$  5-level metal technology.
- 2.5 V internal supply voltage and 3.3 V I/O supply voltage for speed and compatibility.
- Up to 340,000 usable gates in 0.25  $\mu\text{m}$ .
- Up to 612 user I/Os in 0.25  $\mu\text{m}$ . (OR3LxxxB I/Os are 5 V tolerant to allow interconnection to both 3.3 V and 5 V devices, selectable on a per-pin basis, when using 3.3 V I/O supply.)
- Twin-quad programmable function unit (PFU) architecture with eight 16-bit look-up tables (LUTs) per PFU, organized in two nibbles for use in nibble- or byte-wide functions. Allows for mixed arithmetic and logic functions in a single PFU.
- Nine user registers per PFU, one following each LUT, plus one extra. All have programmable clock enable and local set/reset, plus a global set/reset (GSRN) that can be disabled per PFU.
- Flexible Input Structure (FINS) of the PFUs provides a routability enhancement for LUTs with shared inputs and the logic flexibility of LUTs with independent inputs.
- Fast-carry logic and routing to adjacent PFUs for nibble-wide, byte-wide, or longer arithmetic functions, with the option to register the PFU carry-out.
- Softwired LUTs (SWL) allow fast cascading of up to three levels of LUT logic in a single PFU.
- Supplemental logic and interconnect cell (SLIC) provides 3-statable buffers, up to 10-bit decoder, and PAL\*-like AND-OR-INVERT (AOI) in each programmable logic cell (PLC).
- Abundant hierarchical routing resources based on routing two data nibbles and two control lines per set provide for faster place and route implementations and less routing delay.
- Individually programmable drive capability: 12 mA sink/6 mA source or 6 mA sink/3 mA source.
- Built-in boundary scan (*IEEE*<sup>†</sup>1149.1 JTAG) and TS\_ALL testability function to 3-state all I/O pins.
- Enhanced system clock routing for low-skew, high-speed clocks originating on-chip or at any I/O.
- Up to four ExpressCLK inputs allow extremely fast clocking of signals on- and off-chip plus access to internal general clock routing.
- StopCLK feature to glitchlessly stop/start the ExpressCLKs independently by user command. Programmable I/O (PIO) has:
  - Fast-capture input latch and input flip-flop (FF)/latch for reduced input setup time and zero hold time.
  - Capability to (de)multiplex I/O signals.
  - Fast access to SLIC for decodes and PAL-like functions.
  - Output FF and two-signal function generator to reduce CLK to output propagation delay.
- Fast open-drain drive capability.
- New programmable I/O 3-state FF allows 3-state buffer control signals to be set up a clock cycle early for improved clock to output delays

\* PAL is a trademark of Advanced Micro Devices, Inc.

† *IEEE* is a registered trademark of The Institute of Electrical and Electronics Engineers, Inc.

Table 1. ORCA OR3LxxxB Series FPGAs

Device	System Gates <sup>‡</sup>	LUTs	Registers	Max User RAM	User I/Os	Array Size	Process Technology
OR3L165B	120K—244K	8192	10752	131K	516	32 x 32	0.25 $\mu\text{m}$ /5 LM
OR3L225B	166K—340K	11552	14820	185K	612	38 x 38	0.25 $\mu\text{m}$ /5 LM

<sup>‡</sup> The usable gate counts range from a logic-only gate count to a gate count assuming 30% of the PFUs/SLICs being used as RAMs. The logic-only gate count includes each PFU/SLIC (counted as 108 gates/PFU), including 12 gates per LUT/FF pair (eight per PFU), and 12 gates per SLIC/FF pair (one per PFU). Each of the four PIOs per PIC is counted as 16 gates (three FFs, fast-capture latch, output logic, CLK, and I/O buffers). PFUs used as RAM are counted at four gates per bit, with each PFU capable of implementing a 32 x 4 RAM (or 512 gates) per PFU.

## System-Level Features

System-level features reduce glue logic requirements and make a system on a chip possible. These features in the ORCA OR3LxxxB include:

- Full PCI Local Bus compliance for all devices in 3.3 V and 5 V PCI systems. Pin-selectable I/O clamping diodes provide 3.3 V and 5 V compliance and 5 V tolerance.
- Dual-use microprocessor interface (MPI) can be used for configuration, readback, device control, and device status, as well as for a general-purpose interface to the FPGA. Glueless interface to *i960*\* and *PowerPC*† processors with user-configurable address space provided.
- Parallel readback of configuration data capability with the built-in microprocessor interface.

- Programmable clock manager (PCM) adjusts clock phase and duty cycle for input clock rates from 5 MHz to 120 MHz. The PCM may be combined with FPGA logic to create complex functions, such as digital phase-locked loops (DPLL), frequency counters, and frequency synthesizers or clock doublers. Two PCMs are provided per device.
- True internal 3-state, bidirectional buses with simple control provided by the SLIC.
- 32 x 4 RAM per PFU, configurable as single- or dual-port. Create large, fast RAM/ROM blocks (128 x 8 in only eight PFUs) using the SLIC decoders as bank drivers.
- Full UTOPIA Level III I/O compliance (5.0 ns CLK -> OUT, 2.0 ns setup with 0 ns hold).

\* *i960* is a registered trademark of Intel Corporation.

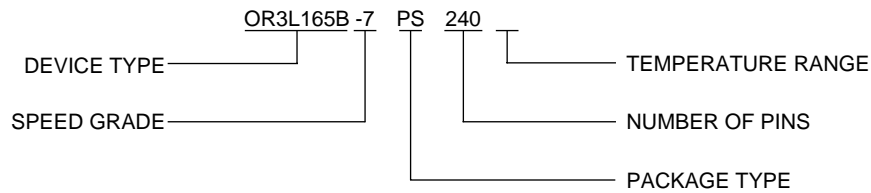
† *PowerPC* is a registered trademark of International Business Machines, Inc.

**Table 2. ORCA Series 3L System Performance**

Parameter	# PFUs	-7	-8	Unit
16-bit Loadable Up/Down Counter	2	151	176	MHz
16-bit Accumulator	2	151	176	MHz
8 x 8 Parallel Multiplier:				
Multiplier Mode, Unpipelined <sup>1</sup>	11.5	38	46	MHz
ROM Mode, Unpipelined <sup>2</sup>	8	93	116	MHz
Multiplier Mode, Pipelined <sup>3</sup>	15	129	152	MHz
32 x 16 RAM (synchronous):				
Single-port, 3-state Bus <sup>4</sup>	4	173	209	MHz
Dual-port <sup>5</sup>	4	231	277	MHz
128 x 8 RAM (synchronous):				
Single-port, 3-state Bus <sup>4</sup>	8	151	181	MHz
Dual-port <sup>5</sup>	8	151	181	MHz
8-bit Address Decode (internal):				
Using Softwired LUTs	0.25	2.30	2.00	ns
Using SLICs <sup>6</sup>	0	1.29	1.12	ns
32-bit Address Decode (internal):				
Using Softwired LUTs	2	7.97	6.84	ns
Using SLICs <sup>7</sup>	0	3.75	3.16	ns
36-bit Parity Check (internal)	2	7.97	6.84	ns

1. Implemented using 8 x 1 multiplier mode (unpipelined), register-to-register, two 8-bit inputs, one 16-bit output.
2. Implemented using two 32 x 12 ROMs and one 12-bit adder, one 8-bit input, one fixed operand, one 16-bit output.
3. Implemented using 8 x 1 multiplier mode (fully pipelined), two 8-bit inputs, one 16-bit output (seven of 15 PFUs contain only pipelining registers).
4. Implemented using 32 x 4 RAM mode with read data on 3-state buffer to bidirectional read/write bus.
5. Implemented using 32 x 4 dual-port RAM mode.
6. Implemented in one partially occupied SLIC with decoded output set up to CE in same PLC.
7. Implemented in five partially occupied SLICs.

## Ordering Information



OR3L165B, -7 Speed Grade, 240-pin Power Quad Shrink Flat Package (SQFP2), Commercial Temperature

**Table 3. Voltage Options**

Device	Voltage
OR3LxxxB	2.5 V internal/3.3 V I/O

**Table 4. Temperature Options**

Symbol	Description	Temperature
(Blank)	Commercial	0 °C to 70 °C
I	Industrial	-40 °C to +85 °C

**Table 5. Package Options**

Symbol	Description
BA	Plastic Ball Grid Array (PBGA)
BC	Enhanced Ball Grid Array (EBGA)
BM	Plastic Ball Grid Array, Multilayer (PBGAM1)
PS	Power Quad Shrink Flat Package (SQFP2)

**Table 6. ORCA OR3LxxxB Series Package Matrix**

Devices	208-Pin EIAJ/SQ	240-Pin EIAJ/SQ	352-Pin PBGA	432-Pin PBGA	680-Pin PBGAM
OR3L165B	CI	CI	CI	CI	CI
OR3L225B	—	—	—	CI	CI

Note: C = commercial, I = industrial.

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