MachXO Family

Optimized for Low Density Applications

The MachXO™ family of non-volatile infinitely reconfigurable Programmable Logic Devices (PLDs) is designed for applications traditionally implemented using CPLDs or low-density FPGAs. Combining an optimized look-up table (LUT) architecture with low-cost embedded Flash process technology, the instant-on, easy-to-use MachXO devices are the most versatile, non-volatile PLDs for low-density applications.

The MachXO PLD family offers the benefits of increased system integration by providing embedded memory, built-in PLLs, flexible multi-voltage high-performance LVDS I/Os, remote field upgrade (TransFR™ technology) and low-power sleep mode, all in a single device.

Designed for a broad range of low-density applications that include general purpose I/O expansion, control, bus bridging and power-up management functions, the MachXO PLD family is used in a variety of end markets such as consumer, automotive, communications, computing, industrial and medical.

Key Features and Benefits

- **Non-Volatile, Infinitely Reconfigurable**
  - Instant-on, powers up in less than 1mS
  - Single-chip, no external configuration memory
  - Excellent design security, no bitstream to intercept

- **Performance to 3.5ns Pin-to-Pin**

- **TransFR Technology Allows Simple Field Upgrades**

- **Flexible LUT Architecture**
  - 256 to 2280 LUT4s
  - 73 to 271 I/Os with extensive package options
  - Density migration supported

- **Embedded and Distributed Memory**
  - Up to 27.6 Kbits sysMEM™ Embedded Block RAM
  - Includes dedicated FIFO control logic
  - Up to 7.7 Kbits distributed RAM

- **Flexible I/O Buffer**
  - Programmable sysIO™ buffer supports wide range of interfaces:
    - LVCMOS 3.3/2.5/1.8/1.5/1.2
    - LVTTL
    - PCI*
    - LVDS*, Bus-LVDS*, LVPECL*, RSDS*

- **sysCLOCK™ PLLs**
  - Up to two analog PLLs per device
  - Clock multiply, divide and phase shifting

- **Sleep Mode Reduces Standby Power to <100µA**

- **System-Level Support**
  - IEEE Standard 1149.1 Boundary Scan
  - On-board 20MHz oscillator for configuration and user logic
  - Devices operate with 3.3V, 2.5V, 1.8V or 1.2V power supply

- **Broad Device Offering**
  - Commercial: 0 to 85°C (TJCOM)
  - Industrial: -40 to 100°C (TJIND)
  - AEC-Q100 qualified: -40 to 125°C (TJAUTO)

* MachXO1200 and 2280 devices only.
**MachXO Architecture**

**Architecture Overview**
MachXO PLDs are designed to offer a low-cost, flexible alternative for applications traditionally served by CPLDs or low-density FPGAs. Built with an extremely efficient architecture, MachXO PLDs deliver excellent pin-to-pin performance, support for high-speed I/Os, embedded block RAM, and sysCLOCK PLLs.

**PFU Block Diagram**

**MachXO Block Diagram**

**sysMEM Configuration Options**

<table>
<thead>
<tr>
<th>Single Port</th>
<th>Dual Port</th>
<th>PseudoDual Port</th>
<th>FIFO</th>
</tr>
</thead>
<tbody>
<tr>
<td>8192 x 1</td>
<td>8192 x 1</td>
<td>8192 x 1</td>
<td>8192 x 1</td>
</tr>
<tr>
<td>4096 x 2</td>
<td>4096 x 2</td>
<td>4096 x 2</td>
<td>4096 x 2</td>
</tr>
<tr>
<td>2048 x 4</td>
<td>2048 x 4</td>
<td>2048 x 4</td>
<td>2048 x 4</td>
</tr>
<tr>
<td>1024 x 9</td>
<td>1024 x 9</td>
<td>1024 x 9</td>
<td>1024 x 9</td>
</tr>
<tr>
<td>512 x 18</td>
<td>512 x 18</td>
<td>512 x 18</td>
<td>512 x 18</td>
</tr>
<tr>
<td>256 x 36</td>
<td>–</td>
<td>256 x 36</td>
<td>256 x 36</td>
</tr>
</tbody>
</table>

**MachXO Voltage Options**

- **1.2V** 
- **3.3V** 
- **1.2 to 3.3V** 
- **1.8 to 3.3V** 

**sysCLOCK PLL Block Diagram**

**sysIO Buffer Supports High-Bandwidth I/O Standards**

- **LVCMOS / LVTTL**
  - Hotsocketing capable
  - Programmable slew rate
  - Programmable drive strength
  - Programmable pull-up, pull-down, bus friendly
  - Programmable open drain
  - Programmable Schmitt element

- **PCI, LVDS, LVPECL, Bus-LVDS, RSDS**
Easy Field Updates
MachXO PLDs include Lattice’s exclusive Transparent Field Reconfiguration (TransFR) technology. TransFR technology allows logic to be updated in the field without interrupting system operation.

Step 1
Program Flash in background while logic functions

Step 2
Precisely control I/Os and initiate Flash to SRAM transfer through JTAG.

MachXO Configuration
MachXO PLDs include both Flash and SRAM technology to provide “instant-on” capabilities in a single low-cost device. At power-up, configuration data is transferred from Flash to SRAM cells in less than 1mS. Both SRAM and Flash memory can be programmed from a JTAG port. This combination of SRAM and Flash enables easy field updates via Lattice’s unique TransFR technology. MachXO PLDs have a security scheme that prevents readback and, by using Flash internally, Lattice eliminates bit stream snooping.

MachXO Sleep Mode Reduces Power by a Factor of 100X!

<table>
<thead>
<tr>
<th>Characteristic</th>
<th>Normal Mode</th>
<th>Off</th>
<th>Sleep Mode</th>
</tr>
</thead>
<tbody>
<tr>
<td>SLEEPN Pin</td>
<td>High</td>
<td>X</td>
<td>Low</td>
</tr>
<tr>
<td>Static $I_{DD}$</td>
<td>Typically &lt;10mA</td>
<td>0</td>
<td>Typically &lt;100µA</td>
</tr>
<tr>
<td>Power Supplies</td>
<td>Normal Range</td>
<td>0</td>
<td>Normal Range</td>
</tr>
<tr>
<td>Logic Operation</td>
<td>User Defined</td>
<td>Non Operational</td>
<td>Non Operational</td>
</tr>
<tr>
<td>I/O Operation</td>
<td>User Defined</td>
<td>Tri-State (&lt;1mA leakage)</td>
<td>Tri-State (&lt;10µA leakage)</td>
</tr>
</tbody>
</table>

MachXO Application Examples
Low-cost system integration

Power Up and Control

Low power cycling
Free, Easy-to-Use Lattice Software

Lattice Diamond® design tools offer a comprehensive design environment for the MachXO architecture and other device families. Featuring design exploration, ease of use, improved design flow, and numerous other features, Diamond allows you to complete designs faster, easier, and with better results than ever before.

Evaluation and Development Boards

Lattice offers a number of evaluation and development boards that provide a complete and easy-to-use platform to evaluate the performance of the MachXO, or aid in the development of custom designs.

Reference Design Portfolio

Lattice offers an expanding portfolio of IP cores and reference designs targeted for low-density applications. Optimized for the MachXO architecture these include popular protocol and connectivity standards such as I2C, SPI, UART and PCI. The reference designs, source codes and documentation can be downloaded for free from the Lattice website. For more information, go to www.latticesemi.com/ip.

Device Selection Guide

<table>
<thead>
<tr>
<th>Parameter</th>
<th>LCMXO256</th>
<th>LCMXO640</th>
<th>LCMXO1200</th>
<th>LCMXO2280</th>
</tr>
</thead>
<tbody>
<tr>
<td>LUTs</td>
<td>256</td>
<td>640</td>
<td>1200</td>
<td>2280</td>
</tr>
<tr>
<td>Distributed RAM (Kbits)</td>
<td>2</td>
<td>6.1</td>
<td>6.4</td>
<td>7.7</td>
</tr>
<tr>
<td>Embedded Block RAM – EBR (Kbits)</td>
<td>–</td>
<td>–</td>
<td>9.2</td>
<td>27.6</td>
</tr>
<tr>
<td>Number of EBR Blocks</td>
<td>–</td>
<td>–</td>
<td>1</td>
<td>3</td>
</tr>
<tr>
<td>$V_{cc}$ Voltage (V) Options</td>
<td>1.2V or 1.8/2.5/3.3V</td>
<td>1.2V or 1.8/2.5/3.3V</td>
<td>1.2V or 1.8/2.5/3.3V</td>
<td>1.2V or 1.8/2.5/3.3V</td>
</tr>
<tr>
<td>Number of PLLs</td>
<td>–</td>
<td>–</td>
<td>1</td>
<td>2</td>
</tr>
<tr>
<td>Number of I/O Banks</td>
<td>2</td>
<td>4</td>
<td>8</td>
<td>8</td>
</tr>
<tr>
<td>Maximum Number of I/Os</td>
<td>78</td>
<td>159</td>
<td>211</td>
<td>271</td>
</tr>
<tr>
<td>Maximum Number of LVDS Pairs*</td>
<td>–</td>
<td>–</td>
<td>1</td>
<td>2</td>
</tr>
</tbody>
</table>

** Packages & I/O Combinations

| 100-pin TQFP (14 x 14 mm)**  | 78       | 74       | 73        | 73        |
| 144-pin TQFP (20 x 20 mm)    | 113      | 113      | 113       | 113       |
| 100-ball csBGA (8 x 8 mm)    | 78       | 74       | 101       | 101       |
| 132-ball csBGA (8 x 8 mm)    | 101      | 101      | 211       | 211       |
| 256-ball caBGA (14 x 14 mm)  | 159      | 211      | 211       | 211       |
| 256-ball tFBGA (17 x 17 mm)  | 211      | 211      | 211       | 211       |
| 324-ball tFBGA (19 x 19 mm)  | 271      | 271      | 271       | 271       |

* Number of LVDS outputs can be increased by emulating with external resistors.
** In the 100-pin TQFP package, designs can not migrate from LCMXO640 to 1200.