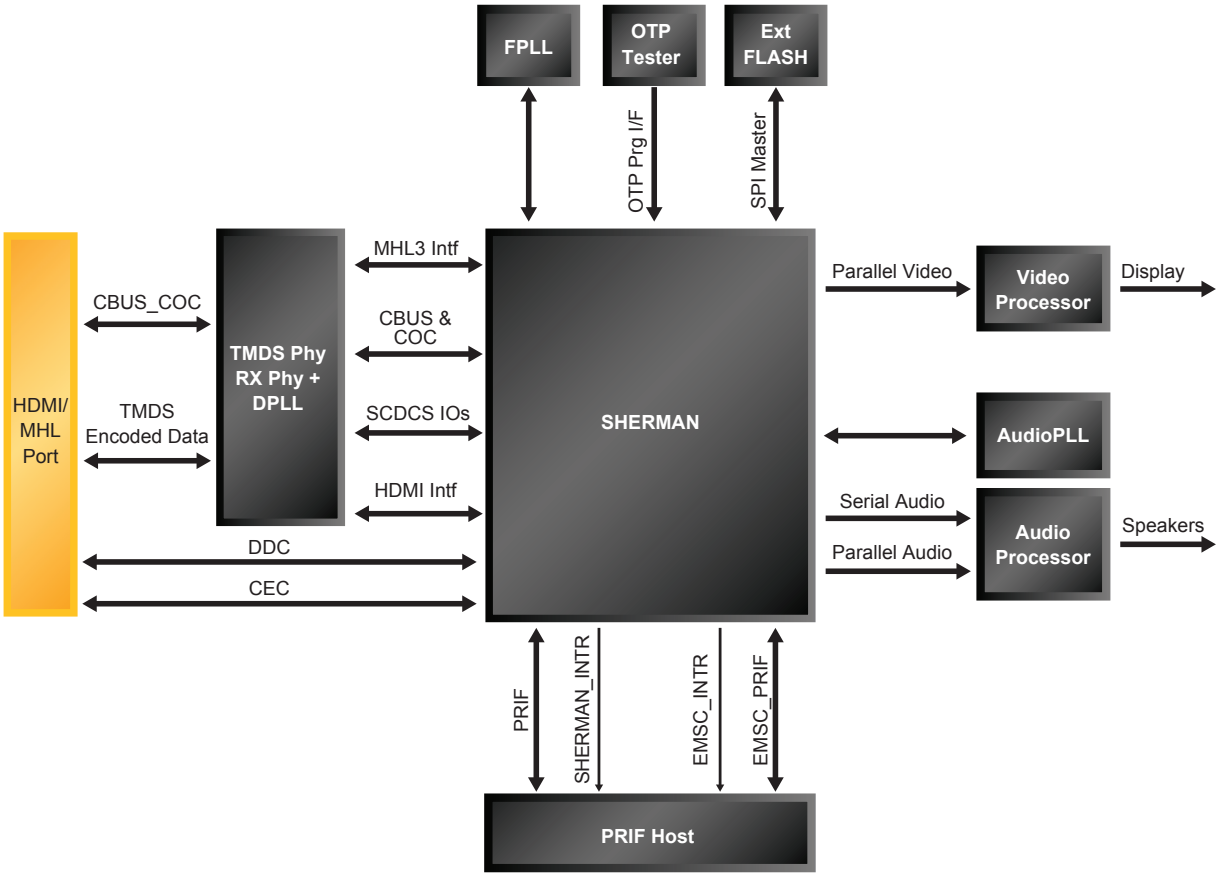
Lattice Semiconductor HDMI® 2.0 Transmitter IP

Lattice HDMI 2.0 transmitter controller IP is a highly configurable, digital TX IP, featuring HDMI 2.0 and HDCP 2.2. The output enables a 600M characters per second/channel and three-lane TMDS performance required to deliver 4Kx2K @60Hz 4:4:4 content to a 4K display. It can also output HDMI 1.4b and HDCP 1.4 depending on the capabilities of the sink.

Configurable HDMI 2.0 Transmitter Interface IP



Key Features

HDMI 2.0 Controller

- Operation of TMDS encoder up to 600M characters per second/channel with 4K60 support
- Scrambling for EMI/RFI reduction on clock and data channels
- DDC Master for Status and Control Data Channel (SCDC)
- Supports YCbCr 4:2:0 pixel encoding with ½ TMDS Character rate
- Supports video and audio formats according to CEA-861-F
- Supports colorimetry defined in ITU-R BT. 2020
- Supports CEC 1.4
- Backward compatible with HDMI 1.4b specification

HDCP 2.2

- Compliant with HDCP 2.2 specification for HDMI 2.0 and the HDCP 1.4 specification for HDMI 1.4b
- Integrated Lattice IP HDCP 2.2 encoder with embedded 8051
- Embedded OTP ROM with BIST controller

HDMI 2.0 PHY

- Compliant with HDMI 1.4/2.0 and DVI 1.0 standards
- Easy integration into customer's SoC with a corresponding HDMI TX IP core
- Supports HDMI 2.0 scramble feature
- Supports 25~600MHz link clock and 8/10/12 bit color mode
- Supports clock multiplication for Deep Color implementation and pixel repetition modes

Controller Interface

Video Interface

- 10 bpp/12 bpp Deep Color for RGB or YCbCr 4:4:4
- 16/20/24-bit YCbCr 4:2:2
- 10-bit or 12-bit YCbCr 4:2:0 for 4K x 2K
- Multi-colorspace converter: Programmable 3x3 matrix operator, plus 64 pre-defined sets of coefficients for standard color space
- Up-/down-sampling between 4:4:4 and 4:2:2, or 4:2:2 and 4:2:0

Audio Interface

- 8-channel I^2S
- 8-channel DSD
- S/PDIF (PCM, Dolby Digital, DTS)
- 2:1 and 4:1 down-sampling
- Packetized Parallel Audio Interfacen (PAI) for 3D and multi-stream audio

PHY Interface

- IP is designed to interface with Lattice HDMI 2.0 PHY

Misc. Interface

- I^2C slave for register access
- SPI slave for HDCP 2.0 PRAM fast access
- Parallel Register Interface (PRIF) for easy integration to SoC for register access

Deliverables

Controller Deliverables

- **Licensed Core Deliverable:**
  - Synthesizable and un-encrypted Verilog RTL for HDMI 2.0 TX digital supporting HDCP 2.2
- **Licensed Core Scripts and Environment:**
  - Synopsys synthesis example scripts and constraint files
  - Prime Time pre-layout scripts
  - Conformal LEC formal verification example scripts
  - Simulation Environment in System Verilog
  - Test bench to verify IP
  - Regression test suite
  - Test invoking scripts
- **Licensed Core Documentation:**
  - Integration guidelines document
  - Design overview, I/O description document
  - Test bench description and regression list document
  - Programming registers spreadsheet with description
  - Digital design datasheet
- **Software Deliverable:**
  - Reference software in source code for configuration and control of licensed core
  - Software documentation

PHY Deliverables

- **GDS for the HDMI PHY IP hard macro and glue logic as RTL**
- **.lib timing views (slow, typical, fast)**
- **LVS netlist**
- **LVS/DRC log file**
- **Integration guidelines document**
- **Data sheet**
- **Silicon characterization report**
- **PHY model**

Applications Support
www.latticesemi.com/support

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