Transmitter IP Core Incorporating HDMI® Specification Version 1.4a

Supporting features, such as 3D over HDMI, HDMI Ethernet Channel, and Audio Return Channel in addition to HDMI 1.3 feature set

Lattice Semiconductor designs, tests and licenses transmitter and receiver IP cores that incorporate features of HDMI specification version 1.4a. The IP cores support 3D over HDMI, HDMI Ethernet Channel, as well as Audio Return Channel capabilities to offer an enhanced entertainment experience that brings 3D functionality to the home theater and simplifies device connectivity. Lattice is one of the founders of the HDMI standard and operates HDMI Authorized Testing Centers worldwide.

Applications

- 3D Video for Movies, Games and Broadcast
- Blu-ray™ & DVD Disc
- Set-Top Box
- PVR Functions
- A/V Receivers & Home Theater
- Portable CE Devices

Key Features

- 1080p/60Hz
- HDMI Ethernet Channel
- Audio Return Channel
- 48-bit Deep Color Video
- 3D over HDMI
- CEC

The HDMI 1.4a specification consolidates the transmission of HD video, audio, data and control into a single cable by enabling high-speed, bidirectional communication through the HDMI cable.

Lattice's TX IP cores support both HDMI 1.3 and HDMI 1.4a features, such as HDMI Ethernet Channel and Audio Return Channel. An HDMI Ethernet Channel enabled device can send and receive data via 100 Mbps Ethernet over an HDMI cable utilizing the new IP core and the customer's own Ethernet transceiver. The Audio Return Channel allows the TV tuner to send audio streams from the TV to an HDMI attached A/V receiver to improve sound quality.

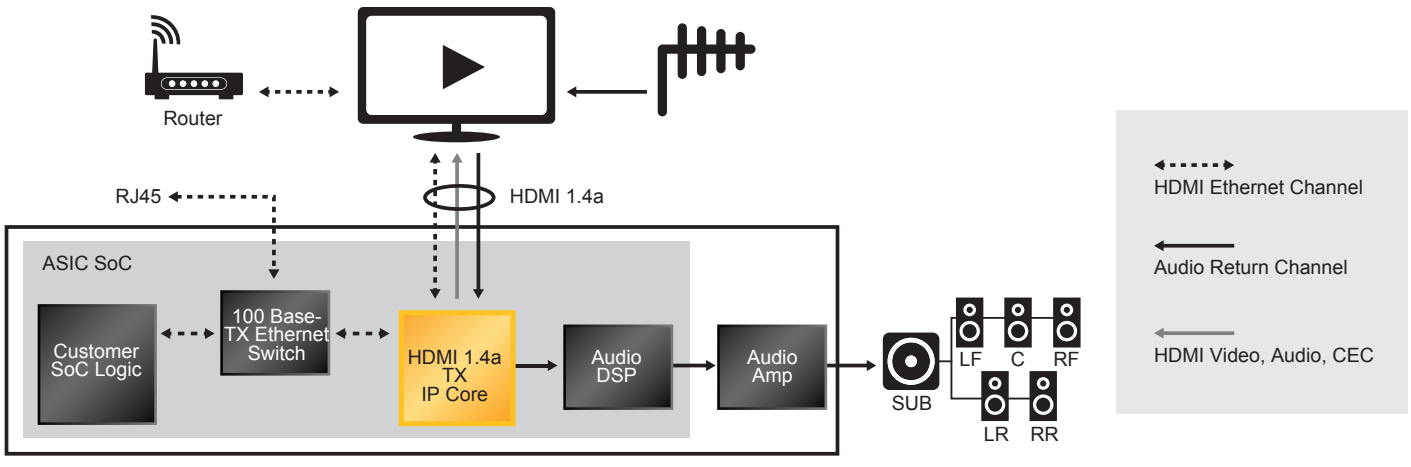
All mandatory and many optional 3D video formats defined in the HDMI 1.4a specification support up to 1080p frame size.

Lattice's TX IP core supports all relevant audio formats, while its colorspace converter allows convenient interfacing with most video decoders. This TX IP core is configurable, providing the SoC designer access to multiple internal interfaces and hardware blocks, potentially reducing integration time and gate count. Lattice's ASSPs also include High-bandwidth Digital Content Protection (HDCP).

In addition to market leading HDMI 1.4a features, the IP cores offer key advantages to SoC manufacturers, including reduced bill of materials cost, as well as lower power consumption for mobile applications. Lattice's industry leadership and unparalleled expertise helps its IP customers accelerate time-to-market through shorter design cycles and faster compliance testing with the assurance of compatibility with hundreds of millions of HDMI-enabled digital TVs worldwide.

Lattice offers the broadest range of silicon proven TX and RX IP solutions, incorporating HDMI features for use in numerous consumer electronics applications.

Transmitter Application Incorporating HDMI 1.4a Feature



Blu-ray Disc Player, Set-top-Box, A/V Receiver...

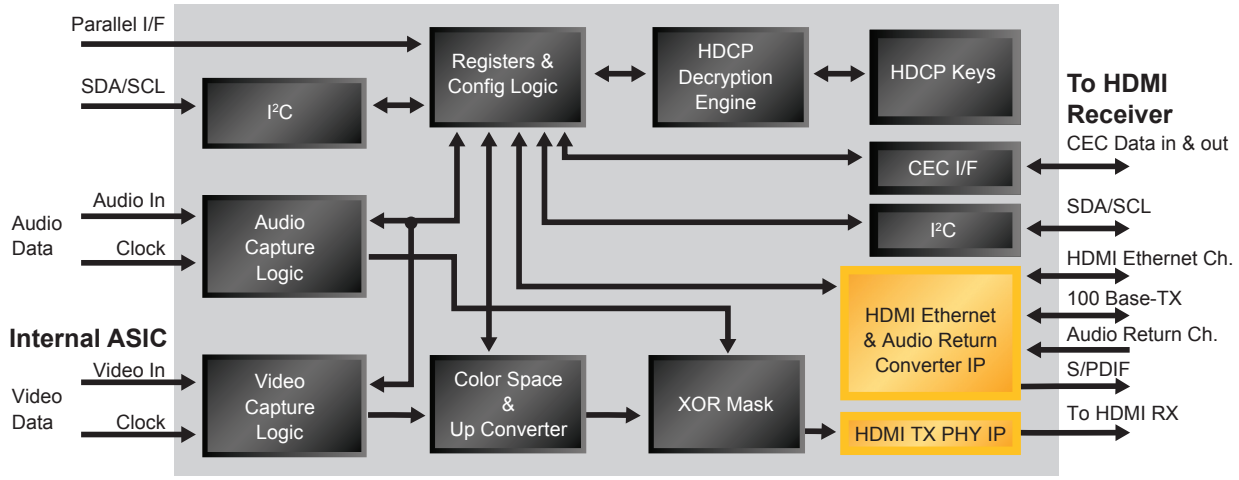
General Features

- **Digital Video Inputs**
  - 24/30/36/48-bit RGB/YCbCr 4:4:4 (Deep Color)
  - x.v.Color
  - 16/20/24-bit YCbCr 4:2:2
  - 8/10/12-bit YCbCr 4:2:2 (ITU 601 and 656)
  - 12/15/18/24-bit, dual-edge clocking input modes
  - Separate and embedded syncs
- **Video Processing**
  - Resolutions up to 16-bit 1080p30 and 12-bit 1080p60
  - Color-space conversion
  - Support of all mandatory and many optional HDMI 1.4a 3D video formats up to 1080p
  - 4:2:2-to-4:4:4 and 4:4:4-to-4:2:2 conversion
- **Digital Audio Inputs**
  - Industry standard S/PDIF, I²S and parallel input
  - Direct Stream Digital (DSD) for Super Audio CD
  - Dolby® TrueHD and DTS-HD Master Audio™ high bit rate support up to 24Mbit/s
  - 2/8 Channel Dolby Digital®, DTS, DVD Audio and PCM support up to 192 kHz
  - IEC 60958 and IEC 61937 compatible
- **System Operation**
  - Parallel and Slave I²C I/F, Master I²C (HDCP)
  - Interrupt pin and registers
  - Monitor detection (hot plug & receiver detect)
  - HDCP cipher engine encrypts video/audio
  - Programmable Data Enable (DE)
  - CEC (Consumer Electronics Control)
- **Home Network Support and Audio Uplink**
  - HDMI Ethernet Channel <=> 100Base-T Ethernet (100Mbps)
  - Audio Return Channel => S/PDIF out
- **Compliance**
  - HDMI 1.1, 1.2, 1.3 and 1.4a
  - HDCP 1.4
  - EIA/CEA-861D
  - DVI 1.0

Deliverables

- **Digital IP Core**
  - Unencrypted, commented RTL
  - Interface to analog TMDS TX PHY and HDMI Ethernet & Audio Return Converter IP Core
  - Development kit and firmware for CEC (option)
- **Analog IP Core**
  - TMDS TX PHY - .lef, .lib, GDSII
  - HDMI Ethernet & Audio Return Converter - .lef, .lib, GDSII
  - LVS Netlist
- **NC-Verilog Test Bench**
  - Test bench
  - I²C verification modules
  - Audio/video stimulus and monitors
  - HDMI receiver encrypted model
  - Regression test suite
  - Test-invoking scripts
- **Scripts and Documentation**
  - Synopsys synthesis scripts & constraint files
  - Primetime static timing scripts
  - ATPG example scripts
  - Logic-equivalency scripts - RTL2Gates
  - Programming and Integration guidelines
  - Design overview and I/O description
  - Design datasheet

HDMI 1.4a Transmitter IP Core Data Flow



Applications Support
www.latticesemi.com/support

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