

Lattice Radiant Software Known Issues



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Type Conventions Used in This Document

Convention	Meaning or Use
Bold	Items in the user interface that you select or click. Text that you type into the user interface.
<i><Italic></i>	Variables in commands, code syntax, and path names.
Ctrl+L	Press the two keys at the same time.
<code>Courier</code>	Code examples. Messages, reports, and prompts from the software.
<code>...</code>	Omitted material in a line of code.
<code>.</code> <code>.</code> <code>.</code>	Omitted lines in code and report examples.
[]	Optional items in syntax descriptions. In bus specifications, the brackets are required.
()	Grouped items in syntax descriptions.
{ }	Repeatable items in syntax descriptions.
	A choice between items in syntax descriptions.

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Lattice Radiant Software Known Issues

This section lists the known issues and workarounds of the Radiant software. Descriptions include the software versions and devices affected. If you are looking for a workaround to a problem, search for related terms including the tool name or a word from an error message, or scan the Contents. If you want issues for a certain version, search for the version number. This will find issues affecting that version and issues fixed in that version of the software.

Design Entry

Radiant software main window stops working on Windows 10 when Dell Backup and Recovery software is installed

When Dell Backup and Recovery software is installed, it conflicts with the Radiant software, and may cause it to stop working.

Versions affected: 1.0

Fixed: 1.1

Devices affected: All

Bug number: DNG-2303

Workaround: Uninstall Dell Backup and Recovery software.

IP Catalog

When generating PLL, calculations are not performed automatically. User must click “Calculate” button before generating PLL.

- ▶ When using the Radiant IP Catalog graphical user interface, if the Calculate button is not clicked before generating PLL, the PLL analog parameter values in the RTL will be incorrect. This affects all designs using PLL, such as GDDR 7:1 Receive Interface and GDDR with enabled PLL instantiation.

Workaround: For configurations that use PLL, click the "Calculate" button before clicking the “Generate” button.

- ▶ If the ipgen command is used to generate PLL, the PLL analog parameter values in the RTL will be incorrect. This affects all designs using PLL, such as GDDR 7:1 Receive Interface and GDDR with enabled PLL instantiation.

Workaround: For configurations that use PLL, the PLL must be manually generated using the Radiant IP Catalog graphical user interface. Click the “Calculate” button before clicking the “Generate” button.

Devices affected: CrossLink-NX

Bug number: DNG-8701

For the Soft MIPI TX mode, the B side result of clock and data are wrong

For assistance with this issue, please contact Lattice Technical Support.

Versions affected: 2.0

Devices affected: CrossLink-NX

Bug number: DNG-8199, DNG-8640

DPHY derating for CrossLink-NX does not work

For assistance with this issue, please contact Lattice Technical Support.

Devices affected: CrossLink-NX

Bug number: DNG-8247

Simulation

When using Aldec Active-HDL the RTL simulation of DLLDEL will output 'x' for VHDL DDR case when the clk < 100Mhz

Workaround: Initialize clk signal as 1'b1 in the test bench and toggle the other signal after a delay of 20 ns.

Versions affected: 2.0

Devices affected: CrossLink-NX

Bug number: DNG-8401

Constraints Views

Floorplan View: When using the left mouse button to zoom while objects are selected, the selected objects will be lost

Versions affected: 1.0

Fixed: 1.1

Devices affected: All

Bug number: DNG-3231

Workaround: If there are objects selected, zoom using the wheel mouse button or keys Ctrl + and Ctrl – keys.

Timing Constraint Editor: It is not possible to drag and drop objects from RTL view into the Timing Constraint Editor while in Detach mode on certain computers

Versions affected: 1.0

Fixed: 1.1

Devices affected: All

Bug number: DNG-2728

Workaround: If you run into this issue, use “Attach” mode to drag and drop objects from RTL view into the Timing Constraint Editor.

Synthesis

Post-syn fails when using Reveal with soft IP ROM

Workaround: If you need to use Reveal with soft-IP ROM, then the data width of the ROM should be no more than 18 bits.

Versions affected: 2.0

Devices affected: CrossLink-NX

Bug number: DNG- 8627

Lattice Synthesis Engine (LSE) does not implement async mult

LSE does not implement async mult. LSE always uses MAC16.

Versions affected: 1.1

Fixed: 2.0

Devices affected: All

Bug number: DNG-3144

The syn_useioff attribute does not work for LSE

This attribute controls selective register to be pack into I/O pad cell based on timing requirements. LSE "Use IO Registers" Strategy option is set to Auto to use IO registers whenever applicable. Those IO register inferences cannot be individually prevented by the user HDL attribute "syn_useioff = 0".

Versions affected: 1.0, 1.1

Fixed: 2.0

Devices affected: All

Bug number: DNG-3382

Workarounds (2 options):

1. Use the global option "Use IO Registers = False" in Strategy Manager if the design permits, in which LSE will not pack any register into I/O pad cell unless instantiated.
2. Use Synplify Pro for Lattice synthesis tool

No warning message issued by Synplify Pro when Synplify encryption key is missing

When the encrypted design without a valid key is not be synthesized by Synplify Pro, it should provide a warning message. Note that the encrypted design will still be protected.

Versions affected: 1.1

Fixed: 2.0

Devices affected: All

Bug number: DNG-5300

For designs with multiple assignments to same parameter, Synplify Pro synthesis will pick up the first assignment without any warning message. Users may get unexpected results

Versions affected: 1.0

Fixed: 1.1

Devices affected: All

Bug number: DNG-2077

Workaround: Remove any unused assignments and keep the ones with the expected value.

LOC attribute does not work for locating registers for Synplify Pro synthesis

Versions affected: 1.0

Fixed: 1.1

Devices affected: All

Bug number: DNG-2767

Workaround: Use "Idc_set_location" constraint in .pdc file to set location constraints for registers

Implementation Flow

NVCM Boot time fluctuates when Osc frequency range strategy setting is set to 'Fast'

Workaround: Use 'Medium' setting.

Versions affected: 2.0

Devices affected: iCE40UP

Bug number: DNG-6499

MAP does not report correct number of SEIO33 I/Os when sysCONFIG pins are used, and this can cause a resource violation

Workaround: In Radiant software, when enabling sysCONFIG pins in an LIFCL device, you need to set Idc_prohibit constraints on the sysCONFIG pins.

For example:

If you set JTAG_PORT = ENABLE, you need to prohibit usage of 4 JTAG pads: TDI, TCK, TMS, TDO. Those 4 pads are E12, F12, E13, E11 in LIFCL-40 CSBGA289 package.

So, add the following constraints in the design:

```
{noformat}
Idc_prohibit -site E12
Idc_prohibit -site F12
Idc_prohibit -site E13
Idc_prohibit -site E11
{noformat}
```

Versions affected: 2.0

Devices affected: CrossLink-NX

Bug number: DNG-8636

Place & Route (PAR): Some designs may encounter long run times

Versions affected: 1.0

Fixed: 1.1

Devices affected: All

DNG-3007

Workaround: Turn off the Place & Route Design Strategy “Path-based Placement” option.

Timing Analysis

PLL output is always 0 with advdataflow and dbg option for Active-HDL and Riviera

Workaround: Don't use options advdataflow and dbg to run simulation with Active-HDL.

Versions affected: 2.0

Devices affected: CrossLink-NX

Bug number: DNG-7752

Hold Time calculation shows user speed grade for setup and hold calculation.

The timing engine uses the user speed grade for both setup and hold calculation. This is not the behavior users of Diamond software are expecting. Future versions of Radiant software will change this behavior to do setup calculation at the user speed grade and hold calculation at the M speed grade.

Versions affected: 1.1

Fixed: 2.0

Devices affected: All

Bug number: DNG-5651

If there are overlapping set_clock_uncertainty constraints, the most constraining one will be honored by the Timing engine

Here is an example of the issue:

```
set_clock_uncertainty 1.33 -from [get_clocks myclk1] -to [get_clocks myclk2] -setup
```

```
set_clock_uncertainty 3.0 [get_clocks myclk2] -setup
```

In the case above, 3.0 will be applied as the constraint.

Versions affected: 1.0

Fixed: 1.1

Devices affected: All

Bug number: DNG-2761

Workaround: None. This limitation will be reviewed and addressed in future version.

Programming

Programmer software may not work properly if you open two or more Radiant software projects at the same time

When two Radiant software projects are opened at the same time with only one using the imported .xcf file, the Programmer software may not operate properly. Clicking on the Programmer icon for the first project opens the .xcf file. If you subsequently click on the programmer icon of the second project, the Programmer will close the first .xcf file and open the second. The second .xcf file will be empty and Programmer will show an error message.

Versions affected: 1.0

Fixed: 1.1

Devices affected: All

DNG-2915

Workaround: If you need two Radiant software projects opened at the same time, close the first Radiant software project before clicking on the programmer icon of the second project.

Other Topics

Tutorial project source files embedded in Radiant 2.0 software for CrossLink-NX Tutorial are incorrect and cause a synthesis error.

Workaround: Use updated tutorial project source files. A .zip file containing updated tutorial project source files can be downloaded from here:

https://www.latticesemi.com/view_document?document_id=52825

The updated tutorial can be downloaded from here:

https://www.latticesemi.com/view_document?document_id=52757

Versions affected: 1.0

Devices affected: CrossLink-NX

Bug number: DNG-8739

Revision History

The following table gives the revision history for this document.

Date	Version	Description
12/17/2019	2.0	Added new known issues for Radiant 2.0. Listed previous known issues that have been resolved
04/08/2019	1.1	Added new known issues for Radiant 1.1. Listed previous known issues that have been resolved
02/14/2018	1.0	Initial Release.