Lattice Software Known Issues

February 2015
Copyright
Copyright © 2015 Lattice Semiconductor Corporation. All rights reserved. This
document may not, in whole or part, be reproduced, modified, distributed, or publicly
displayed without prior written consent from Lattice Semiconductor Corporation
(“Lattice”).

Trademarks
All Lattice trademarks are as listed at www.latticesemi.com/legal. Synopsys and
Synplify Pro are trademarks of Synopsys, Inc. Aldec and Active-HDL are trademarks
of Aldec, Inc. All other trademarks are the property of their respective owners.

Disclaimers
NO WARRANTIES: THE INFORMATION PROVIDED IN THIS DOCUMENT IS "AS IS"
WITHOUT ANY EXPRESS OR IMPLIED WARRANTY OF ANY KIND INCLUDING
WARRANTIES OF ACCURACY, COMPLETENESS, MERCHANTABILITY,
NONINFRINGEMENT OF INTELLECTUAL PROPERTY, OR FITNESS FOR ANY
PARTicular PURPOSE. IN NO EVENT WILL LATTICE OR ITS SUPPLIERS BE
LIABLE FOR ANY DAMAGES WHATSOEVER (WHETHER DIRECT, INDIRECT,
SPECIAL, INCIDENTAL, OR CONSEQUENTIAL, INCLUDING, WITHOUT
LIMITATION, DAMAGES FOR LOSS OF PROFITS, BUSINESS INTERRUPTION, OR
LOSS OF INFORMATION) ARISING OUT OF THE USE OF OR INABILITY TO USE
THE INFORMATION PROVIDED IN THIS DOCUMENT, EVEN IF LATTICE HAS
BEEN ADVISED OF THE POSSIBILITY OF SUCH DAMAGES. BECAUSE SOME
JURISDICTIONS PROHIBIT THE EXCLUSION OR LIMITATION OF CERTAIN
LIABILITY, SOME OF THE ABOVE LIMITATIONS MAY NOT APPLY TO YOU.

Lattice may make changes to these materials, specifications, or information, or to the
products described herein, at any time without notice. Lattice makes no commitment to
update this documentation. Lattice reserves the right to discontinue any product or
service without notice and assumes no obligation to correct any errors contained
herein or to advise any user of this document of any correction if such be made. Lattice
recommends its customers obtain the latest version of the relevant information to
establish that the information being relied upon is current and before ordering any
products.
# Type Conventions Used in This Document

<table>
<thead>
<tr>
<th>Convention</th>
<th>Meaning or Use</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>Bold</strong></td>
<td>Items in the user interface that you select or click. Text that you type into the user interface.</td>
</tr>
<tr>
<td><em>Italic</em></td>
<td>Variables in commands, code syntax, and path names.</td>
</tr>
<tr>
<td><strong>Ctrl+L</strong></td>
<td>Press the two keys at the same time.</td>
</tr>
<tr>
<td><strong>Courier</strong></td>
<td>Code examples. Messages, reports, and prompts from the software.</td>
</tr>
<tr>
<td>...</td>
<td>Omitted material in a line of code.</td>
</tr>
<tr>
<td>.</td>
<td>Omitted lines in code and report examples.</td>
</tr>
<tr>
<td>[ ]</td>
<td>Optional items in syntax descriptions. In bus specifications, the brackets are required.</td>
</tr>
<tr>
<td>( )</td>
<td>Grouped items in syntax descriptions.</td>
</tr>
<tr>
<td>{ }</td>
<td>Repeatable items in syntax descriptions.</td>
</tr>
<tr>
<td></td>
<td>A choice between items in syntax descriptions.</td>
</tr>
</tbody>
</table>
Contents

Chapter 1  Lattice Diamond  1
Design Entry  1
  Cannot place CLKI in Clarity  1  
  Clock placed in Clarity generated without buffer  1  
  Clarity cannot reconfigure a module  2  
  Device Selector shows 8 EBR for MachXO3L 640 and 1300  2  
  LDC Editor may cause errors in SDC files  2  
  Platform Designer rejects multiple hot swap components on an ASC  3  
  PAR fails with missing ECLKBRIDGE in ECP5  3  
  Platform Designer displays Current Monitor trip points that are inconsistent with the datasheet  3  
  Diamond erroneously issues TRACE report warning for PGROUP  4  
  Signal groups are not supported in the Platform Designer Generate Stimulus dialog box  4  
  Cannot generate schematic symbol  4  
  Cannot shorten multiple wires by dragging in the Schematic Editor  5  
  Some bus attribute settings in Schematic Editor may cause an error or get lost  5  
  Cannot select multiple areas of wires in Schematic Editor  5  
  Dragging wire end in the Schematic Editor does not change wire length or direction  6  
  Schematic components are deselected after being dragged or moved  6  
  Schematic Editor limitation on deselecting components  6  
IPExpress  6  
  MULT module has lower bits tied low after programming LatticeECP3  6  
  PLL has Fractional-N Divider of 1 instead of 0  7  
  Process view is not cleared when a module is regenerated  7  
  Calculate button for PLL produces wrong values  8  
  Incorrect delay times for DDR modules for MachXO2  8  
Simulation  8  
  Fails on missing GENERIC statement in OSCH  8  
  Simulation fails on incorrect PMI headers  8
Errors occur in ecp5um_serdes.ibs file at some pin declarations
The MachXO2 SEDFA simulation model does not contain timing
requirements for the signal SEDFRCERR
Active-HDL LEII allows only one design to be simulated at a time even
with a multi-seat license
Simulation Wizard ignoresRTL file modifications that change the top-
level
VHDL package files are not sent to the simulator from Simulation Wizard
in some cases
Active-HDL 8.2 may issue compilation warnings after using Simulation
Wizard
Aldec Active-HDL may return error when .sdf file is located in simulation
project folder
Verilog front-end simulation module compilation fails using Aldec Active-
HDL
After upgrade, Active-HDL cannot open configuration
On Windows 7 when launching the Simulation Project File (SPF) in
Diamond, the Simulation Wizard's Add Source page does not update
properly
Preference Views
Spreadsheet View takes a long time to open
There is no DRC check on the Clock Jitter value entered
Global preference sheet erroneously shows "DISABLE" for
MASTER_SPI_PORT
PAR-assigned pins cannot be cross-probed from Spreadsheet View
Selected nets in NCD View do not get added to the Create New UGROUP
dialog box
Selected nets in Netlist View do not get added to the Create New
UGROUP dialog box
Regions and groups in Physical View are not displayed in the colors
assigned to them
Physical View does not match delay path colors or allow custom
colors
Synthesis
LSE fails on IP for Platform Manager 2
LSE does not process input_delay and output_delay constraints
properly
Synthesis fails with schematic file on Windows 8
Design with DDR_GENERIC fails in synthesis
Defaults in Diamond strategies are different from Synplify Pro itself
LSE does not convert gated clocks driving distributed RAM primitives
Synplify Pro for Lattice fails to produce _prepass.srd file
After synthesis with Synplify Pro, port or net names are changed
Synthesis warns that EBR CSDECODE property should be binary
The last EDIF source in the source file list is automatically treated as the
top module
Implementation Flow
PAR TRACE Report does not include frequency tolerance
Diamond crashes during Translate Design after setting constraints with
Spreadsheet View
PAR report shows placement score values that vary greatly between
phases
PAR report shows placement score values that vary greatly between phases 21
PAR report does not show placement results sorted by timing score 22
Preference semantic errors reported during design implementation 22
Implementation succeeds despite missing EDIF source file 23
PAR may fail to place PIO PGROUP if clock PIO driver is assigned to the same bank 23
Map says to set SHAREDEBRINIT=ENABLE but it already is 23
If more than one EBR has the same INIT, data will be shared if at least one EBR sets INIT_DATA to STATIC and others to INIT_DATA=DYNAMIC 24
Map says WISHBONE clock frequency of EFB module can be up to 166 MHz 24
Map changes DEV_DENSITY incorrectly for U devices 24
IO Timing Report and Trace Report numbers do not match when using SS on INPUT_SETUP 25
MachXO2 design issues PAR warnings for PLL clocks that do not match their divider settings 25
TRACE reports errant clock speed that exceeds target specifications for GDDRX1 designs 26
Default PCICLAMP setting in Spreadsheet View produces illegal combination error 26
Configuration data not fully loaded into EBR from UFM 27
Components within a wide LUT have different PGROUP settings 27
Map Design fails on Linux 64-bit Red Hat 4 machine 28
Design fails in Translate Design with errors about undefined modules or cannot open file 28
Slave Chip Select pins of MachXO2 are not reserved 28
Map does not report an error condition for MULTICYCLE constraint containing net with invalid name 29
"Invalid LPF_RESISTOR value" error from MAP process 29
CONFIG_SECURE attribute in VHDL gets ignored by PAR 30
Error message for MCCLK preference 30
Timing Analysis 31
Unconstrained-path sequence causes cross-probing error in Timing Analysis View 31
In Linux, a memory fault error occurs when exiting Diamond right after closing Timing Analysis view 31
When cross-probing a timing path from the Timing Analysis view's Path Table to a report, it fails to display the corresponding path 31
In Timing Analysis view, unnecessary PGROUP preferences found in the TPF file result in warning messages 32
The Timing Analysis view does not display a path in the view that should appear in the Path Table 33
Power Calculator 33
Power Calculator “Catch unknown exception” error causes Diamond to hang 33
Power Calculator shows incorrect PLL information when TWR file is used 33
Routed design with SERDES shows incorrect channels in Power Calculator 34
Power Calculator underestimates power for some LVCMOS I/O 34
Power Calculator over-estimates power for MachXO2 35
Reveal Hardware Debug 35
  Reveal Analyzer fails to open on Windows 8 35
  Reveal Analyzer crashes when scanning devices 35
  Reveal triggers wrong with 3 trigger units and Max Sequence Depth of 4 35
  Reveal Inserter fails to link a signal 36
  Recently used platforms do not appear in the Open Platform list 36

Other Topics 36
  Hysteresis is not set for the LVTLL33 IO_TYPE 36
  EPIC Help does not display in Firefox 37
  VME file missing USERCODE verification opcode 37
  Tutorials require “Diamond Free License - For Versa Kit Only” for users of free Diamond software 37
  EPIC DRC returns incorrect number of errors and warnings 38
  Maximum number of MachXO2 user I/Os differs from the number shown in Diamond 38
  Process view not updated after changing source file list 38
  Incremental Design Flow can fail if design exceeds unmatched component threshold and contains XSIOLOGIC 39
  ECO Editor signal probe displayed incorrectly 39
  Incremental Design Flow may not recognize anchor and bounding box 39
  Error messages appear when memory is initialized to all 1s 40
  Four ispLeverDSP blocks generate compare errors in Matlab/Simulink 7.5.0 (2007b) 40
  The ispLeverDSP Viterbi Decoder 4.5 will not generate in Matlab/Simulink 7.5.0 (2007b) 41
  Status icons in Reports view do not indicate when Tool Reports need updating 41
  VCS cannot find EFB module 41
  Universal File Writer for Linux does not display all of the valid file types 42
  Help does not work in Google Chrome browser 42
  Cannot change column widths in Hierarchy view 43
  Generate Hierarchy does not expand all the files 43
  Files modified by another application may not get saved in Diamond 43
  Error running BKM check to validate VCD files 43
  Predefined parameters set in the HDL Parameters section of the Project Properties dialog cannot be handled when generating hierarchy 44
  Download of a software update does not work 45
  Wrong file extension shown in “Managing Project Sources” help topic 45
  Double-clicking .ldf cannot invoke Diamond on some Windows computers 45
  HDL Diagram cannot display hierarchy correctly for some pure EDIF designs 46
  HDL Diagram cannot display hierarchy correctly for some VHDL/EDIF designs 46
  Removing an implementation from Diamond does not delete the result files from the implementation directory 46
  ispLeverDSP cannot work properly due to the missing search path 47
Chapter 2  Other Lattice Software  49

ispLEVER Classic  49
UAC dialog will display with multiple schematic designs  49
Timing Analysis View display status is incorrect after reloading  50
Constraint Editor does not reload design changes automatically  50
Pullup on global reset does not work  50
IO power guide (PG) property wrongly set to Enable  50
Wrong device package information for ispGAL22V10av-75LN shown in
Fitter Report and Jedec File  51
Some signals in sub-modules cannot be viewed in the Active-HDL
waveform editor  51
Some mature products are not supported by ispLEVER Classic  51
Functional simulation result incorrect in Lattice Logic Simulator  52
ORCA Series 3 shows in the Device Selector Dialog by error  53
ModelSim fails to simulate due to obsolete simulation library  53
EPIC allows LUT editing in “No-Logic-Changes” mode  53
Constraint Editor fails intermittently on Unix/Linux  54
ispLEVER Classic requires read-write permission on the folder defined in
$LSC_INI_PATH  54

PAC-Designer  54
PAC-Designer USB driver is not up-to-date with Windows  54
VHDL designs using mixed-case characters can cause error
messages  55
Platform Manager designs with a timer in the VHDL netlist always show
an “X” during simulation  55
Windows 7 does not associate .pac files with PAC-Designer  55
PlatformManager_10-12107_I2C_Utility doesn't work  56
.ini file in c:/lsc_env cannot be written using Windows 7 or Windows Vista
OS  56
VID Demo fails to compile when using VHDL entry  56
PAC-Designer does not support device downloading on Windows 7  57
PAC-Designer crashes when compiling a LogiBuilder design  57
PAC-Designer fails to export Jedec after compiling a LogiBuilder design in
ABEL mode  57
Spaces in PAC-Designer project path are not allowed  58
A Clock Frequency Hz radio button does not work in PAC-Designer  58

LatticeMico System  58
EFB not enabled with MachXO3LF when creating a LatticeMico System
Builder platform  58
Debug Configuration operation may time-out over a slow Linux
network  59
LatticeMico Mutli-Memory deployment does not work under certain
conditions  59
Running LatticeMico32 Flash Deployment in Diamond 32-bit for Windows
may cause error  60
LatticeMico System SPE/Debug printf to console does not display  61
In LatticeMico System, the platform.mk file must be modified to work on
Linux  61
LatticeMico installation “splash screens” appear small on some Linux
systems  62
Items may be missing from dialog boxes on systems running Windows 7
64-bit OS  62
Address locking does not function for components with multiple Wishbone slave ports  63
Cannot launch TCP2JTAGVC2 from command-line shell in Lattice Mico System  63
"Failed to Load USB Driver" error in MSB if Diamond 1.2 is uninstalled  64
Unable to open IPexpress from Lattice Mico System Builder on Linux  64
ispVM System  65
USB2 cables do not work using RedHat 32-bit Linux OS  65
ORCAstra  65
ORCAstra fails when setting up the JTAG Hub interface  65
This section lists the known issues and workarounds of the Diamond software. Descriptions include the software versions and devices affected. If you are looking for a workaround to a problem, search for related terms including the tool name or a word from an error message, or scan the Contents. If you want issues for a certain version, search for the version number. This will find issues affecting that version and issues fixed in that version of the software.

**Design Entry**

**Cannot place CLKI in Clarity**

If a PLL that is not included inside a DDR module drives a common clock to two or more DDR modules, the CLKI signal of the PLL cannot be placed using the Planner tab of Clarity Designer.

If you have this situation in your design, do not place these pins with Clarity Designer. Instead, let the place-and-route function place them.

Versions affected: Diamond 3.4, 3.4.1
Devices affected: ECP5
CR123377

**Clock placed in Clarity generated without buffer**

When generating a Clarity Designer module that includes a DDR interface, you may get a warning message similar to the following:

WARNING - Clock input 'clkop' of interface 'eclk_group0' in component 'abc' is generated without any buffer. Planning for each interface needs special attention. Consult document for more information.
This can happen if you use the Planner tab of Clarity to place the clock signal of the DDR module. Clarity does not properly place the clock signal.

If you see this message, place the DDR clock without using Clarity. See Applying Design Constraints in the online help.

Or, if you need a PLL in the design, drive the clock input from the PLL.

Versions affected: Diamond 3.3
Fixed_3.4
Devices affected: ECP5
CR122392

**Clarity cannot reconfigure a module**

When trying to reconfigure a module in Clarity Designer, you may see an error message that says that the component "is not supported for reconfiguration in this version of Diamond."

If you see this message, contact Lattice support for a patch.

Versions affected: Diamond 3.2
Fixed_3.3
Devices affected: ECP5
CR121072

**Device Selector shows 8 EBR for MachXO3L 640 and 1300**

For MachXO3L 640 and 1300, the Device Selector dialog box shows 8 EBR blocks. It should show 7.

Versions affected: Diamond 3.2
Fixed_3.3
Devices affected: MachXO3L
CR121054

**LDC Editor may cause errors in SDC files**

When editing SDC files using LDC Editor, the target may be incorrect after synthesis and some uses won’t be supported.

As a workaround, write the .ldc file manually.

Versions affected: Diamond 3.2
Fixed_3.3
Devices affected: All
CR120924
Platform Designer rejects multiple hot swap components on an ASC
When you run DRC, after creating two or more hot swap components with fast shutdown enabled on the same ASC device, Platform Designer generates an error message similar to the following:

ASC_NONE can’t be used in HotSwap1 and HotSwap2 at the same time.

There is no workaround for this issue.

Versions affected: Diamond 3.1
Fixed_3.2
Devices affected: Platform Manager 2
CR119823

PAR fails with missing ECLKBRIDGE in ECP5
Place and route fails because an ECLKBRIDGE is missing. This can happen if you used Clarity Designer to add two DDR modules using the same clock but located on different sides of an ECP5. Clarity Designer does not automatically add an ECLKBRIDGE and does not give an error message.

If you have this situation in your design, do not place these pins with Clarity Designer. Instead, let the place-and-route function place them.

Versions affected: Diamond 3.1, 3.2, 3.3, 3.4, 3.4.1
Devices affected: ECP5
CR119489

Platform Designer displays Current Monitor trip points that are inconsistent with the datasheet
The trip points displayed in the Current Monitor Trip Point Selection menu differ, depending on the Hysteresis option selected. When Enabled is selected for Hysteresis, the trip points displayed are inconsistent with those in the datasheet. The correct trip points are those displayed when Disabled is selected, and the menus should be the same for both Enabled and Disabled hysteresis.

Versions affected: Diamond 3.0
Fixed_3.1
Devices affected: Platform Manager 2
CR117823
Diamond erroneously issues TRACE report warning for PGROUP
During design implementation, Diamond sometimes issues a TRACE report semantic error message that includes a list of PGROUP components that do not exist.

This warning is the result of post-map component name checking done by the preference parser, and it can be ignored.

Versions affected: Diamond 2.1, 2.2
Fixed_3.0
Devices affected: LatticeECP3
CR115503

Signal groups are not supported in the Platform Designer Generate Stimulus dialog box
In the Diamond Platform Designer, signal groups do not appear in the Generate Stimulus dialog box. To work around this issue, select individual group members one by one.

Versions affected: Diamond 3.0
Fixed_3.1
Devices affected: Platform Manager 2
CR102680

Cannot generate schematic symbol
When you try to generate a schematic symbol for a module of a VHDL, Verilog HDL, or mixed VHDL/Verilog HDL design in the HDL Diagram of Diamond, you may encounter an error message such as “failed to generate naf file”.

The error is caused by unrelated source files. When generating schematic symbols from the hierarchy tree, to support generic map and parameter values that are required from parent modules, all user design source files are passed to the parser engine. However, the HDL Diagram cannot decide which files related to the module are required before parsing. The parser error in any file stops the process.

Lattice recommends you exclude the unrelated source files from the current implementation of the project before generating a schematic symbol.

Versions affected: Diamond 1.0, 1.1, 1.2
Fixed_1.3

Device affected: All devices
CR52520, 52353
Cannot shorten multiple wires by dragging in the Schematic Editor

In the Schematic Editor, you cannot shorten wires if you have selected too many wires which are very close to each other. Shortening wires by dragging requires enough space to avoid wire overlapping.

In such cases, you can shorten the wires one by one or adjust their positions before shortening them.

Versions affected: Diamond 1.0
Fixed_1.1
Devices affected: All
CR49259

Some bus attribute settings in Schematic Editor may cause an error or get lost

Schematic Editor allows you to set different attribute values for each signal inside a bus. However, the Synthesize Design process can only accept one value for each bus attribute. If it is a VHDL design, the synthesizer will report a syntax error. If it is a Verilog design, the synthesis process can pass but the other attribute values you set for signals inside the bus will be ignored.

To avoid this problem, always set the same attribute value for all signals in a bus.

Versions affected: Diamond 1.0, ispLEVER 8.1
Fixed_8.1SP1, Fixed_1.1
Devices affected: All
CR47672

Cannot select multiple areas of wires in Schematic Editor

When selecting wires in Schematic Editor, the area-selecting method (drawing a rectangle area to enclose multiple wires) only allows you to select one area. You cannot use the Shift key to select additional areas.

Select one area at a time.

Versions affected: Diamond 1.0, 1.1
Fixed_1.2
Devices affected: All
CR47465
Dragging wire end in the Schematic Editor does not change wire length or direction
In the Schematic Editor, if the node connected with the wire end that you drag only has one linked connection, dragging the wire end moves the entire wire instead of changing its length or direction.

Workaround: none.

Versions affected: Diamond 1.0
Fixed_1.1
Devices affected: All
CR47464

Schematic components are deselected after being dragged or moved
The selected components in the Schematic Editor will become deselected after they are dragged or moved to another place.

Versions affected: Diamond 1.0, 1.1
Fixed_1.2
Devices affected: All
CR47100

Schematic Editor limitation on deselecting components
After selecting a component in the Schematic Editor, you cannot deselect it by clicking it again or clicking it while holding down the Ctrl key.

To deselect components, click any empty space on the schematic sheet.

Versions affected: Diamond 1.0
Fixed_1.1
Devices affected: All
CR46824

**IPExpress**

MULT module has lower bits tied low after programming LatticeECP3
A MULT module with two 36-bit inputs has a 72-bit output with the lower 18 bits tied low. This is only seen after programming a LatticeECP3 device. It does not appear in simulation.
If you are using such a MULT module, after generating the module with IPexpress, find the code for the ALU54A primitive named dsp_alu_1 and set REG_OUTPUT1_CLK=CLK0. Then generate the bitstream.

Versions affected: Diamond 2.0.1, 2.1
Fixed_2.2
Devices affected: LatticeECP3
CR59334

PLL has Fractional-N Divider of 1 instead of 0
In IPexpress, for the MachXO2 PLL module, if you enable Fractional-N Divider with a value of 0, the generated netlist actually has a value of 1 (FRACN_DIV=1).

Instead, disable Fractional-N Divider. Disabling the divider is the same as having it with a value of 0.

Versions affected: Diamond 1.2, 1.3
Fixed_1.4
Devices affected: MachXO2
CR52752

Process view is not cleared when a module is regenerated
After regenerating a module with IPexpress, the processes in the Process view are not always cleared to indicate that they need to be rerun. This happens if the module's .ipx file is not included in the project.

You can force the processes to run anyway. In the Diamond main window, choose Process > Rerun All.

You can get the Process view to update correctly by adding the module's .ipx file to the project:
1. In the File List view, right-click the implementation folder and choose Add > Existing File.
2. Browse for the customized module's .ipx file, <file_name>.ipx, and select it.
3. Click Open.

 Versions affected: Diamond 1.2, 1.3, 1.4, 2.0, 2.1, 2.2
Fixed_3.0
Devices affected: All
CR52416
Calculate button for PLL produces wrong values
In some cases, the Calculate button in the IPexpress configuration dialog box for MachXO2 PLL modules produces the wrong values. If you use the resulting module, the map process may fail.

If you see unreasonable numbers appearing in the dialog box after clicking Calculate, contact Lattice Technical Support for assistance.

Versions affected: Diamond 1.1, ispLEVER 8.1SP1
Fixed_1.2, Fixed_8.2
Devices affected: MachXO2
CR51757

Incorrect delay times for DDR modules for MachXO2
The software has incorrect delay times for the DDR module for MachXO2.

Contact Lattice technical support for a software patch.

Versions affected: ispLEVER 8.1SP1, Diamond 1.1
Fixed_1.2, Fixed_8.2
Devices affected: MachXO2
CR51728

Simulation

Fails on missing GENERIC statement in OSCH
Simulation can fail because an OSCH oscillator primitive is missing the required GENERIC statement. This can happen with the Post-Synthesis generated VHDL (.vhm) files of Synplify Pro.

If you see this problem, open the .vhm file with a text editor and search for “COMPONENT OSCH”. Manually insert the GENERIC statement. The OSCH declaration should resemble Figure 1 on page 9.

 Versions affected: Diamond 2.1, 3.4, 3.4.1
 Devices affected: MachXO2, MachXO3L, Platform Manager 2
 CR123547

Simulation fails on incorrect PMI headers
Simulation can fail because Synplify Pro’s Post-Synthesis generated VHDL (.vhm) file has the PMI header incorrectly written as:

```vhdl
library pmi;
use pmi.pmi_components.all;
```
If you see this problem, open the .vhm file with a text editor and change the two lines to:

```
library pmi_work;
use work.pmi_components.all;
```

Versions affected: Diamond 2.1, 3.4, 3.4.1
Devices affected: All
CR123546

**Errors occur in ecp5um_serdes.ibs file at some pin declarations**

The ecp5um_serdes.ibs file contains some pin names that exceed the 5-character maximum, and will therefore cause errors.

Pin strings "prvlp_t" and "prvln_t" are too long, and will be truncated to five characters, causing errors.

As a workaround, rename the pins with names that are five characters or less and that do not conflict with other pin names. For example, change "prvlp_t" to "prp_t", and change "prvln_t" to "prn_t".

Versions affected: Diamond 3.2
Fixed_3.3
Devices affected: All
CR120315
The MachXO2 SEDFA simulation model does not contain timing requirements for the signal SEDFRCERR

The MachXO2 SEDFA simulation model does not contain timing requirements for the signal SEDFRCERR.

Refer to the latest version of Lattice Technical Note TN1206 for the correct timing requirements.

Versions affected: Diamond 2.1, 2.2, 3.0
Fixed_3.1
Device affected: MachXO2
CR58746

Active-HDL LEII allows only one design to be simulated at a time even with a multi-seat license

Only one instance of a Verilog design and one instance of a VHDL design can be simulated (using asim/vsim or Initialize Simulation) when using Active-HDL LEII (whether GUI-mode avhdl, or batch-mode vsimsa) on the same machine with a multi-seat floating license.

If you attempt to simulate more than one Verilog design and one VHDL design with Active-HDL LEII, you will receive the following error message:

# ELBREAD: Error: You do not have a valid license to simulate Verilog (or VHDL) module <top_module_name>.
# Contact Aldec for ordering information - sales@aldec.com.
# ELBREAD: Error: Elaboration process completed with errors.

Also, Active-HDL LEII will not start if you open a third instance of Active-HDL LEII (combined avhdl and/or vsimsa). If you attempt to start the tool with a third instance of Active-HDL LEII, you will receive the following error message:

VSIM: Error: You do not have a valid license to run more than 2 instances of Active-HDL (or VSimSA) simultaneously. Contact sales@aldec.com.

A software patch is available upon request.

Versions affected: Diamond 2.0
Fixed_2.0.1
Devices affected: All
CR57501
Simulation Wizard ignores RTL file modifications that change the top-level
If you create a simulation project file (.spf) with the Simulation Wizard; and you then run Active-HDL; and you then close Active-HDL; and you then modify an RTL file that changes the top-level; and you then double-click the .spf in the Diamond file list to re-start the Simulation Wizard, the Simulation Wizard will not recognize the changed top-level, but will instead still show the previous top-level.

You must refresh the Simulation Wizard to force it to recognize the changed top-level by either creating a new .spf, or by clicking the “Back” button twice and then clicking the “Next” button twice. This will cause the Simulation Wizard to re-parse the files and select the correct top-level.

Versions affected: Diamond 2.0, 2.0.1, 2.1
Fixed_2.2
Devices affected: All
CR56955

VHDL package files are not sent to the simulator from Simulation Wizard in some cases
When running a gate-level or timing simulation from Simulation Wizard, any VHDL package files need by simulation only files (such as test benches) are not sent to the simulator. However, all package files are sent correctly for RTL simulations.

Versions affected: Diamond 1.4
Fixed_2.0
Devices affected: All
CR54696

Active-HDL 8.2 may issue compilation warnings after using Simulation Wizard
The Aldec Active-HDL 8.2 OEM simulator may issue a compile warning in designs exported from Diamond 1.3 Simulation Wizard.

The warning states that one or more files are out of date and need to be compiled. The warning asks, “Would you like to compile them and restart the simulation?”

If you click Yes, the Aldec simulator recompiles the indicated files. Depending on the exact file compilation order, this warning may appear multiple times requiring multiple compilations. However, since this is only a warning, you can click No. The simulation will then initialize and run correctly.

To avoid this issue if it happens, in the Diamond File List view, you can manually adjust the file list to reflect the correct compilation order. This will then be passed to the simulator and avoid any warnings. Alternately, the file
order can be adjusted in the Simulation Wizard “Add and Reorder Source” step.

Versions affected: Diamond 1.3
Fixed_1.4
Devices affected: All
CR53986

Aldec Active-HDL may return error when .sdf file is located in simulation project folder
If your simulation directory is the same as your Diamond project directory, and you initialize and run a simulation in Adlec Active-HDL, the Adlec tool may return an “SDF:Error” message.

This is a known issue with Adlec Active-HDL.
If this occurs, you can edit your <project_name>.adf file as follows:
1. Find the line that begins with “1=”. For example:
   1=src/ecp3_ecp3_vo.sdf|/I2C, Maximal, Yes
2. Remove “src\” so that the line is changed to:
   1=ecp3_ecp3_vo.sdf|/I2C, Maximal, Yes

Versions affected: Diamond 1.3, 1.4
Fixed_2.0
Devices affected: All
CR53527

Verilog front-end simulation module compilation fails using Adlec Active-HDL
It was found in one case when compiling Verilog front-end simulation modules for Active-HDL from RTL that a compilation failed due to a coding error. In rare cases, you may experience this issue when using Active-HDL in the Diamond 1.2 environment for front-end simulation.

To avoid this issue, please observe the following two examples given below that illustrate improper and proper Verilog code usage and adhere to its guidelines so you can adjust your Verilog code accordingly.

Verilog Code Example #1
Please be aware that there is a restriction with the use of named generate blocks. You cannot use the block name with an index that is a variable. It has to be a literal integer. Observe the coding violation being employed in the block below in the form of a variable:

genvar i;

generate for(i=0;i<8;i=i+1) begin : gl
reg [17:0] inpipe;

if(i==0) begin
  always @(posedge clk) begin
    inpipe <= in;
  end
end else begin
  always @(posedge clk) begin
    inpipe <= g1[i-1].inpipe;
  end
end
endgenerate

**Verilog Code Example #2**
The following code replaces the block above and works fine. You will notice in the code expands the indexed block name (that is, it replaces the variable with all its possible values).

genvar i;

generate for(i=0;i<8;i=i+1) begin : g1
  reg [17:0] inpipe;

  always @(posedge clk) begin
    case (i)
      0 : inpipe <= in;
      1 : inpipe <= g1[0].inpipe;
      2 : inpipe <= g1[1].inpipe;
      3 : inpipe <= g1[2].inpipe;
      4 : inpipe <= g1[3].inpipe;
      5 : inpipe <= g1[4].inpipe;
      6 : inpipe <= g1[5].inpipe;
      7 : inpipe <= g1[6].inpipe;
    endcase
  end
end
endgenerate

Versions affected: Diamond 1.2, 1.3, 1.4
Fixed_2.0
Devices affected: All
CR52245

**After upgrade, Active-HDL cannot open configuration**
After upgrading to Diamond 1.1 in Windows, designs fail to simulate with Aldec Active-HDL Lattice Edition. The Active-HDL log shows:

```
?# Design: Error: Cannot open configuration: ""
```
The problem is that the Registry key for Active-HDL is still pointing to Diamond 1.0, which was deleted before installing the upgrade. The solution is to edit the Registry.

Editing the Registry must be done carefully. It is possible to make an unrepairable mistake. If you are not comfortable with editing the Registry, please contact your information technology (IT) department for help.

To correct the Active-HDL Registry key:
1. Close Active-HDL.
2. In the Windows Start menu, click Run.
3. In the Run dialog box, enter regedit.
4. Click OK.
   Registry Editor opens.
5. In the folder tree in the left pane, open HKEY_CURRENT_USER\Software\Aldec, Inc.\Active-HDL 8.2.
   Be sure that you are in the HKEY_CURRENT_USER folder. There is a similar path under HKEY_LOCAL_MACHINE, but changing it will corrupt the Active-HDL installation, requiring that you re-install Diamond.
6. Under HKEY_CURRENT_USER\Software\Aldec, Inc.\Active-HDL 8.2, select LatticeEditionII.
7. Press Delete.
8. Close Registry Editor.

You should be able to run simulations now.

Versions affected: Diamond 1.1
   Fixed_1.2
   Devices affected: All
   CR51766

On Windows 7 when launching the Simulation Project File (SPF) in Diamond, the Simulation Wizard’s Add Source page does not update properly
On Windows 7, when you double-click on the Simulation Project File (SPF) in the File List's Script Files folder, the Simulation Wizard's Add Source page does not update properly, still showing a list with no selected criteria for source.

In the Simulation Wizard, click the Back button to go to first page in the wizard and then click Forward to the Add Source page to allow the program to refresh.
Preference Views

Spreadsheet View takes a long time to open
For large projects, it might take a minute or longer for Spreadsheet View to open. This is because of the time needed for real-time PIO design rule checking as the design is loaded.

Versions affected: Diamond 2.0 and later
Devices affected: All
CR56872

There is no DRC check on the Clock Jitter value entered
Currently there is no check on the jitter value entered. It can be more than the given clock period but no error is generated.

Versions affected: Diamond 1.3, 1.4, 2.0., 2.1, 2.2
Fixed_3.0
Devices affected: All
CR53669

Global preference sheet erroneously shows "DISABLE" for MASTER_SPI_PORT
If your design includes both master and slave SPI configurations, the Global preference sheet might show DISABLE as the default preference value for MASTER_SPI_PORT. The correct default value should be EFB_USER. To work around this issue, select either EFB_USER or ENABLE from the drop-down menu.

Version affected: Diamond 1.2
Fixed_1.3
Devices affect: MachXO2
CR52675
PAR-assigned pins cannot be cross-probed from Spreadsheet View
In Spreadsheet View, the “Show In” commands are not enabled for pins that were assigned by the Place & Route process. Only ports assigned to pins by LOCATE preferences can be cross-probed with the “Show In” command in Spreadsheet View. The “Show In” commands are available, however, from Package View for pins assigned by Place & Route.

Versions affected: Diamond 1.0
Fixed_1.1
Devices affected: All
CR50328

Selected nets in NCD View do not get added to the Create New UGROUP dialog box
When you right-click one or more selected nets from the Nets tree in NCD View, you are able to access the “Set UGROUP Preference” command. The selected nets in NCD View are used to identify the set of NCD components into which the NGD components are packed. Only PFU, PFF, EBR, or DSP types of NGD components can be included in a UGROUP. Based on the selected net, any of these types of NGD components that are connected to the selected net will appear in the Selected Instances list of the dialog box. If no appropriate instances for a UGROUP are connected to the selected nets, the Selected Instances list will be empty. The nets are never added to this list.

Versions affected: Diamond 1.0
Fixed_1.1
Devices affected: All
CR50287

Selected nets in Netlist View do not get added to the Create New UGROUP dialog box
When you right-click one or more selected nets from the Nets tree in Netlist View, you are able to access the “Set UGROUP Preference” command. This command opens the “Create New UGROUP” dialog box. Only PFU, PFF, EBR, or DSP types of NGD components can be included in a UGROUP. Based on the selected net, any of these types of NGD components that are connected to the selected net will appear in the Selected Instances list of the dialog box. If no appropriate instances for a UGROUP are connected to the selected nets, the Selected Instances list will be empty. The nets are never added to this list.

Versions affected: Diamond 1.0
Fixed_1.1
Devices affected: All
CR50286
Regions and groups in Physical View are not displayed in the colors assigned to them
Physical View displays only fixed colors for different elements such as regions, groups, sites, and delay paths. It does not support customized color settings. Therefore, the borders of all regions and groups are displayed in the same default color on the layout. They are not displayed in the colors that were assigned to them.

To view regions and groups in their assigned colors on the layout, open Floorplan View.

Versions affected: All
Devices affected: All
CR50166

Physical View does not match delay path colors or allow custom colors
Physical View displays only fixed colors for different elements such as delay paths, regions, groups, and sites. Therefore, when you cross-probe a delay path from Timing Analysis View, Physical View highlights the path in the same default color. It does not show the path color that is displayed in Timing Analysis View or allow you to manually change the color. Currently there is no way to distinguish the color of individual delay paths in Physical View. However, if you cross-probe to Floorplan View from Timing Analysis View, you will see the delay paths distinguished by color.

Versions affected: All
Devices affected: All
CR47031, CR49201

Synthesis

LSE fails on IP for Platform Manager 2
Synthesis with Lattice Synthesis Engine (LSE) fails on IP in the design. This can happen when the IP is specifically for Platform Manager 2, such as DualBoot, ViD, and Fault Logger.

If you see this problem, try using the Synplify Pro synthesis tool.

Versions affected: Diamond 3.4, 3.4.1
Devices affected: Platform Manager 2
CR123572
LSE does not process input_delay and output_delay constraints properly
In some cases, when input_delay or output_delay SDC constraints are used in Lattice Synthesis Engine (LSE), LSE crashes.

Do not use these constraints in SDC. Instead, use the equivalent LPF constraints such as INPUT_SETUP and CLOCK_TO_OUT.

Versions affected: Diamond 2.1
Fixed_3.4
Devices affected: All
CR123349

Synthesis fails with schematic file on Windows 8
Diamond does not support the Windows 8 operating system. Synthesizing a design with a schematic file fails with error code 1.

Run Diamond on a different operating system.

Versions affected: All
Fixed_3.3
Devices affected: All
CR118394

Design with DDR_GENERIC fails in synthesis
Designs using the DDR_GENERIC module from IPexpress may fail during synthesis. This can happen if the module was generated with VHDL output using 64-bit Lattice Diamond on Windows. If you look at the VHDL code for the DDR_GENERIC module, you will see various attributes set to incorrect characters, which is the cause of the synthesis failure.

If you see this problem, contact Lattice customer support for a patch.

Versions affected: Windows 64-bit Diamond 2.0
Fixed_2.0.1
Devices affected: All
CR57781

Defaults in Diamond strategies are different from Synplify Pro itself
The default settings for Synplify Pro in the Diamond options are not always the same as the default settings built into Synplify Pro itself. If you run Synplify Pro in interactive mode (from the Diamond Tools menu) or by command line, check that the settings are correct to ensure that the results do not differ. In interactive mode, Synplify Pro does not use the Diamond strategy settings. Instead you have full, direct use of the Synplify Pro controls.
LATTICE DIAMOND: Synthesis

 Versions affected: Diamond 2.0, 2.0.1
 Fixed_2.1
 Devices affected: All
 CR56755

 LSE does not convert gated clocks driving distributed RAM primitives
 Lattice Synthesis Engine (LSE) does not perform gated clock conversion for gated clocks driving distributed RAM primitives such as DPR16X4C and SPR16X4C.

 Versions affected: Diamond 2.0, 2.0.1
 Fixed_2.1
 Devices affected: MachXO, MachXO2, Platform Manager
 CR56264

 Synplify Pro for Lattice fails to produce _prepass.srd file
 Sometimes Synplify Pro for Lattice fails with error code 2. The log shows that a file with a long name ending in "_prepass.srd" does not exist.

 The problem may be the length of the path names for the project's source files. Windows has a limit on how long path names can be. Try reducing the path names, especially the source file names.

 Versions affected: Diamond 1.0, 1.1, 1.2, 1.3, 1.3.1, 1.4, 1.4.1, 1.4.2, 2.0, 2.0.1, 2.1, 2.2
 Fixed_3.0
 Devices affected: All
 CR52736

 After synthesis with Synplify Pro, port or net names are changed
 After synthesizing a design with Synplify Pro, you sometimes find that the name of a port or net has changed unexpectedly.

 This can happen if the syn_keep directive is mistakenly applied to a port. The syn_keep directive can only be applied to nets but Synplify Pro does not issue an error message if the directive is incorrectly used.

 Versions affected: Diamond 1.2
 Fixed_1.3
 Devices affected: All
 CR52423
Synthesis warns that EBR CSDECODE property should be binary
The Synthesize Design process sometimes gives a warning such as this:

@W:BN283 : sdi_gamma_in_tbl_22.vhd(295) | Expect property csdecode_a of instance sdi Gamma in tbl_22_0_0_0 to be binary, but 0b000 is seen.

The message says the property is not binary but shows that it is. This can happen when using Synplify Pro for Lattice. There is actually no problem with the design. This warning can be ignored.

 Versions affected: Diamond 1.0, 1.1, 1.2, 1.3
 Fixed_1.4
 Devices affected: All
 CR51814, CR53812

The last EDIF source in the source file list is automatically treated as the top module
If you have a pure EDIF design, after processing the design, the last EDIF source is automatically treated as the top module.

Before processing a pure EDIF design, you need to rearrange the source file order to put the top EDIF module to the last of the source file list.

 Versions affected: Diamond 1.0
 Devices affected: All

Implementation Flow
PAR TRACE Report does not include frequency tolerance
The built-in oscillator of MachXO2 has a 5% frequency tolerance. But the Place & Route TRACE Report is only calculated for the nominal value.

To be sure that the design will work with the frequency variation, use the next higher available frequency in the FREQUENCY preference in the Lattice preference file (.lpf). For the frequency, see TN1199, “MachXO2 sysCLOCK PLL Design and Usage Guide,” Table 13-15, “OSCH Supported Frequency Settings.”

For example, if the nominal frequency is 53.2 MHz, the preference should be:

FREQUENCY NET "osc_clk" 66.50 MHz ;

 Versions affected: Diamond 3.2 and earlier
 Fixed_3.3
 Devices affected: MachXO2
 CR123062
Diamond crashes during Translate Design after setting constraints with Spreadsheet View
On Windows, Diamond sometimes crashes during the Translate Design stage after setting constraints with Spreadsheet View. This can happen if you are using a language setting, such as German, that uses commas (,) as decimal points.

To avoid this problem, change your operating system to use periods instead of commas as decimal points. The following instructions are for Windows 7:

1. In the Windows Start menu, click Control Panel.
2. In the Control Panel, click Region and Language.
   The Region and Language dialog box opens.
3. In the Format tab, click Additional settings.
   The Customize Format dialog box opens.
4. Find “Decimal symbol” and choose “.” (period).
5. Click OK.
6. In the Region and Language dialog box, click OK.
7. Close the Control Panel.
8. Restart Diamond.

Versions affected: Diamond 2.1
Fixed_2.2
Devices affected: All
CR59584

PAR report shows placement score values that vary greatly between phases
The EFB (Embedded Function Blocks) module for MachXO2 UHC devices shows the wrong number of user flash memory (UFM) pages. So IPexpress cannot access all of the pages in the device.

There is no workaround for this issue.

Versions affected: Diamond 1.2, 1.3, 1.3.1, 1.4, 1.4.1, 1.4.2, 2.0, 2.0.1, 2.1
Fixed_2.2
Devices affected: MachXO2 UHC
CR59398

PAR report shows placement score values that vary greatly between phases
In the place and route report (*.par), any LatticeECP3 placement will report a different score value compared to previous releases. For example, the par file might have the following message:
Starting Placer Phase 1.

Placer score = 42182813.
Finished Placer Phase 1. REAL time: 5 mins 29 secs

Starting Placer Phase 2.

Placer score = 574428473
Finished Placer Phase 2. REAL time: 7 mins 9 secs

The score (574428473) after phase 2 is much bigger than the score (4218281) in phase 1. This is normal and does not mean that the score after phase 2 becomes worse. Because “Placer score” is a weighted combination of different placement merits, the placer in Phase 2 uses a different weighted formula than that used in phase 1.

Note: This only happens with LatticeECP3 devices. For other device families, the scores in both phase 1 and 2 use the same weighted formula.

Versions affected: Diamond 2.1
Fixed_2.2
Devices affected: LatticeECP3
CR59260

**PAR report does not show placement results sorted by timing score**

When “Generate TRACE report for each iteration” has been enabled in the active strategy, the Place & Route report will show placement results sorted by “Worst Slack,” even when the “Timing Score” option has been selected for “Placement Sort Best Run.”

Versions affected: Diamond 2.1, 2.2, 3.0
Devices affected: All
CR59212

**Preference semantic errors reported during design implementation**

In the design implementation flow, preference parsing will sometimes generate semantic error warnings for PGROUPs.

These warning messages can be ignored, since the preference is still honored by Place & Route, and the implementation results are not impacted.

Versions affected: Diamond 2.1
Fixed_2.2
Implementation succeeds despite missing EDIF source file

If you remove or exclude an EDIF source file, implementation of the design might still succeed despite the missing file. This can happen if you ran implementation through the Map Design stage before removing or excluding the EDIF file and did not make any other changes to the design. The project still has the generated files to work with and does not recognize a need to unlink the .ngo file just because the EDIF file has been removed or excluded.

If this is a problem for you, remove the .ngo file manually.

Versions affected: Diamond 2.1, 2.2
Fixed_3.0
Devices affected: All
CR58533

PAR may fail to place PIO PGROUP if clock PIO driver is assigned to the same bank

For LatticeECP3 devices, if a design has:

- PIO driven primary or secondary clock;
- PIO PGROUP located to an I/O bank; and
- clock PIO driver that requires a different Vccio than that of the PIOs in the PGROUP,

then there's a chance PAR will fail to place the PIO PGROUP if the clock PIO driver is assigned to the same bank as this PGROUP.

As a workaround, manually lock the clock PIO driver to a different I/O bank.

Versions affected: Diamond 1.3
Fixed_1.4
Devices affected: LatticeECP3
CR53999

Map says to set SHAREDEBRINIT=ENABLE but it already is

The Map Design process recommends setting SHAREDEBRINIT=ENABLE for the EBR INIT value sharing but it is already set to ENABLE. The message is:

INFO - map: Please set SHAREDEBRINIT=ENABLE with SYSCONFIG preference in LPF file and map again to compress all unique EBR patterns.
You can ignore this message if the sharing INIT value for the EBRs is caused by using INIT_DATA=DYNAMIC.

versions affected: Diamond 1.3
Fixed_1.4
Devices affected: MachXO2
CR53998

If more than one EBR has the same INIT, data will be shared if at least one EBR sets INIT_DATA to STATIC and others to INIT_DATA=DYNAMIC

If more than one EBR has the same INIT, data will be shared if at least one EBR sets INIT_DATA to STATIC and others to INIT_DATA=DYNAMIC.

As a workaround, set INIT_DATA to DYNAMIC for all EBRs with same INIT data. Don't mix STATIC and DYNAMIC for the INIT_DATA setting. This will ensure that all EBRs with same INIT data will not be shared.

versions affected: Diamond 1.3
Fixed_1.4
Devices affected: MachXO2
CR53997

Map says WISHBONE clock frequency of EFB module can be up to 166 MHz

For the WISHBONE clock frequency of the EFB (Embedded Function Block) module, the Map Design process allows frequencies of up to 166 MHz. This is an error. Legal values are no more than 133 MHz.

versions affected: Diamond 1.3
Fixed_1.4
Devices affected: MachXO2
CR53897

Map changes DEV_DENSITY incorrectly for U devices

The Map Design process issues a message such as the following while using an UHC device:

WARNING - map: SED device density parameter '2000L' does not match that of the selected device. Software has changed the DEV_DENSITY value to '640L' to match the device that is used in this project.

However the new DEV_DENSITY value is for a non-UHC device.
This can happen with a design using the EFB (Embedded Function Block) module.

If this happens, use IPexpress to regenerate the EFB module.

Versions affected: Diamond 1.3, 1.4
Fixed_2.0
Devices affected: MachXO2
CR53801

**IO Timing Report and Trace Report numbers do not match when using SS on INPUT_SETUP**

When using the “SS” key on INPUT_SETUP, Trace Report will ignore CLOCK_JITTER and show setup and hold numbers without CLOCK_JITTER. IO Timing Report currently does not read the “SS” key on the INPUT_SETUP preference and hence will show setup and hold numbers that include the CLOCK_JITTER

Versions affected: Diamond 1.3, 1.4, 2.0, 2.1, 2.2
Fixed_3.0
Devices affected: All
CR53605

**MachXO2 design issues PAR warnings for PLL clocks that do not match their divider settings**

In a MachXO2 design in the Diamond 1.1 release, a user created a design in VHDL that used a PLL in the module “ricevitore”. In the PAR report there appeared repeated warnings that the CLKOP and CLKOS frequencies did not match divider settings for the PLL as shown in the example below:

```
WARNING - par: Output clock frequencies on pin CLKOP and CLKOS do not match their divider settings for
inst_ricevitore/inst_RX_pll/PLLInst_0
WARNING - par: Output clock frequencies on pin CLKOP and CLKOS do not match their divider settings for
inst_ricevitore/inst_RX_pll/PLLInst_0
WARNING - par: Output clock frequencies on pin CLKOP and CLKOS do not match their divider settings for
inst_ricevitore/inst_RX_pll/PLLInst_0
```

The warnings were caused by an inconsistency in the CLKOS setting. The design has a consistent frequency setting; however, when the LPF and resulting PRF was changed to 14 MHz from 13.3 MHz, a condition for triggering the warning was created.

Please be aware that this condition exists and the warning message now includes the signals in the preference as shown below in the example for troubleshooting. Also, the warning message will be issued only once per trace instance.
WARNING - trce: The Preference FREQUENCY NET at signal inst_ricevitore_clk_100_c (CLKOP) or signal clk_received_c (CLKOS) do not match their divider settings for inst_ricevitore/inst_RX_pll/PLLInst_0

Versions affected: Diamond 1.1, 1.2
Fixed_1.3
Devices affected: MachXO2
CR52734

TRACE reports errant clock speed that exceeds target specifications for GDDRX1 designs
Sometimes TRACE timing analysis reports that a MachXO2 design containing a GDDRX1 interface could run at clock speeds approaching 285 MHz. But device target specifications state that the maximum clock frequency is 150 MHz (FDDRX1). The report is not correct. Below is an example of the clock speed issued in the TRACE report:

<table>
<thead>
<tr>
<th>Preference</th>
<th>Constraint</th>
<th>Actual</th>
<th>Levels</th>
</tr>
</thead>
</table>
| FREQUENCY PORT "clk" 285.000000 MHz | 285.000 MHz | 284.091 MHz | 1 *

When using the DDR interfaces, refer to data sheets and other documentation on the Lattice Web site to guide your target design constraints or contact customer support. Hardware model timing data will be addressed to accurately reflect these specifications.

Versions affected: Diamond 1.1, 1.2
Fixed_1.3
Devices affected: MachXO2
CR52704

Default PCICLAMP setting in Spreadsheet View produces illegal combination error
In Spreadsheet View, default values are displayed in blue font when Show Default Values has been selected from the View menu. For some IOBUF attribute combinations, the default PCICLAMP setting of ON does not get adopted properly. Consequently, the PIO DRC check reads the setting as OFF and issues an illegal combination error. The design will then fail when you run Place & Route.

To resolve this error, manually select ON in the PCICLAMP column for the identified iobuffer. Spreadsheet View will then show the ON value in black font, indicating a user setting, and it will add the setting to the IOBUF preference.
LATTICE DIAMOND : Implementation Flow

 Versions affected: Diamond 1.0, 1.1, 1.2
 Fixed_1.3
 Devices affected: All
 CR52666

Configuration data not fully loaded into EBR from UFM

With MachXO2-1200, you sometimes find that the configuration data has not fully loaded into the Embedded Block RAM (EBR) from the User Flash Memory (UFM). This is because the last page of the UFM cannot be used. If configuration data is loaded to it, the EBR will not be fully initialized.

So only six unique initial patterns can be loaded into the EBR. The seventh EBR cannot be used.

More generally, to avoid the last page of the UFM, reconfigure the EFB module to use one extra page, forcing everything to load before the last page. For example, suppose you have 100 pages of data. In the EFB configuration dialog box of IPexpress, go to the UFM tab and enter 101. The data will then start at page 411 instead of 412, leaving the last page empty.

 Versions affected: Diamond 1.1.01, 1.2
 Fixed_1.3
 Devices affected: MachXO2-1200
 CR52661

Components within a wide LUT have different PGROUP settings

Sometimes during the Map Design process, you may get an error message referring to L6MUX21 or PFUMX having a PGROUP setting different from other components in a “wide LUT.” For example:

ERROR: One or more components in the wide LUT rooted at L6MUX21 \lpc_peripheral_inst0/lpc_data_out_2_m0_d_d_0_d_3/GATE has a PGROUP setting which differs from the PGROUP settings of other components within the wide LUT. All components within a wide LUT must have the same PGROUP settings.

This can be caused by the L6MUX21 and PFUMX primitives being in different hierarchies, and both hierarchies having different UGROUP constraints.

If you see this problem, either change the UGROUP constraints to put both hierarchies in the same group or put a "syn_hier=firm" directive on one or both hierarchies in the synthesis constraints file.

 Versions affected: Diamond 1.1, 1.2, 1.3, 1.3.1, 1.4, 1.4.1, 1.4.2, 2.0, 2.0.1, 2.1, 2.2
 Fixed_3.0
Devices affected: All
CR52579

**Map Design fails on Linux 64-bit Red Hat 4 machine**
The Map Design process sometimes reports “error waiting for process to exit” on a Linux machine that runs Red Hat Enterprise Linux WS release 4 (Nahant Update 2) with kernel release 2.6.9-22.EL. This is caused when the process-wait API fails to get the return status.

Although you may be able to ignore this error safely and continue with the flow, Lattice recommends that the best solution is to update the Redhat 4 kernel to a higher version.

Versions affected: Diamond 1.2, 1.3, 1.3.1, 1.4, 1.4.1, 1.4.2, 2.0, 2.0.1, 2.1, 2.2
Fixed_3.0
Devices affected: LatticeECP, LatticeECP2, LatticeECP2S, LatticeXP, LatticeSC, LatticeSCM
CR52155

**Design fails in Translate Design with errors about undefined modules or cannot open file**
Sometimes, what seems to be a perfectly good design fails in the Translate Design stage with errors about undefined modules or being unable to open input files. This happens when you are using Synplify Pro for Lattice as the synthesis tool.

Check the full pathname to the project’s folder. Look for a space followed by a dash, as in “/WI -P/demo.ldf”. If you see the space-dash combination, try changing the pathname to eliminate the space or the dash character. For example, “/WI-P/demo.ldf” or “/WI P/demo.ldf” should work.

Versions affected: Diamond 1.1, 1.2, 1.3
Fixed_1.4
Devices affected: All
CR52036, CR52198

**Slave Chip Select pins of MachXO2 are not reserved**
Software does not reserve two Slave Chip Select pins when you use the Slave SPI port of the Embedded Functional Block (EFB) of MachXO2. The two Slave Chip Select pins are used in the device for the following two functions:

- Chip Select for Slave SPI Configuration
- Chip Select for the Hardened Slave SPI IP in the EFB module
If you have this situation, set aside the configuration Slave Chip Select pin and do not use it as a general purpose I/O.

Versions affected: Diamond 1.1, ispLEVER 8.1SP1
Fixed_1.2, Fixed_8.2
Devices affected: MachXO2
CR51903

Map does not report an error condition for MULTICYCLE constraint containing net with invalid name

In one case PAR and TRACE reported semantic errors when the LPF preference file input into Map contained an invalid net name in a FREQUENCY constraint. When the same net causing the error condition was also used in a MULTICYCLE constraint in the same LPF file, it was not being reported.

For example, in this case the constraints were as follows and the net in question was called “tx_clk_187m_c”.

FREQUENCY NET “tx_clk_187m_c” 187.000000 MHz ;
MULTICYCLE FROM CLKNET “tx_clk_187m_c” CLKEN_NET “tx_clken_94m” TO CLKNET “tx_clk_187m_c” 2.000000 X ;

In this scenario, both preferences should have generated an error, not just the FREQUENCY preference and it should have been detected and reported in the Map stage, prior to PAR and TRACE. So, currently, the MULTICYCLE preference containing an invalid net name will not be flagged as an error in the user flow.

This type of case may be rare and not be encountered very often by a user. It is typically caused when you re-synthesize your design and component name changes take place and you presume your preference definitions are still viable.

To avoid this issue, Lattice recommend that you check both the Map Report and the TRACE report for the results you would expect to occur in your design to validate your preference designations.

Versions affected: Diamond 1.2, 1.3, 1.3.1, 1.4, 1.4.1, 1.4.2, 2.0
Fixed_2.0.1
Devices affected: All
CR51777

“Invalid LPF_RESISTOR value” error from MAP process

In some cases, a MachXO2 PLL module causes the map process to fail with the following error:
LATTICE DIAMOND : Implementation Flow

EHXPLLJ '<instance_name>' has invalid LPF_RESISTOR value <number>. Valid values are 0 to 63.

Contact Lattice Technical Support for assistance.

Versions affected: Diamond 1.1, ispLEVER 8.1SP1
Fixed_1.2, Fixed_8.2
Devices affected: MachXO2
CR51758

CONFIG_SECURE attribute in VHDL gets ignored by PAR

When you use the CONFIG_SECURE attribute in the VHDL source file (CONFIG_SECURE=ON), the string gets converted to lower case by Synplify Pro during synthesis. The lower-case version of this attribute is not recognized by Place & Route, which causes it to be ignored.

To avoid this error, add the following preference to the logical preference file before mapping:

```
SYSCONFIG CONFIG_SECURE=ON ;
```

The preference will override the attribute in the VHDL.

Versions affected: Diamond 1.0, 1.1, 1.2; ispLEVER 8.1, 8.1 SP1
Fixed_1.3
Devices affected: All
CR51593

Error message for MCCLK preference

Spreadsheet View's Global preference sheet allows you to select an MCCLK frequency of 33 MHz for LatticeECP3 devices. The LatticeECP3 master configuration clock (MCCLK) frequency is limited in hardware to 33 MHz maximum. However, the software erroneously produces an error for a frequency selection equal to or greater than 30.

Versions affected: Diamond 1.1
Fixed_1.2
Devices affected: LatticeECP3
CR50679
Timing Analysis

Unconstrained-path sequence causes cross-probing error in Timing Analysis View
In Timing Analysis View, the unconstrained-path sequence might be different from the sequence of the unconstrained paths in the timing report. This can cause a problem when cross-probing a path from Timing Analysis View to the timing report.

Versions affected: Diamond 2.0, 2.0.1
Fixed_2.1
Devices affected: All
CR57219

In Linux, a memory fault error occurs when exiting Diamond right after closing Timing Analysis view
When you open the Diamond user interface, open Timing Analysis view, close the view, and then exit the program, it produces a memory fault error.

There is no current workaround for this issue.

Versions affected: Diamond 1.0
Fixed_1.1
Devices affected: All
CR50360

When cross-probing a timing path from the Timing Analysis view's Path Table to a report, it fails to display the corresponding path
In some cases where a user has selected a path in the Timing Analysis view for cross probing the Report view, the path cross-probed in the report does not match.

In the timing report, manually search for the correct path that corresponds to the one in the Path Table. To search in the report, right-click in the report and choose Find text. In the Find dialog enter some search criteria and click Find Next.

Versions affected: Diamond 1.0
Fixed_1.1
Devices affected: All
CR50316
In Timing Analysis view, unnecessary PGROUP preferences found in the TPF file result in warning messages

When a TPF file that is produced from a PRF file that contains grouping preferences (such as PGROUP) is run in the Timing Analysis view, Diamond may issue unwanted warning messages. When it finds these preferences the Timing Analysis view generates warnings and then disables the preferences.

For example, you might encounter warnings in the Output pane’s Warning tab similar to the following test case:

WARNING - C:/bugs/50186/npt2/start2.tpf.prf (34): Error in PGROUP "insideh" BBOX 7 8 DEVSIZE
COMP "inside_inst/SLICE_4"
COMP "inside_inst/SLICE_10"
COMP "inside_inst/SLICE_11"
COMP "inside_inst/SLICE_12"
COMP "inside_inst/SLICE_13"
COMP "inside_inst/SLICE_14"
COMP "inside_inst/SLICE_15"
COMP "inside_inst/SLICE_16"
COMP "inside_inst/SLICE_17"
COMP "inside_inst/SLICE_18"
COMP "inside_inst/SLICE_19"
COMP "inside_inst/SLICE_20"
COMP "inside_inst/SLICE_21"
COMP "inside_inst/SLICE_22"
COMP "inside_inst/SLICE_23"
COMP "inside_inst/SLICE_24"
COMP "inside_inst/SLICE_25"
COMP "inside_inst/SLICE_26";
: This comp does not exist in the design: inside_inst/SLICE_4.. Disabled this preference.
WARNING - C:/bugs/50186/npt2/start2.tpf.prf (35): Error in LOCATE PGROUP "insideh" SITE "R14C2D";
: PGROUP "insideh" has not been defined.. Disabled this preference.
WARNING - Preference parsing results: 2 semantic errors detected

These warnings can be safely ignored and will not affect output TPF files or analysis since Timing Analysis view does not use them. They can be regarded as “don’t care” elements in the file.

Versions affected: Diamond 1.0
Fixed_1.1
Devices affected: All
CR50186
The Timing Analysis view does not display a path in the view that should appear in the Path Table

When the first critical f\textsubscript{MAX} path occurs at the minimum pulse width and there is only one additional path, only the minimum pulse width path shows in the Timing Analysis view's Path Table, even if the number of timing paths to show is greater than two.

The missing path in the Path Table can be found in the timing report. Use the Find dialog box by right-clicking in the report and choosing Find text.

Versions affected: Diamond 1.0
Fixed_1.1
Devices affected: All
CR50169

Power Calculator

Power Calculator “Catch unknown exception” error causes Diamond to hang

When designing with the LatticeXP2-5E device and running Power Calculator, you will receive the error message "Catch unknown exception: Remove Power Calculator from Lattice Diamond." After you click OK, the Diamond software will freeze up.

When you get this error message, contact Lattice Technical Support.

Versions affected: Diamond 2.0, 2.0.1 Windows 32-bit, Linux Redhat/SUSE
Fixed_2.1
Devices affected: LatticeXP2-5E
CR57764

Power Calculator shows incorrect PLL information when TWR file is used

When you use the Trace report file (TWR) to import frequency settings into Power Calculator, the information shown for PLL might not be accurate. To ensure that the frequency is set correctly for PLL clocks, enter the frequency value manually in the "Input Freq (MHz)" column on the PLL page.

Versions affected: ispLEVER 8.1, 8.1SP1; Diamond 1.0, 1.1, 1.2
Fixed_1.3, Fixed_8.2
Devices affected: All
CR52604
Routed design with SERDES shows incorrect channels in Power Calculator

When your routed design contains SERDES, Power Calculator might not extract the PCS settings if the PCS configuration files are not in the project root directory.

In most cases, you can resolve this problem by manually copying your PCS configuration files to the project root directory (the same directory as the .ldf file) before you launch Power Calculator. In Diamond, these configuration files are usually located in the project implementation directory. In some cases, this might not resolve the issue, depending on whether the directories had been changed. If copying the files does not work and you want to look at SERDES power in more detail, enter the number of channels manually in Power Calculator. This will take you out of calculation mode and into estimation mode.

Versions affected: Diamond 1.0, 1.1, 1.2
Fixed_1.3
Devices affected: LatticeECP2M, LatticeECP2MS, LatticeECP3, LatticeSC, LatticeSCM
CR52246, CR52708

Power Calculator underestimates power for some LVCMOS I/O

For MachXO2 designs with the following combinations of LVCMOS types and I/O bank VCCIO values, Power Calculator underestimates the I/O power:

LVCMOS18 Input/Bidi and VCCIO = 2.5 V
Typical static ICCIO reported: 0.0139 uA per I/O
Actual typical static ICCIO: 19.7 uA per I/O

LVCMOS18 Input/Bidi and VCCIO = 3.3 V
Typical static ICCIO reported: 0.0173 uA per I/O
Actual typical static ICCIO: 205.56 uA per I/O

LVCMOS25 Input/Bidi and VCCIO = 3.3 V
Typical static ICCIO reported: 0.0206 uA per I/O
Actual typical static ICCIO: 15.47 uA per I/O

The above values are for TJ = 25 C and inputs at logic high.

Version affected: Diamond 1.1, ispLEVER 8.1SP1
Fixed_1.2, Fixed_8.2
Devices affected: MachXO2
CR52011
Power Calculator over-estimates power for MachXO2
The Oscillator model in Power Calculator does not include all the capacitive loads that exist in MachXO2 devices. The Oscillator power dissipation in Power Calculator is lower than what is observed in these devices.

Contact Lattice Technical Support for detailed information.

Versions affected: Diamond 1.1, ispLEVER 8.1SP1
Fixed_1.2, Fixed_8.2
Devices affected: MachXO2
CR51904, CR51905

Reveal Hardware Debug

Reveal Analyzer fails to open on Windows 8
Diamond does not support the Windows 8 operating system. Reveal Analyzer fails to open.

Run Diamond on a different operating system.

Versions affected: All
Fixed_3.3
Devices affected: All
CR118978

Reveal Analyzer crashes when scanning devices
If pin 1 of the JTAG connector on the board is not connected to the VCC signal of the USB (or Parallel) download cable, Reveal Analyzer crashes when the Startup Wizard scans the devices.

VCC must be connected for Reveal Analyzer to work.

Versions affected: Diamond 2.0, 2.0.1
Fixed_2.1
Devices affected: All
CR57299

Reveal triggers wrong with 3 trigger units and Max Sequence Depth of 4
Reveal Analyzer may not trigger correctly if there are three trigger units and a maximum sequence depth of 4. If your Reveal module has three trigger units, open Reveal Inserter and set Max Sequence Depth of the trigger expression to 1, 2, 8, or 16 (not 4).
Reveal Inserter fails to link a signal

In Reveal Inserter, if you try to trace multiple dimension array signals within a VHDL design whose top entity is defined by the Configuration statement, Reveal Inserter may issue a runtime error. After you select the Ignore button of the dialog box, Reveal issues an error message in the Output view as follows:

ERROR: Failed to link signal 'keysch/round0a/m_value_even'.
ERROR: Core Linker Failed.

To avoid this problem, choose Design > Generate Hierarchy in the Diamond main window. Then launch Reveal Inserter to get the correct design tree. Regenerate the Reveal project file.

Versions affected: Diamond 1.0, 1.1, 1.2
Fixed_1.3
Devices affected: All
CR52516

Recently used platforms do not appear in the Open Platform list

Reveal Inserter might not open with a large VHDL design that has many user-defined data types. There’s no error message. You see a message about “loading design” but Reveal Inserter never opens.

The process was probably killed because it ran out of memory. You can work around this problem by synthesizing the design to create an EDIF file. Then create an EDIF design project and run Reveal Inserter.

Versions affected: ispLEVER 7.1SP1, 7.2, 7.2SP1, 7.2SP2, 8.0, 8.0SP1, 8.1, 8.1SP1; Diamond 1.0
Fixed_1.1, Fixed_8.2
Devices affected: All
CR43358

Other Topics

Hysteresis is not set for the LVTLL33 IO_TYPE

Hysteresis bits are not set for the LVTLL33 IO_TYPE. Changing the Hysteresis setting in the software will not have any effect if you select the IO_TYPE to be LVTTL33.
Change the IO_TYPE to LVCMOS33 and then use the Hysteresis settings. LVCMOS33 and LVTL33 are exactly the same.

Versions affected: Diamond 3.3
Fixed_3.4
Devices affected: MachXO2
CR122740

**EPIC Help does not display in Firefox**

EPIC cannot open its online Help if Firefox is your default browser. Instead, Firefox displays, “The address wasn’t understood.”

To work around this problem, do one of the following:

- Set a different browser, such as Chrome or Internet Explorer, as your default browser. Then open the Help from EPIC.
- In Firefox, enter the path to the Help:
  `<Diamond directory>\ispfpga\webhelp\epichelp\index.htm`

Versions affected: Diamond 3.1, 3.2, 3.3
Fixed_3.4
Devices affected: All
CR122659

**VME file missing USERCODE verification opcode**

Deployment Tool, with the Verify USERCODE option, does not include the opcode for USERCODE Verification test (case VUES = 0x61) at the beginning of the VME hex file.

Use ispVM System to generate the VME file instead.

Versions affected: Diamond 2.2, 3.0
Fixed_3.1
Devices affected: All
CR117915

**Tutorials require “Diamond Free License - For Versa Kit Only” for users of free Diamond software**

Users of free Diamond software who wish to perform either the *Diamond Tutorial* or the *LatticeMico32 Tutorial* should request the “Diamond Free License - For Versa Kit Only.” This license enables the user to select the LatticeECP3 LFE3-35EA device, which is required to perform the tutorials.

Many of the tasks in the tutorials can be performed without an actual LatticeECP3 Versa Development Kit, but the low-cost LatticeECP3 Versa Development Kit is recommended to perform all of the tasks in the tutorials.
To obtain a “Diamond Free License - For Versa Kit Only,” go to www.latticesemi.com and chose Support > Licensing.

To purchase a low-cost LatticeECP3 Versa Development Kit, go to www.latticesemi.com and chose Products > Development Hardware > Development Boards and Kits.

Versions affected: Diamond 2.1, 2.2
Fixed_3.0
Devices affected: LatticeECP3
CR115710

**EPIC DRC returns incorrect number of errors and warnings**

When you open a component for editing in EPIC's Logic Block View and run DRC for one selected item on the schematic (such as a slice mode), EPIC returns errors and warnings for the selected item. If you then select other items and run DRC for each of them, or if you repeat the process with the same item, EPIC DRC will not reset the numbering of warnings or errors with each DRC run. Instead, it will report a cumulative total of errors and warnings for all the DRC runs.

Versions affected: Diamond 2.2
Fixed_3.0
Devices affected: All
CR115470

**Maximum number of MachXO2 user I/Os differs from the number shown in Diamond**

The MachXO2 family maximum number of user I/Os shown and reported in the Diamond software should be reduced by 1 to account for the JTAGENB pin.

Versions affected: Diamond 2.0, 2.0.1, 2.1
Fixed_2.2
Devices affected: MachXO2
CR58288

**Process view not updated after changing source file list**

Sometimes when you modify the list of source files for a design, Diamond does not correctly reset the status in the Process view. This can happen when you add, remove, include, or exclude a source file.

Regardless of the status showing in the Process view, if you modify the source files, you need to rerun the implementation process from the beginning.
Incremental Design Flow can fail if design exceeds unmatched component threshold and contains XSIOLOGIC

In most cases when using Incremental Design Flow (IDF), if your design exceeds 20 percent unmatched components, you will receive a warning message, and IDF will automatically switch to normal design flow.

However, if your design contains an XSIOLOGIC element and also exceeds the 20 percent unmatched components threshold, IDF will display the warning message, but will then fail in normal design flow because it can’t locate the XSIOLOGIC location.

As a workaround, use the normal design flow.

ECO Editor signal probe displayed incorrectly

When you add a signal probe in the ECO Editor and then cross-probe to Floorplan View or Physical View, sometimes the wrong connection is displayed for the net.

To work around this issue, close Floorplan View or Physical View. Cross-probe the selected signal again from the Signal Probes sheet of ECO Editor. The correct connection will then be displayed.

Incremental Design Flow may not recognize anchor and bounding box

In some isolated cases when using Incremental Design Flow, some user-defined partitions may not recognize anchor and bounding boxes that are either specified by the user or automatically assigned by the engine. This symptom can be observed through the Partition Manager view.

If this happens, it is suggested that you run the normal design flow.
Error messages appear when memory is initialized to all 1s
If you have EBR-based modules in a MachXO2 design, error messages will be generated when you attempt to update initial memory to all 1s using the ECO Editor. This occurs for RAM_DP, RAM_DP_TRUE, RAM_DQ, and ROM. The error messages will appear when you try to save the .ncd file or when you run DRC.

To work around this issue, provide a memory file (.mem) that contains the initialization data.

Four ispLeverDSP blocks generate compare errors in Matlab/Simulink 7.5.0 (2007b)
The following ispLeverDSP blocks generate compare errors when using Matlab/Simulink 7.5.0 (2007b):

- Convolutional Encoder 3.4
- DA_FIR 2.1
- FIR 4.2
- NCO 2.5

This problem is due to a mismatch between Simulink blocks and the latest Lattice IP. New Simulink blocks will be provided upon request through the hot patch flow.

Note: ispLeverDSP is no longer supported starting with Diamond 2.2.
The ispLeverDSP Viterbi Decoder 4.5 will not generate in Matlab/Simulink 7.5.0 (2007b)
The ispLeverDSP Viterbi Decoder module, version 4.5, will not generate in Matlab/Simulink 7.5.0 (2007b). This problem is caused by a generation error due to a problem with the mdl2vhd.exe file. A new Simulink block, which updates the .mexw32 files for the blocks and the mdl2vhd.exe file, will be provided upon request through the hot patch flow.

Note: ispLeverDSP is no longer supported starting with Diamond 2.2.

Versions affected: Diamond 1.4, 1.4.1, 1.4.2, 2.0, 2.0.1, 2.1
Fixed_2.2
Devices affected: All
CR55567

Status icons in Reports view do not indicate when Tool Reports need updating
After changing the design or the strategy, the icons of the Tool Reports in the Reports view do not change to the question mark form. It looks like the Tool Reports are still up-to-date when they actually need to be rerun.

Either rerun the Tool Reports promptly after making changes or make a note that they are out of date.

Versions affected: Diamond 1.4
Fixed_2.0
Devices affected: All
CR54692

VCS cannot find EFB module
The VCS black-box encrypted models for MachXO2 have the wrong module content. The following files have to be replaced with a patch available from Lattice.

For Verilog simulation:
caelibrary\simulation\blackbox\machxo2_black_boxes.vp.zip

For VHDL simulation (need VCS-MX license):caelibrary\simulation\blackbox\machxo2_black_boxes_vhdl.vp.zip

Please contact Lattice Semiconductor customer support.

Versions affected: Diamond 1.2, 1.3
Fixed_1.4
Devices affected: MachXO2
CR54024
**Universal File Writer for Linux does not display all of the valid file types**

The Open Input Data File dialog box on Universal File Writer (UFW) for Linux does not display all of the valid file types. For example, for generating an SVF file, the valid input files are *.jed and *.isc. The Linux UFW only displays the *.isc file. The dialog box does not offer an “All Files” as a workaround.

There are two workarounds:

- Type the file name into the File name box.
- Run UFW using the command line.

Versions affected: Diamond 1.3 for Linux
Fixed_1.4  
Devices affected: All
CR54016

**Help does not work in Google Chrome browser**

When you try to open the help with Google Chrome, the browser displays an empty window. If you get the help from a server it works fine, but if you get the help from your local computer there’s nothing.

This is because Google added a security feature in March 2010 that interfered with the file:// protocol, which is at the heart of browser-based help that Diamond and other Lattice software uses. (This affects the help of many other companies' software too.)

Workarounds include:

- Open a different kind of browser (such as Internet Explorer) and browse to the index.htm file of the software’s help.
- Set a different kind of browser as your default browser.
- In Chrome, go to www.latticesemi.com and search on your topic there.
- Install the Lattice software on a server.
- Open Chrome from a command prompt with the following flag:

```
chrome --allow-file-access-from-files
```

**Note:** Doing this means that when you open any Web page that is resident on your computer - not just Diamond Help - the page will automatically run any active content that it has. While active content is common and can be very useful, malicious content can damage your files. Be sure you trust the software on your computer.

Versions affected: Diamond, Diamond 1.0, 1.1, 1.2, 1.3, 1.3.1, 1.4, 1.4.1, 1.4.2, 2.0, 2.0.1, 2.1, 2.2, 3.0, 3.1, 3.2
Fixed_3.3  
Devices affected: All
CR53868
**Cannot change column widths in Hierarchy view**

In the Hierarchy view, if you hover over a column divider, the cursor changes to a resizing cursor, but clicking and dragging has no effect.

The columns are automatically sized, so manually changing them is not available. Showing the resizing cursor is a mistake.

Versions affected: Diamond 1.3, 1.3.1, 1.4, 1.4.1, 1.4.2, 2.0, 2.0.1  
Fixed_2.1  
Devices affected: All  
CR53428

---

**Generate Hierarchy does not expand all the files**

Sometimes the Generate Hierarchy function fails to expand the Verilog files in a mixed Verilog/VHDL design. This happens when the top module is in VHDL.

The workaround is to create a top module in Verilog.

Versions affected: Diamond 1.0, 1.1, 1.2, 1.3, 1.3.1, 1.4, 1.4.1, 1.4.2, 2.0, 2.0.1, 2.2  
Fixed_3.0  
Devices affected: All  
CR52738

---

**Files modified by another application may not get saved in Diamond**

When a file is opened in Diamond, if you modify it in another application and switch back to Diamond, you will not be notified that the file is updated outside until the file editor in Diamond is activated.

In such cases, the Save All command may not save the file changes you made outside of Diamond. You may lose the changes without any notification.

Versions affected: Diamond 1.2, 1.3, 1.4  
Fixed_2.0  
Devices affected: All  
CR52655

---

**Error running BKM check to validate VCD files**

When running BKM check to validate the existence and timestamp of VCD files, you may get the following error message:

```
Running BKM Check  
ERROR: (ST-1303) Error running 'Module' BKM command 'moduleVCDCheck' on 'Module 'count'.  
-- Error Parsing command '[Module 'count' -stnode_0bc5d9d0] addExternalFile d:/test_tasks/bali_test/
```
temp/always/top/source/count_8.vcd
-- -- bad node command name "addExternalFile": must be -
help, getName, isVhdl, isVerilog, isEDIF, getTypeName, 
getNodeType, getInstancePath, getTitle, getToolTipInfo, 
getFileName, getLineNum, getColumn, getLineColInfo, 
isValid, getStickyNotes, hasStickyNotes, runBKM, canDrop, 
getDropText, addStickyNote, removeStickyNote, 
addAttribute, setAttribute, getAttributes, 
findAttributes, removeAttribute, addMessage, 
getStatusText, getLineFileText, getStatus, getInstances, 
getLibInstances, getAssignmentBlocks, 
getAssignmentBlockCount, getLibrary, findInstance, 
findNet, findPort, getNumLevels, getInstCount, 
getDefiningModule, getDefiningDefinitionBlock, 
getDefiningPrimaryBlock, getDefiningSecondaryBlock, 
getFullName, getBaseName, getSignals, getClocks, 
getWireorRegs, getWires, getRegisters, getChildren, 
getOwner, getNets, getPortCount, getPorts, getInPorts, 
getOutPorts, getInstantiations, isBlackBox, 
isDefined, isPrimitive, isLibCell, isRoot, prettyPrint, 
getAlwaysBlocks, getInitialBlocks, or 
getContinuousAssigns

BKM Check finished with (1) errors, and (0) warnings.

Clear Validate VCD from the Options dialog box (Tools > Options from the 
Diamond main window), the HDL Diagram > BKM > Verification section, to 
disable the check for VCD files.

Versions affected: Diamond 1.0, 1.1, 1.2
Fixed_1.3
Devices affected: All
CR52647

Predefined parameters set in the HDL Parameters section of the Project Properties dialog cannot be handled when generating hierarchy

Predefined parameters set in the HDL Parameters section of the Project properties dialog cannot be handled when generating hierarchy (Tools > Generate Hierarchy from the Diamond main window). For example, the bus width set in the HDL parameters section of the Project properties dialog cannot be displayed in the Hierarchy view.

Define parameters within a source file and include the source file to the project.

Versions affected: Diamond 1.2
Fixed_1.3
Devices affected: All devices
CR52589
Download of a software update does not work
On Linux, in the UPDATE dialog box, the Download button does nothing.

To download an update without immediately installing it, open Diamond’s main window and choose Help > Check for Updates. In the Start Page there is a frame that lists available updates. Find the desired update and click the Download icon that is next to it. There are two icons. Download is the one on the right. Hover over the icons to see labels.

Versions affected: Diamond 1.1 on Linux
Fixed_1.2
Devices affected: All
CR51749

Wrong file extension shown in “Managing Project Sources” help topic
In the Diamond online Help, in the Managing Projects > Managing Project Sources topic, there is a “Source Listed in the File List view” table. In this table, the IP Module Config File extension should be .ipx, not .lpc.

Versions affected: Diamond 1.0
Fixed_1.1
Devices affected: All
CR50432

Double-clicking .ldf cannot invoke Diamond on some Windows computers
For some Windows computers, double-clicking the Diamond project file (.ldf) cannot invoke the Diamond software. The Diamond installation cannot associate the Diamond project file extension .ldf to Diamond, because some Microsoft Applications lock this file extension for its use. An example is the Microsoft SQL Server log file.

Instead, start Diamond from the Windows Start menu. Then open the .ldf file by choosing File > Open > Project. In the Open Project dialog box, browse to the .ldf file and click Open.

Version affected: Diamond 1.0, 1.1, 1.2, 1.3, 1.3.1, 1.4, 1.4.1, 1.4.2, 2.0, 2.0.1, 2.1, 2.2
Fixed_3.0
Devices affected: All
CR49233
HDL Diagram cannot display hierarchy correctly for some pure EDIF designs
With a pure EDIF design including multiple EDIF files, after running the Generate Hierarchy process, you may find the top module and sub-modules are shown in the same level in the HDL Diagram.

Diamond HDL Diagram is designed to support a single EDIF file. If there are multiple EDIF files in a pure EDIF design, all the EDIF files are treated as separate single EDIF designs and the hierarchy will be displayed in HDL Diagram in the same level.

To see the hierarchy, merge all the design units into one EDIF file.

Versions affected: Diamond 1.0, 1.1, 1.2
Fixed_1.3
Devices affected: All
CR49214

HDL Diagram cannot display hierarchy correctly for some VHDL/EDIF designs
If you have a mixed VHDL/EDIF design, the top of which is a VHDL file, and run the Generate Hierarchy process in Diamond, you will find in HDL Diagram that the top module is connected to empty submodules and the submodules are shown as “not loaded”. Design units in EDIF files will be displayed in separate hierarchy trees.

Workaround: none.

Versions affected: Diamond 1.0
Fixed_1.1
Devices affected: All
CR49213

Removing an implementation from Diamond does not delete the result files from the implementation directory
Removing an implementation from Diamond will not delete the result files from the implementation directory.

Manually delete the files or the implementation directory if needed. If deleting the implementation directory, be careful to make sure that there are no source files in the implementation directory.

Versions affected: All
Devices affected: All
CR48000
ispLeverDSP cannot work properly due to the missing search path
The ispLeverDSP blocks in Diamond cannot be run correctly in MATLAB/Simulink. This is caused by the missing search path.

To solve the problem, take the following procedures to set the search path in both MATLAB and Windows System Environment Variables.

1. In the MATLAB startup window, choose File > Set Path to open the Set Path dialog box. Add the following paths to the search path list:

   `<diamond_installation_path>\ispLeverDSP`
   `<diamond_installation_path>\ispFPGA\bin\nt`

2. Go to the Windows Control Panel. Choose System > Advanced > Environment Variables > System Variables. Add the above two paths to the search path list.

After adding the two search paths in MATLAB and the Windows Environment Variables tab, re-run MATLAB/Simulink.

Versions affected: Diamond 1.0
Fixed_1.1
Devices affected: All
Other Lattice Software

This section lists the known issues and workarounds of other Lattice software including ispLEVER Classic, PAC-Designer, LatticeMico System, ispVM System, and ORCAstra. Descriptions include the software versions and devices affected. If you are looking for a workaround to a problem, search for related terms including the tool name or a word from an error message, or scan the Contents. If you want issues for a certain version, search for the version number. This will find issues affecting that version and issues fixed in that version of the software.

ispLEVER Classic

UAC dialog will display with multiple schematic designs

On Windows 7 or Windows Vista, when the User Account Control (UAC) is on, an Unknown Publisher dialog box displays when running multiple schematic designs because of the engine updatesc.exe.

If you see this, click Yes to continue.

Versions affected: ispLEVER Classic, all versions
Devices affected: All
CR54791
Timing Analysis View display status is incorrect after reloading
While Timing Analysis View is opening, if you change a design and rerun it, Timing Analysis View reloads but the fmax result is not cleared. After switching to another timing analysis and back, you are not able to run to redo the timing analysis.

If you see this, close and re-open Timing Analysis View.

Versions affected: ispLEVER Classic 1.5
Fixed_1.6
Devices affected: All
CR54581

Constraint Editor does not reload design changes automatically
Constraint Editor does not reload design changes automatically. While running Constraint Editor, if you change design signals or change the properties of synthesis to assign different internal signals, and then rerun the Constraint Editor process, the Constraint Editor will only reload the .lct file, but the design changes will not automatically update.

After making the changes, close and re-open Constraint Editor.

Versions affected: ispLEVER Classic 1.4
Fixed_1.5
Devices affected: All
CR54580

Pullup on global reset does not work
Adding a pullup to the RST (global reset) pin of an ispLSI design does not appear to have any effect in the JEDEC output.

In fact, ispLSI 1000 and 2000 do not support a pullup on the global reset pin. So the JEDEC file is correct. If needed, the pullup should be added externally.

Versions affected: ispLEVER Classic 1.4 and earlier
Fixed_1.5
Devices affected: ispLSI 1000, ispLSI 2000
CR54330

IO power guide (PG) property wrongly set to Enable
When an I/O is used as BIDI in the combinational circuit, the IO Power Guard (PG) property is wrongly set to Enable in the Jedec file after running the "Fit Design" process.

Contact Lattice technical support to get a software patch.
Wrong device package information for ispGAL22V10av-75LN shown in Fitter Report and Jedec File

If you select ispGAL22V10AV-75LN, after compilation, you will find “QP28” shown in the fitter report and the Jedec file. The correct display for this package should be “QP32”.

Contact Lattice technical support to get a software patch.

Some signals in sub-modules cannot be viewed in the Active-HDL waveform editor

While doing simulation in Active-HDL, some signals in sub-module file cannot be viewed in the Active HDL Waveform Editor.

Rerun the simulation in the Active-HDL console window using the following command:

```
vsim +access +r <testbench_module_name> -L <library_name>
```

Some mature products are not supported by ispLEVER Classic

Some of the older, or "mature," devices cannot be designed for using ispLEVER Classic.

First of all, make sure the device is not supported by ispLEVER Classic. In the Device Selector dialog box, select Show Obsolete Devices (bottom-right of the dialog box) and check again for the device.

If you still don't see it, you need to use Lattice Semiconductor's ispDesignEXPERT 8.x, an older form of Lattice's design software. (If you do not have ispDesignEXPERT, contact Lattice Technical Support.) If you do not
see the device offered in ispDesignEXPERT, use the following procedure to enable the mature devices.

The basic procedure is to replace the device's .sds file in ispDesignEXPERT System and the .lst file in ispDesignEXPERT Compiler with the corresponding .obs files.

To enable mature devices in ispDesignEXPERT:

1. Go to the <install dir>\ispsys\config\device folder and find the family parts list for the device. The file name is based on the device family name, such as plsi1k.obs or mach2.obs.
2. Copy this file to <install dir>\ispsys\config, one level up.
3. Rename the corresponding .sds file. For example, change plsi1k.sds to plsi1k.new.
4. Rename the .obs file that you found to match the original .sds file. For example, change plsi1k.obs to plsi1k.sds.
5. If you are working on a MACH device, restart ispDesignEXPERT. If you are working with an ispLSI device, continue with the following steps.
6. Go to the <install dir>\ispcomp\config\device folder and find the parts list, lscpart.obs.
7. Copy lscpart.obs to <install dir>\ispcomp\config, one level up.
8. Rename the lscpart.lst file. For example, change lscpart.lst to lscpart.new.
9. Rename the lscpart.obs file that you found to lscpart.lst.
10. Restart ispDesignEXPERT.

The .obs files include both production and mature devices, so reverting back to the original .sds and .lst files is not necessary.

Versions affected: ispLEVER Classic, all versions
Devices affected: ispLSI, MACH

CR51768

Functional simulation result incorrect in Lattice Logic Simulator

In some designs, if reset is used as both reset and general logic, the functional simulation result might be incorrect in Lattice Logic Simulator. However, the timing simulation works fine.

Change to simulating your design in Active-HDL.

Versions affected: ispLEVER Classic 1.2, 1.3, 1.4
Fixed_1.5
Devices affected: ispMACH 4000
CR51496
**ORCA Series 3 shows in the Device Selector Dialog by error**

During installation, you do not select ORCA Series 3 devices, but after you install the control pack, ORCA Series 3 appears in the Device Selector dialog box.

Do not select ORCA Series 3 from the Device Selector dialog box if you did not choose ORCA Series 3 during installation.

Versions affected: ispLEVER Classic 1.0, 1.1  
Fixed_1.2  
Devices affected: ORCA Series 3  
CR39502

**ModelSim fails to simulate due to obsolete simulation library**

An error occurs if the simulation libraries were compiled with an older version of ModelSim and are now being loaded into a newer version. For example, if your design was compiled using ModelSim Lattice OEM 5.8c and is then loaded using ModelSim Lattice OEM 6.2i, this error occurs.

To prevent this error, contact Lattice Support to get recompiled libraries for latest version of ModelSim.

This problem can also be fixed by finding the obsolete library and right-clicking that library from the left-hand window (library pane) of the newer version ModelSim. When right-clicking the selected library, you will find that one of the options is to refresh.

Click the refresh option. This should start library refreshing, and the error should not occur.

**Note**

To refresh the library, you need write permission to the folder where the library resides.

Versions affected: ispLEVER Classic, all versions  
Devices affected: All  
CR37933

**EPIC allows LUT editing in “No-Logic-Changes” mode**

EPIC Device Editor allows LUT equation editing (editblock/properties) in "No-Logic-Changes" mode for ORCA Series 2 devices. Users are not advised to edit the equations in LUT of ORCA Series 2 devices in “no-logic-changes” mode of EPIC Device Editor.
Versions affected: ispLEVER Classic, all versions
Devices affected: ORCA Series 2 Devices
CR36004

**Constraint Editor fails intermittently on Unix/Linux**
The Constraint Editor fails intermittently on Linux and Solaris running on the OpenLook environment.

Solaris users can use CDE (Common Desktop Environment) to avoid this problem. If you use Linux or Solaris running on OpenLook, close the Constraint Editor and re-open it until it works.

Versions affected: ispLEVER Classic 1.0, 1.1
Fixed_1.2
Devices affected: ORCA Series 2, ORCA Series 3
CR36003

**ispLEVER Classic requires read-write permission on the folder defined in $LSC_INI_PATH**
If the ispLEVER software is installed on a Windows XP system with administrator privilege and to be used by an account in the “Users” group, Project Navigator may not function correctly. The cause is that users have no read-write access to the folder where user settings are stored.

In such cases, make sure that the user account has read-write permission on the folder defined in the $LSC_INI_PATH environment variable, so that the user can create new configuration files and modify all the existing configuration files in that folder. The default $LSC_INI_PATH value is “<boot_drive>:LSC_ENV” on Windows.

Version affected: ispLEVER Classic 1.0, 1.1
Fixed_1.2
Devices affected: All
CR34145

**PAC-Designer**

**PAC-Designer USB driver is not up-to-date with Windows**
The PAC-Designer USB driver is not up-to-date with Windows Vista and later operating systems. Consequently, devices cannot be programmed within the PAC-Designer environment.

PAC-Designer USB driver is not up-to-date with Windows

After using PAC-Designer to generate the JEDEC file, use Diamond Programmer to program the device.
Versions affected: PAC-Designer 6.2, 6.23, 6.24, 6.25, 6.26
CR57682

VHDL designs using mixed-case characters can cause error messages
Since VHDL is not sensitive to uppercase letters, error messages can occur when using such declarations as "RESET_ALL", "cltrim0", "cltrim1" and "POTS_OK".

To avoid this, set the FPGA environment to Verilog.

Versions affected: PAC-Designer 6.1
Fixed_6.2
Devices affected: Platform Manager
CR53920

Platform Manager designs with a timer in the VHDL netlist always show an “X” during simulation
In PAC-Designer, when running the PLD gate-level simulations with Platform Manager VHDL designs, the signal timer_tc always shows an “X” during the PLD simulation time. This is caused by clock edge and input data changes occurring at the same time stamp.

Instead, export a Verilog netlist for the PLD simulation.

Versions affected: PAC-Designer 6.1
Fixed_6.2
Devices affected: Platform Manager
CR53919

Windows 7 does not associate .pac files with PAC-Designer
Double-clicking on a .pac file in an Explorer window does not open the file. Instead it brings up the Windows 7 Open With dialog box.

To open the file:
1. Click Browse and browse to where you installed PAC-Designer.
2. Select PACD##.exe and click Open.
3. In the Open With dialog box, select PAC-Designer.
4. Select Always use the selected program to open this kind of file.
5. Click OK.

PAC-Designer opens with the file. In the future, double-clicking a .pac file will open PAC-Designer.
Versions affected: PAC-Designer 6.0.1, 6.1
Fixed_6.2
Devices affected: All
CR53870

**PlatformManager_10-12107_I2C_Utility doesn’t work**
The PlatformManager_10-12107_I2C_Utility doesn’t work in PAC-Designer. A connection cannot be established between the computer and the Platform Manager board. “No device found” or “check Cable connection or device address” error messages are displayed.

Versions affected: PAC-Designer 6.1
Fixed_6.2
Devices affected: Platform Manager
CR53849

**.ini file in c:/lsc_env cannot be written using Windows 7 or Windows Vista OS**
After installing PAC-Designer on PCs running using Windows 7 or Windows Vista operating systems, the .ini file in c:/lsc_env is created successfully, but it cannot be written to by the software.

To make the .ini file writable:
1. Copy the .ini file to another location.
2. Delete the original .ini file.
3. Rename the copied .ini file to the original .ini file name.

Versions affected: PAC-Designer 6.1
Fixed_6.2
Devices affected: Platform Manager
CR53708

**VID Demo fails to compile when using VHDL entry**
The Platform Manager Development Kit Power Supply Voltage Control (VID) Demo source files fail to compile when using VHDL entry. There are two issues:

- Some of the port definitions require a semicolon to end.
- Signal D4 is an output type and is connected to both output and inout ports. VHDL does not allow this.

To fix this, add a semicolon to the end of these signal definitions, and define signal D4 as a buffer.
PAC-Designer does not support device downloading on Windows 7

If your operating system is Windows 7, you cannot download a design to a device in PAC-Designer.

Instead, use ispVM System or Diamond Programmer to download the design.

PAC-Designer crashes when compiling a LogiBuilder design

Add an FPGA node in the Logic I/O Assignment dialog box, and open LogiBuilder to assign the node in a supervisory logic equation. After that, if you delete the node with the Logic I/O Assignment dialog box, the node name will appear as “???” in the LogiBuilder window. Then, if you compile the LogiBuilder design, the PAC-Designer software crashes.

To resolve the issue, after deleting the FPGA node in the Logic I/O Assignment dialog box, also delete the node assignment from the LogiBuilder Equation table. Then save the project and run compilation again.

PAC-Designer fails to export Jede after compiling a LogiBuilder design in ABEL mode

When CPLD LogiBuilder is in ABEL mode, if you use FPGA LogiBuilder to compile the design, and then choose File > Export from the main window to export a Jede file, you will receive the error message, “Your design has changed, so you will need to recompile the design before you download or export.”

To avoid this issue, before exporting Jede, save the ABEL file in CPLD LogiBuilder and re-compile the design in FPGA LogiBuilder, or compile the design in the ABEL Source View by choosing Tools > Compile Design.

Versions affected: PAC-Designer 6.1
Fixed_6.2
Devices affected: Platform Manager
CR53371

Versions affected: PAC-Designer all versions
Devices affected: All
CR52248

Versions affected: PAC-Designer 6.0, 6.0.1
Fixed_6.1
Devices affected: Platform Manager
CR52071

Versions affected: PAC-Designer 6.0, 6.0.1
Fixed_6.1
Spaces in PAC-Designer project path are not allowed
PAC-Designer does not allow you to create a project in a path that contains a directory with spaces in its name.

Versions affected: PAC-Designer, all versions
Devices affected: Platform Manager
CR51080

A Clock Frequency Hz radio button does not work in PAC-Designer
In PAC-Designer, the Clock Frequency Hz radio button does not work in the “Edit Clock and Simulation Time” dialog box. To enter a Hz value, select the kHz radio button and divide the clock frequency by 1000.

Versions affected: PAC-Designer 5.0, 4.99a, 4.99, 4.98, 4.97, 4.96, 4.95, 4.9, 4.8, 4.7, 4.6, 4.5, 4.3, 4.2, 4.1, 4.0
Fixed_5.1
Devices affected: ispPAC-POWR1220AT8, ispPAC-POWR1014/A, LA-ispPAC-POWR1014/A, ispPAC-POWR6AT6, ispPAC-POWR1208P1, ispPAC-POWR1208, ispPAC-POWR607, ispPAC-POWR604
CR43522

LatticeMico System

EFB not enabled with MachXO3LF when creating a LatticeMico System Builder platform
When creating a platform in LatticeMico System Builder for a MachXO3LF design, if you choose MachXO3LF in the Platform Wizard, the EFB component will not be enabled.

As a workaround, you can create a platform specifying a MachXO2 device instead. This will enable the EFB component, and your MachXO3LF design will work properly.

Versions affected: LatticeMico System 3.4.1
Devices affected: MachXO3LF
CR124013
Debug Configuration operation may time-out over a slow Linux network

When running the Linux version of LatticeMico System software remotely over a slow Linux network connection, the Run > Debug Configuration operation may hang or display an “Unknown Device” error message.

The workaround is to debug your design using the LatticeMico System software installed on a local computer (PC or Linux), rather than running over a Linux network.

Versions affected: All LatticeMico System software versions
Fixed_3.1
Devices affected: All
CR117821

LatticeMico Mutli-Memory deployment does not work under certain conditions

LatticeMico Mutli-Memory deployment does not work under certain conditions.

This issue affects the LatticeMico8 Memory Deployment flow under the Tools > Software Deployment tab in the LatticeMico SPE perspective. It happens when you choose the same memory instance for the Program memory and the Read/Write Data memory, but choose a different memory instance for the Read-Only Data memory.

You can detect this issue by reading the log message in the console. A correct Multi-Memory deployment flow generates multiple memory files that contain the following five sections:

.boot
.text
.rodata
.data
.bss

If any of these sections are missing, the memory initialization files were incorrectly generated.

The workaround is to generate the memory files manually in the LatticeMico System SDK shell:

1. You can find the memory segment information using the following command:

   `lm32-elf-readelf -l <elf_file>`

2. Then you can deploy the memory segments into corresponding memory files using the following two commands:

   `lm32-elf-objcopy [-j <section>] -O binary <elf_file> <application_bin>`
bin_to_verilog --h --EB --width 4 <application_bin> <memory_file>

Example:
******
Elf file type is EXEC (Executable file)
* Entry point 0x2000000
* There are 3 program headers, starting at offset 52
* * Program Headers: * Type Offset VirtAddr PhysAddr FileSiz MemSiz Flg Align
  * LOAD 0x001000 0x02000000 0x02000000 0x01ffc 0x01ffc R E 0x1000
  * LOAD 0x003000 0x04200000 0x02001ffc 0x0008c 0x0008c R 0x1000
  * LOAD 0x003ffc 0x02001ffc 0x02002088 0x00078 0x002f0 RW 0x1000
* * Section to Segment mapping:
* Segment Sections...
* 00 .boot .text
* 01 .rodata
* 02 .data .bss
******

As shown in the above example, the lm32-elf-objcopy program header and segment mapping help you determine that:

► The .boot, .text, .data, and .bss files go into one memory segment.
► The .rodata file goes into another memory segment.

3. Then run the following commands to generate multiple memory files:

```
Im32-elf-objcopy -j .boot -j .text -j .data -j . bss -O binary <elf_file> <application_bin>
<diamond_directory>/micosystem/utilities/bin_to_verilog --h --EB --width 4 <application_bin> <memory_file>

Im32-elf-objcopy -j .rodata binary <elf_file> <application_bin>
<diamond_directory>/micosystem/utilities/bin_to_verilog --h --EB --width 4 <application_bin> <memory_file>
```

For more details about the lm32 command, refer to the “Software Development Utilities” chapter of the LatticeMico32 Software Developer User Guide.

Versions affected: LatticeMico System 2.1, 2.2
Fixed_3.0
Devices affected: All
CR59106

Running LatticeMico32 Flash Deployment in Diamond 32-bit for Windows may cause error

When performing LatticeMico32 Flash Deployment using LatticeMico System C/C++ perspective in Diamond 32-bit for Windows, you may receive the following error:
/cygdrive/c/bug/57989/ecp2/spiflashprogrammer/Debug/.fgdbini:1: Error in sourced command file:
localhost:1000: Connection refused.
(gdb)

If you see this error, start LatticeMico System SDK Shell by choosing **Start > Lattice Diamond > Accessories > LatticeMico System SDK Shell**, and run `tcp2jtagvc2` before you perform LatticeMico32 Flash Deployment.

Versions affected: LatticeMico System 2.0, 2.0.1
Fixed_2.1
Devices affected: All FPGAs
CR58040

**LatticeMico System SPE/Debug printf to console does not display**

On Linux operating systems only, the C printf to SPE/Debug console does not display, giving an impression that there is an error.

This issue is seen on Red Hat Enterprises versions 4, 5, and 6. The Windows operating system does not have this issue.

As a workaround on Linux operating systems, run the debugger from the command-line. C printfs will then be seen correctly.

Versions affected: LatticeMico System 2.0
Fixed_2.0.1
 Devices affected: All
CR57690

**In LatticeMico System, the platform.mk file must be modified to work on Linux**

The platform.mk file located in:
`<Mico_install_directory>/utilities/templates/std_mk_makefile_sample`
will not work on Linux systems because the following line in the file is incorrect:
`PLATFORM_BLD_CFG=debug`

The line should be modified so that the “D” in the word “Debug” is upper-case, as follows:
`PLATFORM_BLD_CFG=Debug`

Versions affected: LatticeMico System 2.0, 2.0.1
Fixed_2.1
Devices affected: All
CR57379
LatticeMico installation "splash screens" appear small on some Linux systems

On some Linux systems, such as Red Hat RHEL 6-64, the "splash screens" that display during installation can appear small--measuring approximately 1-inch by 1-inch--rather than full-size.

This issue happens on RHEL 6-64 if the 32-bit library libz.so.1 is not installed before gtk2-2.18.9-6.el6.i686.

The gtk2-2.18.9-6.el6.i686 file does not report the dependency for 32-bit libz.so.1 library properly. If 32-bit libz.so.1 is not installed when you install gtk2-2.18.9-6.el6.i686, you will receive a warning and an installation "Complete!" message. The following is an example of a warning and a "Complete!" message:

Non-fatal POSTIN scriptlet failure in rpm package gtk2-2.18.9-6.el6.i686
/usr/bin/gdk-pixbuf-query-loaders-32: error while loading shared libraries: libz.so.1: cannot open shared object file: No such file or directory
/usr/bin/gtk-query-immodules-2.0-32: error while loading shared libraries: libz.so.1: cannot open shared object file: No such file or directory
warning: %post(gtk2-2.18.9-6.el6.i686) scriptlet failed, exit status 127
duration: 105(ms)
Installed products updated.
Installed:
gtk2.i686 0:2.18.9-6.el6
Complete!

The small "splash screens" issue has no impact on the actual installation of LatticeMico System software. The software will work. However, as a workaround to avoid the small "splash screens" issue, install the 32-bit library libz.so.1 before gtk2-2.18.9-6.el6.i686.

Versions affected: LatticeMico System 2.1
Fixed_2.2
Devices affected: All
CR57236

Items may be missing from dialog boxes on systems running Windows 7 64-bit OS

On systems running Windows 7 64-bit operating systems, deployment icons may be missing in the MSB Software Deployment Tools dialog box and in the C/C++ Debug dialog box.

Workaround this problem by doing one of the following:

- Use a 32-bit Windows OS to run MSB
- Use a Linux OS to run MSB
Use the MSB SDK Shell to execute the necessary commands manually:

```
/micosystem/gtools/lm8/bin/lm8-elf-objcopy -j .text -O binary .elf prom_init.bin
/micosystem/utilities/bin_to_verilog --LM8 --h --EB --width 3 prom_init.bin prom_init.mem
/micosystem/gtools/lm8/bin/lm8-elf-objcopy -j .data -j .irq_stack -O binary .elf scratchpad_init.bin
/micosystem/utilities/bin_to_verilog --LM8 --h --EB --width 1 scratchpad_init.bin scratchpad_init.mem
```

Versions affected: LatticeMico System 1.3, 1.4
Fixed 2.0
Devices affected: All
CR54010

**Address locking does not function for components with multiple Wishbone slave ports**

Address locking does not function for components with multiple Wishbone slave ports. The next time a platform is opened in MSB, it loses the address lock for these components, even when the lock was explicitly set the prior time it was opened in MSB.

Versions affected: LatticeMico System 1.3
Fixed 1.4
Devices affected: All
CR53907

**Cannot launch TCP2JTAGVC2 from command-line shell in Lattice Mico System**

Command-line debugging of LatticeMico32 designs via the LatticeMico System SDK Shell requires launching the TCP2JTAGVC2 process prior to launching lm32-elf-gdb. The shell does not recognize the TCP2JTAGVC2 executable.

The fix is to set the PATH environment variable using the following syntax:

```
export PATH=/micosystem/gtools/bin:$PATH
```

Versions affected: LatticeMico System 1.2
Fixed 1.3
Devices affected: All
CR52714
“Failed to Load USB Driver” error in MSB if Diamond 1.2 is uninstalled
If you install both Diamond 1.1 and Diamond 1.2, and then uninstall Diamond 1.2, the TCP2JTAGVC2 application that provides the communication channel between the LatticeMico32 microprocessor debug module and lm32-elf-gdb may not function properly when running Mico System Builder (MSB).

The following error message may be returned:

“Failed to Load USB Driver.”

This should only be a problem if running Diamond 1.1 MSB, as this has been fixed in Diamond 1.2 MSB.

As a workaround, set the ISPVM_DIR system variable to the Diamond 1.1ispvmsystem directory.

For example:

Variable name: ISPVM_DIR
Variable value: c:\lscc\diamond\1.1\ispvmsystem

Versions affected: LatticeMico System 1.1
Fixed_1.2
Devices affected: All
CR52634

Unable to open IPexpress from Lattice Mico System Builder on Linux
On Linux, the LatticeMico32 System for Diamond does not allow you to open IPexpress from within the Lattice Mico System Builder user interface (MSB). To generate an IP, you must open IPexpress separately and generate the IP. The work-around differs, depending on whether you want to generate a VHDL NGO file or not. The following procedure shows how to generate an IP using both options.

1. Create a Platform in Lattice MSB. In the Platform Wizard, select Create VHDL Wrapper if desired.

   Leave “Create VHDL NGO File” unselected. You will create the VHDL NGO file in a final step if needed.

2. Open IPexpress and select the IP.

3. In the Project Path, select the Diamond project location where you will implement the LatticeMico32 platform.

4. Generate the IP.

   IPexpress creates some IP source files in the following directory:../<project_directory>/<IP_name_eval>models/<dev>
   where dev is your choice of device family.
5. Return to Lattice MSB and double-click the IP name to open the dialog box and add the IP to the platform.

6. Browse to the Diamond project directory you used in Step 3 and select the project .ldf file.

7. Browse to the location of the IP NGO file generated in Step 4, select the `<IP_name>.ngo` file and click OK.

8. Run generator from MSB.

9. Copy all files from:
   
   `<project_directory>/<IP_name_eval>/models/<dev>`
   
   to:
   
   `../components/<IP_directory>/rtl/verilog`

10. If you need to create the VHDL NGO file, add the following steps:

   ▶ Open the Properties dialog box in MSB and select **Create VHDL Wrapper** and **Create NGO File**.

   ▶ Rerun the generator from MSB.

**ispVM System**

**USB2 cables do not work using RedHat 32-bit Linux OS**

USB2 cables do not work in ispVM System using RedHat 32-bit Linux OS.

Instead, use USB or parallel cable for download.

Versions affected: ispVM 18.0.1
Devices affected: All
CR54019

**ORCAstra**

**ORCAstra fails when setting up the JTAG Hub interface**

ORCAstra gets random errors when attempting to set up the JTAG Hub interface to a LatticeECP3 PCI Express Evaluation Board. ORCAstra reports one of several errors:

▶ “ORCA-sta has encountered a problem and needs to close.”

▶ All ones were written, so ORCAstra reverts to demo mode.

▶ Corrupted data transmission, so ORCAstra reverts to demo mode.
If you see this problem, try restarting ORCAsra.

Versions affected: Diamond 1.1
Fixed_1.2
Devices affected: LatticeECP3
CR51683