MachXO3D Product Family Qualification Summary

Lattice Document # MS – 200040 July 2020

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1.0 INTRODUCTION

The MachXO3D™ device family is the next generation of Lattice Semiconductor Low Density PLDs including enhanced security features and on-chip dual boot flash. The enhanced security features include Advanced Encryption Standard (AES) AES-128/256, Secure Hash Algorithm (SHA) SHA-256, Elliptic Curve Digital Signature Algorithm (ECDSA), Elliptic Curve Integrated Encryption Scheme (ECIES), Hash Message Authentication Code (HMAC) HMAC-SHA256, Public Key Cryptography, and Unique Secure ID. The MachXO3D family is a Root-of-Trust hardware solution that can easily scale to protect the whole system with its enhanced bitstream security and user mode functions. MachXO3D device provides breakthrough I/O density with high number of options for I/O programmability. The device I/O features the support for latest industry standard I/O, including programmable slew-rate enhancements and I3C support.

The MachXO3D family of low power, instant-on, Flash based PLDs have two devices with densities of 4300 and 9400 Look-Up Tables (LUTs). MachXO3D devices include on-chip dual boot configuration flash as well as multi-sectored User Flash Memory (UFM). In addition to LUT-based programmable logic, these devices feature Embedded Block RAM (EBR), Distributed RAM, Phase Locked Loops (PLLs), pre-engineered source synchronous I/O support, advanced configuration support including on-chip dual-boot capability and hardened versions of commonly used functions such as SPI controller, I2C controller, and timer/counter.

The MachXO3D devices are designed on a 65-nm non-volatile low power process. The device architecture has several features such as programmable low swing differential I/O and the ability to turn off I/O banks, on-chip PLLs and oscillators dynamically. These features help manage static and dynamic power consumption resulting in low power for all members of the family.

The MachXO3D devices are available in two performance levels: ultra low power (ZC) and high performance (HC). ZC/HC devices have an internal linear voltage regulator, which supports external VCC supply voltages of 3.3 V or 2.5 V. With the exception of power/performance profiles, the two types of devices, ZC and HC, are pin compatible with each other.

The MachXO3D PLDs are available in a broad range of advanced halogen-free packages ranging from the space saving 10 x 10 mm QFN to the 19 x 19 mm caBGA. MachXO3D devices support density migration within the same package.

This report details the Commercial/Industrial reliability qualification results of the MachXO3D Commercial/Industrial Product Family.

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2.0 LATTICE PRODUCT QUALIFICATION PROGRAM

Lattice Semiconductor Corp. maintains a comprehensive reliability qualification program to assure that each product achieves its reliability goals. After initial qualification, the continued high reliability of Lattice products is assured through ongoing monitor programs as described in Lattice Semiconductor's Reliability Monitor Program Procedure (Doc. 101667). All product qualification plans are generated in conformance with Lattice Semiconductor's Qualification Procedure (Doc. 100164) with failure analysis performed in conformance with Lattice Semiconductor's Failure Analysis Procedure (Doc. 100166). Both documents are referenced in Lattice Semiconductor's Quality Assurance Manual, which can be obtained upon request from a Lattice Semiconductor sales office. Figure 2.1 shows the Product Qualification Process Flow.

If failures occur during qualification, an 8D process is used to find root cause and eliminate the failure mode from the design, materials, or process. The effectiveness of any fix or change is validated through additional testing as required. Final testing results are reported in the qualification reports.

Failure rates in this reliability report are expressed in FITs. Due to the very low failure rate of integrated circuits, it is convenient to refer to failures in a population during a period of 10^9 device hours; one failure in 10^9 device hours is defined as one FIT.

Product families are qualified based upon the requirements outlined in Table 2.2. In general, Lattice Semiconductor follows the current Joint Electron Device Engineering Council (JEDEC) and Military Standard testing methods. Lattice automotive products are qualified and characterized to the Automotive Electronics Council (AEC) testing requirements and methods. Product family qualification will include products with a wide range of circuit densities, package types, and package lead counts. Major changes to products, processes, or vendors require additional qualification before implementation.

The MachXO2, MachXO3L, MachXO3LF and MachXO3D families are all 65nm technology-based product offerings that leverage the same silicon design blocks, wafer fabrication design rules, bills of materials, and assembly processes & test sites. Therefore, the MachXO3D FPGA product family qualifications are based on a combination of device specific qual data and family generic qual data as per the Lattice Semiconductor Qualification Procedure, Doc. 100164.

Lattice Semiconductor maintains a regular reliability monitor program. The current Lattice Reliability Monitor Report can be found at Product Reliability Monitor Report.

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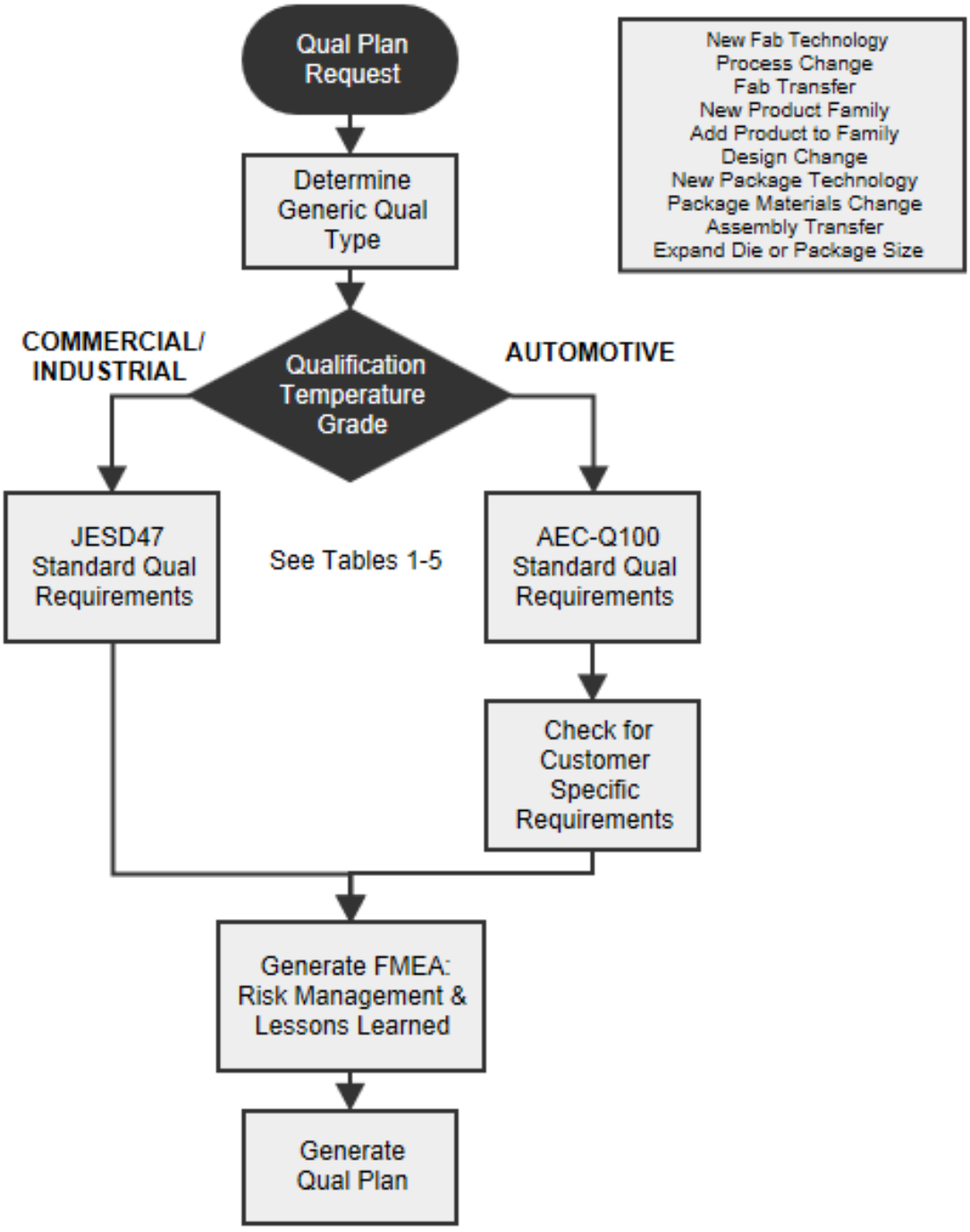
Figure 2.0.1 Lattice Standard Product Qualification Process Flow

This diagram represents the standard qualification flow used by Lattice to qualify new Product Families. The target end market for the Product Family determines which flow options are used. The MachXO3D Product Family was qualified using the Commercial / Industrial Qualification Option.



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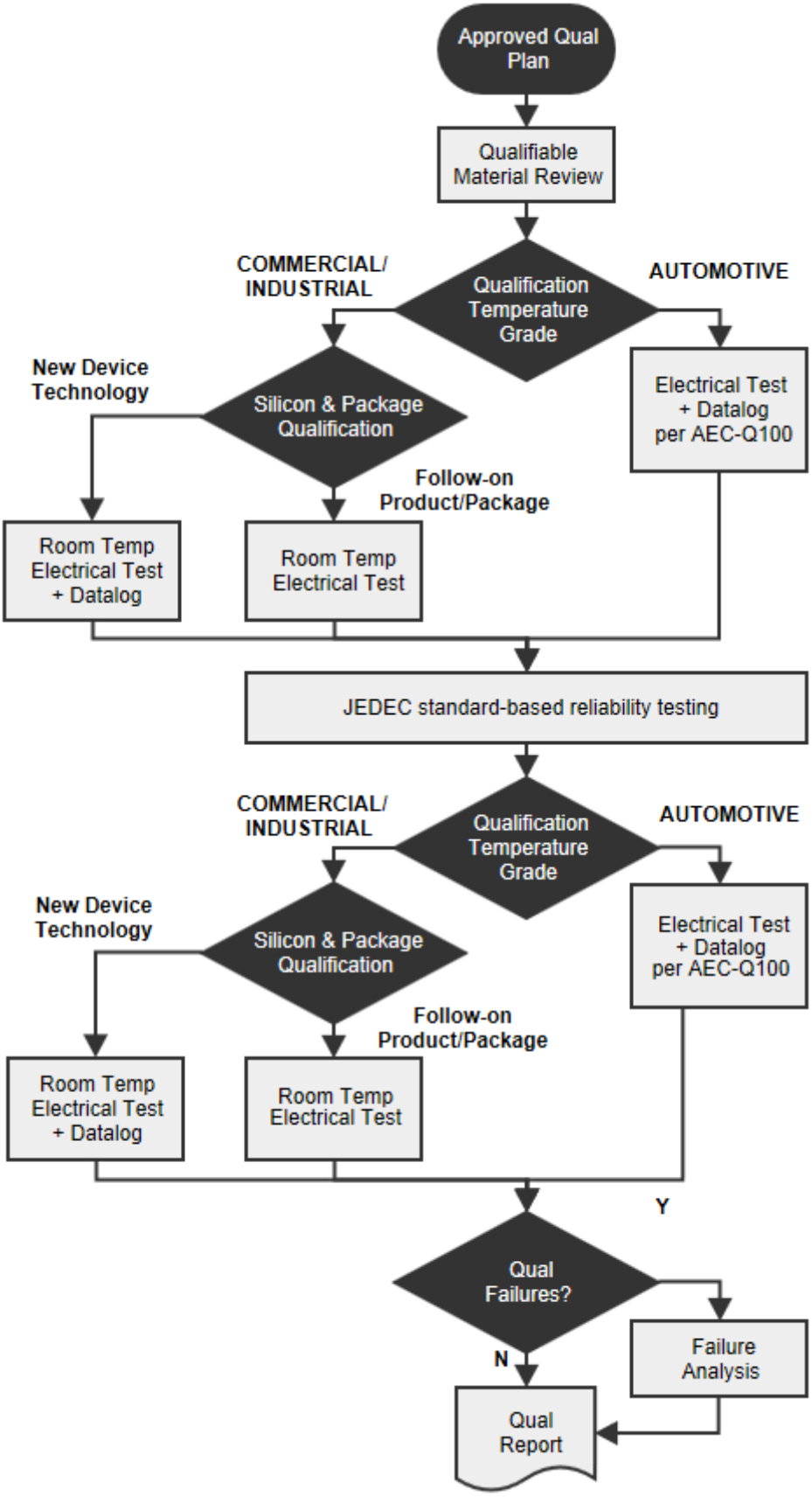

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Table 2.0.2 Standard Qualification Testing

TEST	STANDARD	TEST CONDITIONS
High Temperature Operating Life (HTOL)	JESD22-A108	≥125°C Tj and max operating supplies
Human Body Model ESD (HBM)	JS-001	25°C (Technology/Device dependent Performance Targets)
Charged Device Model ESD (CDM)	JS-002	25°C (Technology/Device dependent Performance Targets)
Latch-Up (LU)	JESD78	Class II, +/-100mA trigger current and 1.5x max operating supplies
Non-Volatile Cycling Endurance (NVCE)	JESD47 JESD22-A117 AEC Q100-005	25°C, 85°C depending on follow-on stress Continuous program/erase operation
Post-Cycle High Temperature Data Retention (PCHTDR)	JESD47 JESD22-A117 AEC Q100-005	150°C ambient, unbiased
Low Temperature Data Retention (LTDR)	AEC Q100-005	25°C ambient, unbiased
Un-Cycled High Temperature Data Retention (UCHTDR)	JESD47 JESD22-A117	150°C ambient, unbiased
Post-Cycle High Temperature Operating Life (PCHTOL)	AEC Q100-005 JESD22-A108	≥125°C Tj and max operating supplies Periodic Flash read and device configuration
Accelerated Soft Error Testing (ASER)	JESD89	25°C, Nominal operating supplies
Surface Mount Pre-conditioning (SMPC)	IPC/JEDEC J-STD-020 JESD-A113	Per appropriate MSL level per J-STD-020
High Temp Storage Life (HTSL)	JESD22-A103	Condition B
Temperature Cycling (TC)	JESD22-A104	Condition B, soak mode 2 (typical)
Temperature Humidity Bias (THB) or Biased Highly Accelerated Stress Test (HAST)	JESD22-A101 JESD22-A110	85°C/85%RH, max operating supplies or 110°C/85%RH, max operating supplies or 130°C/85%RH, max operating supplies
Unbiased Highly Accelerated Stress Test (UHAST)	JESD22-A118	110°C/85%RH or 130°C/85%RH

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3.0 QUALIFICATION DATA MACHXO3D PRODUCT FAMILY

The MachXO3D devices are fabricated at United Semiconductor Japan Corporation (USJC) on a 65nm non-volatile low power process, then assembled and tested at Advanced Semiconductor Engineering, Kaohsiung (ASEK). Table 3.0.1 shows the LUT densities, package and I/O options, along with other key parameters. The LCMXO3D-9400 is the lead qualification vehicle for this product family.

Product Family: MachXO3D
Package Offered: caBGA and QFN
Process Technology Node: 65nm

Table 3.0.1 MachXO3D Family Selection Guide

Features		MachXO3D-4300	MachXO3D-9400
LUTs		4300	9400
Distributed RAM (kbits)		34	73
EBR SRAM (kbits)		92	432
UFM (kbits)		367/1122[4]	1088/2693[4]
Number of PLLs		2	2
Hardened Functions	Security	1	1
	I²C	2	2
	SPI	1	1
	Timer/ Counter	1	1
	Oscillator	1	1
On-chip Dual-boot		Yes	Yes
I3C compatible I/O		Yes[1]	Yes[1]
MIPI D-PHY Support[2]		Yes	Yes
Core Vcc	2.5 – 3.3V	ZC/HC	ZC/HC
Temperature	Commercial	Yes	Yes
	Industrial	Yes	Yes
	Automotive	Yes[3]	No

Packages	I/O	
72 QFN (10 mm x 10 mm, 0.5 mm)	58 (HC/ZC)	58 (HC/ZC)
256-ball caBGA (14 mm x 14 mm, 0.8 mm)	206 (HC/ZC)	206 (HC/ZC)
400-ball caBGA (17 mm x 17 mm, 0.8 mm)	—	335 (HC/ZC)
484-ball caBGA (19 mm x 19 mm, 0.8 mm)	—	383 (HC)

Notes:
1. 4 pairs of I/O in bank 3 with I3C dynamic pull up capability.
2. HC device only.
3. ZC lowest speed grade device only.
4. When dual-boot is disabled, image space can be repurposed as extra UFM. Refer to Table 2.17 for more details.

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3.1 MachXO3D Product Family Life (HTOL) Data

High Temperature Operating Life (HTOL) Test

The High Temperature Operating Life test is used to accelerate thermally-activated failure mechanisms that would occur as a result of operating the device continuously in a system application. Consistent with JEDEC JESD22-A108 "Temperature, Bias, and Operating Life", a pattern specifically designed to exercise the maximum amount of circuitry is programmed into the device and this pattern is continuously exercised at 125°C junction temperature with a bias level at the maximum datasheet specification.

Life Test (HTOL) Conditions:

Devices Stressed: MachXO3D
Stress Duration: 168, 500, 1000, 2000 hours
Stress Temperature: $T_{JUNCTION}$ = ≥125°C
Stress Voltage: MachXO3D HTOL Pattern, Vcc=3.63V (HC/ZC), Vccio=3.63V
Stress Method: JESD22-A108F

Table 3.1.1 MachXO3D Product Family Life Results

Product Name	Lot #	Qty	500 Hrs Result	1000 Hrs Result	Cumulative Hours
LCMXO3D-9400HC	Lot #1	77	0	0	77,000
LCMXO3D-9400HC	Lot #2	77	0	0	77,000
LCMXO3D-9400HC	Lot #3	77	0	0	77,000
LCMXO3D-9400ZC	Lot #1	77	0	0	77,000
LCMXO3D-9400ZC	Lot #2	77	0	0	77,000
LCMXO3D-9400ZC	Lot #3	77	0	0	77,000

Cumulative Life Testing Device Hours = 462,000
Cumulative Result = 0 failures at 1000 hours
Long Term Failure Rate < 25 FIT
FIT Assumptions: CL=60%, AE=0.7eV, Tjref=55C

HTOL (1000 Hrs) Cumulative Result/Sample Size = 0 / 462

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3.2 MachXO3D Product Family Non-Volatile Cycling Endurance (NVCE) Data

Non-Volatile Cycling Endurance (NVCE)

The NVCE test evaluates the ability for Flash memory cells to survive repeated program and erase operations. Cycling is performed continuously and functionality is monitored at each program and erase operation. Testing is performed at both room temperature and hot temperature in order to target different failure mechanisms. In accordance with JEDEC and AEC test specifications, 50% of flash cells are cycled to the datasheet specified maximum cycles, while 50% of flash cells are cycled to 10% of the specified max cycles.

Units subjected to NVCE stress are then subjected to follow-on stresses: Low Temperature Data Retention (LTDR), Post-Cycle High Temperature Data Retention (PCHTDR), and Post-Cycle High Temperature Operating Life (PCHTOL), to ensure their continued retention and operation. See following sections for more details.

NVCE Conditions:

Devices Stressed: MachXO3D
Spec Max P/E Cycles: 10,000
Stress Duration: 50% of array: 1,000 Cycles; 50% of array: 10,000 Cycles
Temperature: 25°C, 85°C ambient (See Table)
Stress Voltage: V_{CC}=2.4V / V_{CCIO}=3.2V
Method: JESD47J.01, JESD22-A117A, AEC Q100-005D1

Table 3.2.1 MachXO3D Room Temperature NVCE Results

Product Name	Lot #	Qty	Temp (°C)	1,000 Cyc Result	10,000 Cyc Result
LCMXO3D-9400ZC	Lot #1	77	25	0	0
LCMXO3D-9400ZC	Lot #2	77	25	0	0
LCMXO3D-9400ZC	Lot #3	77	25	0	0

Table 3.2.2 MachXO3D Hot Temperature NVCE Results

Product Name	Lot #	Qty	Temp (°C)	1,000 Cyc Result	10,000 Cyc Result
LCMXO3D-9400HC	Lot #1	77	85	0	0
LCMXO3D-9400HC	Lot #2	77	85	0	0
LCMXO3D-9400HC	Lot #3	77	85	0	0
LCMXO3D-9400ZC	Lot #1	77	85	0	0
LCMXO3D-9400ZC	Lot #2	77	85	0	0
LCMXO3D-9400ZC	Lot #3	77	85	0	0

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3.3 MachXO3D Product Family Post-Cycle High Temperature Data Retention (PCHTDR) Data

Post-Cycle High Temperature Data Retention (PCHTDR)

The PCHTDR test evaluates the ability for Flash memory cells to retain their state during high-temperature, accelerated stress. Devices are unbiased during this retention stress. All units subjected to PCHTDR are first subjected to High-Temperature NVCE stress, as detailed previously. This cycling ensures that cells are adequately stressed to detect stress-induced leakage current (SILC), which could impact their retention lifetime.

PCHTDR Conditions:

Devices Stressed: MachXO3D
Stress Duration: 1000 hours
Temperature: 150°C ambient
Stress Voltage: Unbiased
Method: JESD47J.01, JESD22-A117A, AEC Q100-005D1

Table 3.3.1 MachXO3D PCHTDR Results

Product Name	Lot #	Qty	168 Hrs Result	500 Hrs Result	1000 Hrs Result
LCMXO3D-9400HC	Lot #1	77	0	0	0
LCMXO3D-9400HC	Lot #2	77	0	0	0
LCMXO3D-9400HC	Lot #3	77	0	0	0

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3.4 MachXO3D Product Family Low Temperature Data Retention (LTDR) Data

Low Temperature Data Retention (LTDR)

The LTDR test evaluates the ability for Flash memory cells to retain their state. Some forms of cell leakage may recover during high temperature retention stress (PCHTDR), driving the need for a low-temperature test to ensure adequate retention characteristics. Devices are unbiased during this retention stress. All units subjected to LTDR are first subjected to Room-Temperature NVCE stress, as detailed previously. This cycling ensures that cells are adequately stressed to detect stress-induced leakage current (SILC), which could impact their retention lifetime.

LTDR Conditions:

Devices Stressed: MachXO3D
Stress Duration: 1000 hours
Temperature: 25°C ambient
Stress Voltage: Unbiased
Method: JESD47J.01, AEC Q100-005D1

Table 3.4.1 MachXO3D LTDR Results

Product Name	Lot #	Qty	168 Hrs Result	500 Hrs Result	1000 Hrs Result
LCMXO3D-9400ZC	Lot #1	77	0	0	0
LCMXO3D-9400ZC	Lot #2	77	0	0	0
LCMXO3D-9400ZC	Lot #3	77	0	0	0

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3.5 MachXO3D Product Family Uncycled High Temperature Data Retention (UCHTDR) Data

Uncycled High Temperature Data Retention (UCHTDR)

The UCHTDR test evaluates the ability for uncycled Flash memory cells to retain their state during high-temperature accelerated testing. Devices are unbiased during this retention stress. This testing is intended to demonstrate a use-case where devices are infrequently programmed, but expected to retain their state for long durations.

UCHTDR Conditions:

Devices Stressed: MachXO3D
Stress Duration: 1000 hours
Temperature: 150°C ambient
Stress Voltage: Unbiased
Method: JESD47J.01, JESD22-A117A

This stress is performed simultaneously with HTSL by programming a worst-case pattern into the device prior to stress and verifying the contents upon completion. See Section 4.6 for applicable HTSL data.

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3.6 MachXO3D Product Family Post-Cycle High Temperature Operating Life (PCHTOL) Data

Post-Cycle High Temperature Operating Life (PCHTOL)

The PCHTOL test evaluates the electrical lifetime of the Flash memory block and supporting circuitry under accelerated temperature and bias conditions. During PCHTOL, a logic pattern is periodically read from the Flash memory and used to configure the device under test in order to simulate a representative use-case. Because of the logic downtime associated with this repeated configuration, stress testing of the Flash memory was separated from the primary HTOL test. All units subjected to PCHTOL are first subjected to High-Temperature NVCE stress, as detailed previously. This cycling ensures that cells and supporting circuitry are adequately stressed to to represent electrical lifetime.

PCHTOL Conditions:

Devices Stressed: MachXO3D
Stress Duration: 1000 hours
Temperature: ≥125°C junction
Stress Voltage: V_{CC}=3.63V / V_{CCIO}=3.63V, 2.75V (LVDS)
Method: AEC Q100-005D1, JESD22-A108F

Table 3.6.1 MachXO3D PCHTOL Results

Product Name	Lot #	Qty	500 Hrs Result	1000 Hrs Result
LCMXO3D-9400ZC	Lot #1	77	0	0
LCMXO3D-9400ZC	Lot #2	77	0	0
LCMXO3D-9400ZC	Lot #3	77	0	0

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3.7 MachXO3D Product Family – ESD and Latch-Up Data

Electrostatic Discharge-Human Body Model:

MachXO3D product family was tested per the JS-001 Electrostatic Discharge (ESD) Sensitivity Testing Human Body Model (HBM) procedure. All units were Class tested at room ambient prior to reliability stress and after reliability stress. No failures were observed within the passing classification.

Table 3.4.1 MachXO3D ESD-HBM Data

Product	Classification
LCMXO3D-9400HC	Class 1C
LCMXO3D-9400ZC	Class 1C
LCMXO3D-4300HC	Class 1C
LCMXO3D-4300ZC	Class 1C

HBM classification for Commercial/Industrial products, per JS-001-2017.
All HBM levels indicated are dual-polarity (±).

Electrostatic Discharge-Charged Device Model:

MachXO3D product family was tested per the JS-002, Field-Induced Charged-Device Model Test Method for Electrostatic-Discharge-Withstand Thresholds of Microelectronic Components procedure. All units were Class tested at room ambient prior to reliability stress and after reliability stress. No failures were observed within the passing classification.

Table 3.4.2 MachXO3D ESD-CDM Data

Product	Classification
LCMXO3D-9400HC	Class C3
LCMXO3D-9400ZC	Class C3
LCMXO3D-4300HC	Class C3
LCMXO3D-4300ZC	Class C3

CDM classification for Commercial/Industrial products, per JS-002-2018.
All CDM levels indicated are dual-polarity (±).

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Latch-Up:

MachXO3D product family was tested per the JEDEC EIA/JESD78 IC Latch-up Test procedure. All units were Class tested at room ambient prior to reliability stress and after reliability stress. No failures were observed within the passing classification.

Table 3.4.3 MachXO3D I/O Latch Up >100mA @ HOT (105°C) Data

Product	Classification
LCMXO3D-9400HC	> +/-100mA Class II
LCMXO3D-9400ZC	> +/-100mA Class II
LCMXO3D-4300HC	> +/-100mA Class II
LCMXO3D-4300ZC	> +/-100mA Class II

I-Test LU classification for Commercial/Industrial products, per JESD78E.
All IO-LU levels indicated are dual-polarity (±).

Table 3.4.4 MachXO3D Vcc Latch Up >1.5X @ HOT (105°C) Data

Product	Classification
LCMXO3D-9400HC	> 1.5x Vcc Class II
LCMXO3D-9400ZC	> 1.5x Vcc Class II
LCMXO3D-4300HC	> 1.5x Vcc Class II
LCMXO3D-4300ZC	> 1.5x Vcc Class II

Vsupply Over-voltage Test LU classification for Commercial/Industrial products, per JESD78E.

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4.0 PACKAGE QUALIFICATION DATA FOR MACHXO3D PRODUCT FAMILY

The MachXO3D Saw-singulated Chip Array BGA (caBGA) and Quad Flat No-leads (QFN) packages are assembled and tested at Advanced Semiconductor Engineering, Kaohsiung (ASEK). This report details the package qualification results of the various MachXO3D product introductions. Package qualification tests include Surface Mount Pre-Conditioning (SMPC), Temperature Cycling (TC), Unbiased HAST (uHAST), Temperature-Humidity Bias (THB) and High Temperature Storage Life (HTSL). Mechanical evaluation tests include Scanning Acoustic Tomography (SAT) and Visual Inspection (VI).

4.1 Family Qualifications

The generation and use of generic data applied across a package family emanating from one base assembly process is a Family Qualification, or Qualification-by-Similarity (QBS). For the package stresses THB, UHAST and HTSL, these are considered generic for a given Package Technology. Interactive effects of the silicon and package are addressed during qualification.

The following tables demonstrate the package stresses qualification matrix.

Table 4.1.1 Product-Package Qualification-By-Similarity (QBS) Matrix at ASEK

The LCMXO3D product/package combinations are Qualified-by-Similarity (QBS) using the qualification vehicles below.	**Stress Tests**	**Advanced Semiconductor Engineering, Kaohsiung (ASEK)**			
		caBGA (3)			**QFN**
		256 14x14mm 0.8mm pitch	**400 17x17mm 0.8mm pitch**	**484 19x19mm 0.8mm pitch**	**72 10x10mm**
LCMXO3D-9400	SMPC	MSL3	MSL3	MSL3	MSL3
	TC	700 cycles	700 cycles	700 cycles	700 cycles
	uHAST	264 hours	QBS (1)	QBS (1)	96 hours
	THB	1000 hours			1000 hours
	HTSL	1000 hours			1000 hours
LCMXO3D-4300 (4)	SMPC	QBS (1)	Package not offered	Package not offered	QBS (2)
	TC				
	uHAST				
	THB				
	HTSL				

(1) QBS to LCMXO3D-9400 BG256
(2) QBS to LCMXO3D-9400 SG72
(3) 256caBGA (PTH) is the lead caBGA qual vehicle and with worst die/package ratio. 400caBGA is the largest package using plated through hole (PTH) substrate design while 484caBGA is the largest package using blind via-on-pad substrate design
(4) Product-package offering, both with lower die/package ratio compared to LCMXO3D-9400 product-package combination

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4.2 Surface Mount Preconditioning (SMPC)

The SMPC Test is used to model the surface mount assembly conditions during component solder processing. This preconditioning is consistent with JEDEC JESD22-A113, "Preconditioning of Nonhermetic Surface Mount Devices Prior to Reliability Testing", Moisture Sensitivity Level 3 (MSL3) package moisture sensitivity and dry-pack storage requirements.

MSL3 Packages: caBGA and QFN
Surface Mount Preconditioning (MSL3): 5 Temperature Cycles; 24 hours Bake @ 125°C; 30°C/60% RH soak for 192 hours; 3X passes of reflow simulation performed before all[A] package stresses.
Method: J-STD-020E, JESD22-A113H

Table 4.2.1 SMPC Data

Product Name	Package	Assembly Site	Lot Number	Moisture Soak Level	3X Reflow Temperature	Quantity	# of Fails
LCMXO3D-9400ZC	256caBGA	ASEK	Lot #1	MSL3	260°C	308	0
LCMXO3D-9400ZC	256caBGA	ASEK	Lot #2	MSL3	260°C	308	0
LCMXO3D-9400ZC	256caBGA	ASEK	Lot #3	MSL3	260°C	308	0
LCMXO3D-4300ZC	256caBGA	ASEK	Lot #1	MSL3	260°C	308	0
LCMXO3D-4300ZC	256caBGA	ASEK	Lot #2	MSL3	260°C	308	0
LCMXO3D-4300ZC	256caBGA	ASEK	Lot #3	MSL3	260°C	308	0
LCMXO3D-9400ZC	400caBGA	ASEK	Lot #1	MSL3	260°C	77	0
LCMXO3D-9400ZC	400caBGA	ASEK	Lot #2	MSL3	260°C	77	0
LCMXO3D-9400ZC	400caBGA	ASEK	Lot #3	MSL3	260°C	77	0
LCMXO3D-9400HC	484caBGA	ASEK	Lot #1	MSL3	260°C	77	0
LCMXO3D-9400HC	484caBGA	ASEK	Lot #2	MSL3	260°C	77	0
LCMXO3D-9400HC	484caBGA	ASEK	Lot #3	MSL3	260°C	77	0
LCMXO3D-9400ZC	72QFN	ASEK	Lot #1	MSL3	260°C	308	0
LCMXO3D-9400ZC	72QFN	ASEK	Lot #2	MSL3	260°C	308	0
LCMXO3D-9400ZC	72QFN	ASEK	Lot #3	MSL3	260°C	308	0

[A]For parts intended for HTSL, preconditioning (minimum Bake + Reflow) is recommended only for wirebonded packages on Pb-free reflow profile.

Cumulative SMPC Failure Rate = 0 / 3,234

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4.3 Temperature Cycling (TC)

The TC test is used to accelerate mechanical fatigue failures resulting from differential thermal expansion of adjacent films, layers and metallurgical interfaces in the die and package with exposure to cyclical thermomechanical loading. Devices are tested at 25°C after exposure to repeated cycling between -55°C and +125°C in an air environment consistent with JEDEC JESD22-A104 "Temperature Cycling", Condition B temperature cycling requirements. Prior to Temperature Cycling testing, all devices are subjected to Surface Mount Preconditioning.

MSL3 Packages: caBGA and QFN
Stress Conditions: Temperature cycling between -55°C to 125°C
Stress Duration: 700 cycles
Method: JESD22-A104E, Condition B

Table 4.3.1 TC Data

Product Name	Package	Assembly Site	Lot Number	Stress Temperature	Stress Duration	Quantity	# of Fails
LCMXO3D-9400ZC	256caBGA	ASEK	Lot #1	-55°C to 125°C	700 cycles	77	0
LCMXO3D-9400ZC	256caBGA	ASEK	Lot #2	-55°C to 125°C	700 cycles	77	0
LCMXO3D-9400ZC	256caBGA	ASEK	Lot #3	-55°C to 125°C	700 cycles	77	0
LCMXO3D-4300ZC	256caBGA	ASEK	Lot #1	-55°C to 125°C	700 cycles	77	0
LCMXO3D-4300ZC	256caBGA	ASEK	Lot #2	-55°C to 125°C	700 cycles	77	0
LCMXO3D-4300ZC	256caBGA	ASEK	Lot #3	-55°C to 125°C	700 cycles	77	0
LCMXO3D-9400ZC	400caBGA	ASEK	Lot #1	-55°C to 125°C	700 cycles	77	0
LCMXO3D-9400ZC	400caBGA	ASEK	Lot #2	-55°C to 125°C	700 cycles	77	0
LCMXO3D-9400ZC	400caBGA	ASEK	Lot #3	-55°C to 125°C	700 cycles	77	0
LCMXO3D-9400HC	484caBGA	ASEK	Lot #1	-55°C to 125°C	700 cycles	77	0
LCMXO3D-9400HC	484caBGA	ASEK	Lot #2	-55°C to 125°C	700 cycles	77	0
LCMXO3D-9400HC	484caBGA	ASEK	Lot #3	-55°C to 125°C	700 cycles	77	0
LCMXO3D-9400ZC	72QFN	ASEK	Lot #1	-55°C to 125°C	700 cycles	77	0
LCMXO3D-9400ZC	72QFN	ASEK	Lot #2	-55°C to 125°C	700 cycles	77	0
LCMXO3D-9400ZC	72QFN	ASEK	Lot #3	-55°C to 125°C	700 cycles	77	0

Cumulative Temp Cycle Failure Rate = 0/1,155

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4.4 Unbiased Highly Accelerated Temperature/Humidity Stress Test (uHAST)

The uHAST test is used to accelerate galvanic or direct chemical corrosion mechanisms. Devices are subjected to temperature and humidity under pressure to highly accelerate penetration of moisture into the package and to the die surface. Consistent with JEDEC JESD22-A118, "Accelerated Moisture Resistance - Unbiased HAST," the unbiased HAST conditions are either 96 hours exposure at 130°C and 85% relative humidity, or 264 hours exposure at 110°C and 85% relative humidity. Prior to unbiased HAST testing, all devices are subjected to Surface Mount Preconditioning.

MSL3 Packages: caBGA and QFN
Stress Conditions: 110°C/85% RH (caBGA) or 130°C/85%RH (QFN)
Stress Duration: 264 hours (caBGA) or 96 hours (QFN)
Method: JESD22-A118B

Table 4.4.1 uHAST Data

Product Name	Package	Assembly Site	Lot Number	Stress Humidity	Stress Temperature	Stress Duration	Qty	# of Fails
LCMXO3D-9400ZC	256caBGA	ASEK	Lot #1	85% RH	110°C	264 hours	77	0
LCMXO3D-9400ZC	256caBGA	ASEK	Lot #2	85% RH	110°C	264 hours	77	0
LCMXO3D-9400ZC	256caBGA	ASEK	Lot #3	85% RH	110°C	264 hours	77	0
LCMXO3D-4300ZC	256caBGA	ASEK	Lot #1	85% RH	110°C	264 hours	77	0
LCMXO3D-4300ZC	256caBGA	ASEK	Lot #2	85% RH	110°C	264 hours	77	0
LCMXO3D-4300ZC	256caBGA	ASEK	Lot #3	85% RH	110°C	264 hours	77	0
LCMXO3D-9400ZC	72QFN	ASEK	Lot #1	85% RH	130°C	96 hours	77	0
LCMXO3D-9400ZC	72QFN	ASEK	Lot #2	85% RH	130°C	96 hours	77	0
LCMXO3D-9400ZC	72QFN	ASEK	Lot #3	85% RH	130°C	96 hours	77	0

Cumulative Unbiased HAST failure Rate = 0/693

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4.5 Steady State Humidity Bias Life Test (THB)

The THB test is used to accelerate galvanic, electrochemical or direct chemical corrosion mechanisms. Devices are subjected to temperature and humidity to accelerate penetration of moisture into the package and to the die surface. It additionally employs maximum differential bias on alternating pins to trigger a corrosion process. Consistent with JEDEC JESD22-A101, "Steady State Temperature Humidity Bias Life Test", devices are exposed for1000 hours at 85°C and 85% relative humidity with bias applied to the device. Prior to THB testing, all devices are subjected to Surface Mount Preconditioning.

MSL3 Packages: caBGA and QFN
Stress Conditions: Vcc/VccIO at MachXO3D max operating condition and 85°C/85% RH
Stress Duration: 1000 hours
Method: JESD22-A101D

Table 4.5.1 THB Data

Product Name	Package	Assembly Site	Lot Number	Stress Humidity	Stress Temperature	Stress Duration	Qty	# of Fails
LCMXO3D-9400ZC	256caBGA	ASEK	Lot #1	85% RH	85°C	1000 hours	77	0
LCMXO3D-9400ZC	256caBGA	ASEK	Lot #2	85% RH	85°C	1000 hours	77	0
LCMXO3D-9400ZC	256caBGA	ASEK	Lot #3	85% RH	85°C	1000 hours	77	0
LCMXO3D-4300ZC	256caBGA	ASEK	Lot #1	85% RH	85°C	1000 hours	77	0
LCMXO3D-4300ZC	256caBGA	ASEK	Lot #2	85% RH	85°C	1000 hours	77	0
LCMXO3D-4300ZC	256caBGA	ASEK	Lot #3	85% RH	85°C	1000 hours	77	0
LCMXO3D-9400ZC	72QFN	ASEK	Lot #1	85% RH	85°C	1000 hours	77	0
LCMXO3D-9400ZC	72QFN	ASEK	Lot #2	85% RH	85°C	1000 hours	77	0
LCMXO3D-9400ZC	72QFN	ASEK	Lot #3	85% RH	85°C	1000 hours	77	0

Cumulative THB 85-85 failure Rate = 0 / 693

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4.6 High Temperature Storage Life (HTSL)

The HTSL test is used to accelerate diffusion, oxidation, intermetallic growth, and chemical degradation of packaging components and determine its impact to product life. Consistent with JEDEC JESD22-A103, the devices are subjected to high temperature storage Condition B: +150 (-0/+10) °C for 1000 hours. Prior to High Temperature Storage, per JESD47, all wirebonded devices on Pb-free reflow profile are to be subjected to Surface Mount Preconditioning (moisture soak is optional).

MSL3 Packages: caBGA and QFN
Stress Duration: 1000 hours
Temperature: 150°C (ambient)
Method: JESD22-A103E

Table 4.6.1 HTSL Data

Product Name	Package	Assembly Site	Lot Number	Stress Temperature	Stress Duration	Qty	# of Fails
LCMXO3D-9400ZC	256caBGA	ASEK	Lot #1	150°C	1000 hours	77	0
LCMXO3D-9400ZC	256caBGA	ASEK	Lot #2	150°C	1000 hours	77	0
LCMXO3D-9400ZC	256caBGA	ASEK	Lot #3	150°C	1000 hours	77	0
LCMXO3D-4300ZC	256caBGA	ASEK	Lot #1	150°C	1000 hours	77	0
LCMXO3D-4300ZC	256caBGA	ASEK	Lot #2	150°C	1000 hours	77	0
LCMXO3D-4300ZC	256caBGA	ASEK	Lot #3	150°C	1000 hours	77	0
LCMXO3D-9400ZC	72QFN	ASEK	Lot #1	150°C	1000 hours	77	0
LCMXO3D-9400ZC	72QFN	ASEK	Lot #2	150°C	1000 hours	77	0
LCMXO3D-9400ZC	72QFN	ASEK	Lot #3	150°C	1000 hours	77	0

Cumulative HTSL failure Rate = 0/693

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5.0 MACHXO3D PROCESS WAFER LEVEL RELIABILITY (WLR)

Several key wafer fabrication process related parameters affect the Reliability of the End-Product. These parameters are tested during the Development Phase of the Technology. Passing data (a 10yr lifetime at the reliability junction temperature) must be obtained for three lots minimum for each parameter before release to production. These parameters are:

Hot Carrier Immunity (**HCI**): Effect is a reduction in transistor Idsat. Worst case is low temperature.
Time Dependent Dielectric Breakdown (**TDDB**): Transistor and capacitor oxide shorts or leakage.
Negative Bias Temperature Instability (**NBTI**): Symptom is a shift in Vth (also a reduction in Idsat).
Electromigration Lifetime (**EML**): Symptom is opens within, or shorts between, metal conductors.
Stress Migration (**SM**): Symptom is a void (open) in a metal Via due to microvoid coalescence.

Table 5.0.1 CS200F WLR Results

HCI

Device	LVN	LVP	MVN	MVP	HVN	HVP
delta Ids	-10%	-10%	-10%	-10%	-10%	-10%
Celsius	25	25	25	25	25	25
Vgstress	Vd/2	Vd	Vd/2	Vd	Vd/2	Vd
Vds	1.26	-1.26	3.465	-3.465	5.25	-5.25
0.1% TTF	3 lots>34yr DC	3 lots>71yr	3 lots>20yr AC	3 lots>684yr	3 lots >3.5e6 s DC*	3 lots >1e9 s DC*

TDDB

Device	LVN	LVP	MVN	MVP	HVN	HVP	Intermediate IMD	Semi-Global IMD
Celsius	100	100	100	100	100	100	100	100
Vg	1.26	-1.26	3.465	-3.465	5.25	-5.25	3.465	3.465
Max Area	2.2 cm^2	22 cm^2	1 cm^2	2.5 cm^2	5e-4 cm^2	5e-4 cm^2	L/S=100nm	L/S=200nm
0.1% TTF	3 lots>2.5e5 yr	3 lots>1.4e3 yr	3 lots>25yr	3 lots>390 yr	3 lots>1.2e3 yr	3 lots>20 yr	3 lots>229yr	3 lots>6690yr

NBTI

Device	LVP	MVP
delta Vth	50mv	100mv
Celsius	100	100
Vg	-1.26	-3.465
0.1% TTF	3 lots>5.8e5 yr	3 lots>4.2e3 yr

EML

Device	Intermediate	Semi-Global	Global	Top Al
Celsius	100	100	100	100
delta R	+5%	+5%	+5%	+5%
Jmax	6.65E+05	6.65E+05	6.65E+05	2.85E+05
0.1% TTF	3 lots>380 yr	3 lots>77 yr	3 lots>22 yr	3 lots>70yr

SM

Device	Intermediate	Semi-Global	Global
delta R	+100%	+100%	+100%
Celsius	100	100	100
0.1% TTF	3 lots>2400 yr	3 lots>328 yr	3 lots>1.1e4 yr

Note: Reliability life times are based on listed temperature and use conditions. A Detailed WLR report is available upon request. Lattice Semiconductor Corporation document 106883.

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6.0 MACHXO3D SOFT ERROR RATE DATA

Soft Error Rate (SER) testing is conducted to characterize the sensitivity of SRAM memory elements to Atmospheric Neutron and Alpha Particle radiation. Charge induced by the impact of these particles can collect at sensitive nodes in the device and result in changes to the internal states of the device. While these changes do not cause physical damage to the device, they can cause errors in device operation.

Neutron SER – The normalized upset rate of Configuration RAM and Embedded Block RAM (EBR) memories due to neutron events. During testing, devices were configured with a memory pattern, exposed to an accelerated neutron environment, and the memory was read back from the device. Upset bits were identified through pattern comparison. Neutron testing results are normalized to the standard neutron flux for New York City at sea level: 14 n/cm^2/hr. The SER is represented in Failures in Time per million bits (FIT/Mb) to allow for translation across different device families and densities.

Alpha Particle SER – The normalized upset rate of Configuration RAM and Embedded Block RAM (EBR) memories due to alpha particle events. During testing, devices were configured with a memory pattern, exposed to a calibrated alpha source (Am-241), and the memory was read back from the device. Upset bits were identified through pattern comparison. Alpha particle testing results are normalized to a standard flux for Ultra Low Alpha (ULA) packaging materials: 0.001 alpha/cm^2/hr. The SER is represented in Failures in Time per million bits (FIT/Mb) to allow for translation across different device families and densities.

Table 6.0.1 CS200F (65nm) SER

Particle Type	Memory	SER (FIT/Mb)
Neutron	Configuration RAM	241.6
	EBR	650.3
Alpha Particle	Configuration RAM	176.0
	EBR	462.5

Note: Detailed SER reports are available upon request.

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7.0 MACHXO3D ADDITIONAL FAMILY DATA

Table 7.0.1 MachXO3D Package Assembly Data

Package Attributes	LCMXO3D-9400			LCMXO3D-4300	LCMXO3D-9400	LCMXO3D-4300
Assembly Supplier	ASEKH					
Assembly Location	Kaohsiung, Taiwan					
Package Type	caBGA				QFN	
Package Code	BG484	BG400	BG256		SG72	
Package Body Size (mm)	19x19	17x17	14x14		10x10	
Ball/Lead count	484	400	256		72	
Package Thickness Max (mm)	1.45				0.9	
Package Volume (mm3)	523	419	284		90	
Peak Reflow Temperature (°C)	260					
Moisture Sensitivity Level	MSL3					
Wafer Tech	65nm					
Wafer Fab	United Semiconductor Japan Corporation					
Wafer Diameter (mm)	300					
Die Size (mm)	5.232x6.258			3.95x5.55	5.232x6.258	3.95x5.55
Die to Pkg Ratio	0.09	0.11	0.17	0.11	0.33	0.22
Scribe Width (um)	55x80					
Backgrind Thickness (mils)	8					
Wafer singulation Method	Laser Groove + Mech Saw					
Substrate Material	Core material: CCL-HL832NX(A-HS)				N/A	
Substrate Supplier	ASEE Shanghai					
Solder Mask	AUS320					
Number of layers	2					
Substrate thickness (mm)	0.282					
Power Planes, or Traces?	Traces					
Substrate Design	Via on Pad	PTH				
Leadframe Material	N/A				C194 CuAg	
Leadframe Finish					Roughened + Photo Plated	
Leadframe Supplier					Haesung DS	
Leadframe Thickness (mm)					0.2	
Package Singulation Method	Saw				Punch	
Die Attach Epoxy	Ablebond 2100A				Hitachi EN-4900F	
Bond Wire Type	CuPdAu+ (Au-PCC Plus)					
Bond Wire Diameter (mils)	0.8					
Bond Pad Pitch (um)	70					
Bond Pad Size (um)	50					
Probe-Only Pads Included?	Yes					
Mold cap Height (mm)	0.7				0.65	
Mold Compound Vendor	Kyocera				Sumitomo	
Mold Compound Type	G1250AHT				G631SB	
Low-Alpha Mold Compound?	Yes					
Halogen-Free Mold Compound?	Yes					
Ball Size (mm)	0.45				N/A	
Ball Pitch (mm)	0.8					
Ball Composition	SnAg3.0Cu0.5 (SAC305)					

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8.0 REVISION HISTORY

Table 8.0.1 MachXO3D Product Family Qualification Summary revisions

Date	Revision	Section	Change Summary
July 2020	A	---	Initial document release.

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