Crosslink Product Family Qualification Summary

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Dear Customer,

Enclosed is Lattice Semiconductor's Crosslink Product Family Qualification Summary Report.

This report was created to assist you in the decision making process of selecting and using our products. The information contained in this report represents the entire qualification effort for this device family.

The information is drawn from an extensive qualification program of the wafer technology and packaging assembly processes used to manufacture our products. The program adheres to JEDEC and Automotive Industry standards for qualification of the technology and device packaging. This program ensures you only receive product that meets the most demanding requirements for Quality and Reliability.

Your feedback is valuable to Lattice. If you have suggestions to improve this report, or the data included, we encourage you to contact your Lattice representative.

Sincerely,

James M. Orr
Vice President,
Corporate Quality
Lattice Semiconductor Corporation

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1.0 INTRODUCTION

CrossLink™ from Lattice Semiconductor is a programmable video bridging device that supports a variety of protocols and interfaces for mobile image sensors and displays. The device is based on Lattice mobile FPGA 40nm technology. It combines the extreme flexibility of an FPGA with the low power, low cost and small footprint of an ASIC.

CrossLink supports video interfaces including MIPI® DPI, MIPI DBI, CMOS camera and display interfaces, OpenLDI, FPD-Link, FLATLINK, MIPI D-PHY, MIPI CSI-2, MIPI DSI, SLVS200, SubLVDS, HiSPi and more. Lattice Semiconductor provides many pre-engineered IP (Intellectual Property) modules for CrossLink. By using these configurable soft core IPs as standardized blocks, designers are free to concentrate on the unique aspects of their design, increasing their productivity.

The Lattice Diamond® design software allows large complex designs to be efficiently implemented using CrossLink. Synthesis library support for CrossLink devices is available for popular logic synthesis tools. The Diamond tools use the synthesis tool output along with the constraints from its floor planning tools to place and route the design in the CrossLink device. The tools extract the timing from the routing and back-annotate it into the design for timing verification.

Interfaces on CrossLink provide a variety of bridging solutions for smart phone, tablets, wearables, VR, AR, Drone, Smart Home, HMI as well as adjacent ISM markets. The device is capable of supporting high-resolution, high-bandwidth content for mobile cameras and displays at 4k UHD and beyond.

Table 1.0.1 CrossLink Product Family Attributes

Device	**CrossLink**
LUTs	5936
sysMEM Blocks (9kb)	20
Embedded Memory (kb)	180
Distributed RAM Bits (kb)	47
General Purpose PLL	1
NVCM	Yes
Embedded I2C	2
Oscillator (10 KHz)	1
Oscillator (48 MHz)	1
Hardened MIPI D-PHY	2 [1,2]
Packages	**I/O**
36 WLCSP (2.5x25. mm2)	17
64ucfBGA (3.5x3.5 mm2)	29
80 ctfBGA (6.5x6.5 mm2)	36
81csfBGA (4.5x4.5 mm2)	37

Notes:

1. Additional D-PHY Rx interfaces are available using programmable I/O.
2. Only one Hardened D-PHY is available in 36 WLCSP package.

2.0 LATTICE PRODUCT QUALIFICATION PROGRAM

Lattice Semiconductor Corp. maintains a comprehensive reliability qualification program to assure that each product achieves its reliability goals. After initial qualification, the continued high reliability of Lattice products is assured through ongoing monitor programs as described in Lattice Semiconductor's Reliability Monitor Program Procedure (Doc. #70-101667). All product qualification plans are generated in conformance with Lattice Semiconductor's Qualification Procedure (Doc. #70-100164) with failure analysis performed in conformance with Lattice Semiconductor's Failure Analysis Procedure (Doc. #70-100166). Both documents are referenced in Lattice Semiconductor's Quality Assurance Manual, which can be obtained upon request from a Lattice Semiconductor sales office. Figure 2.0.1 shows the Product Qualification Process Flow.

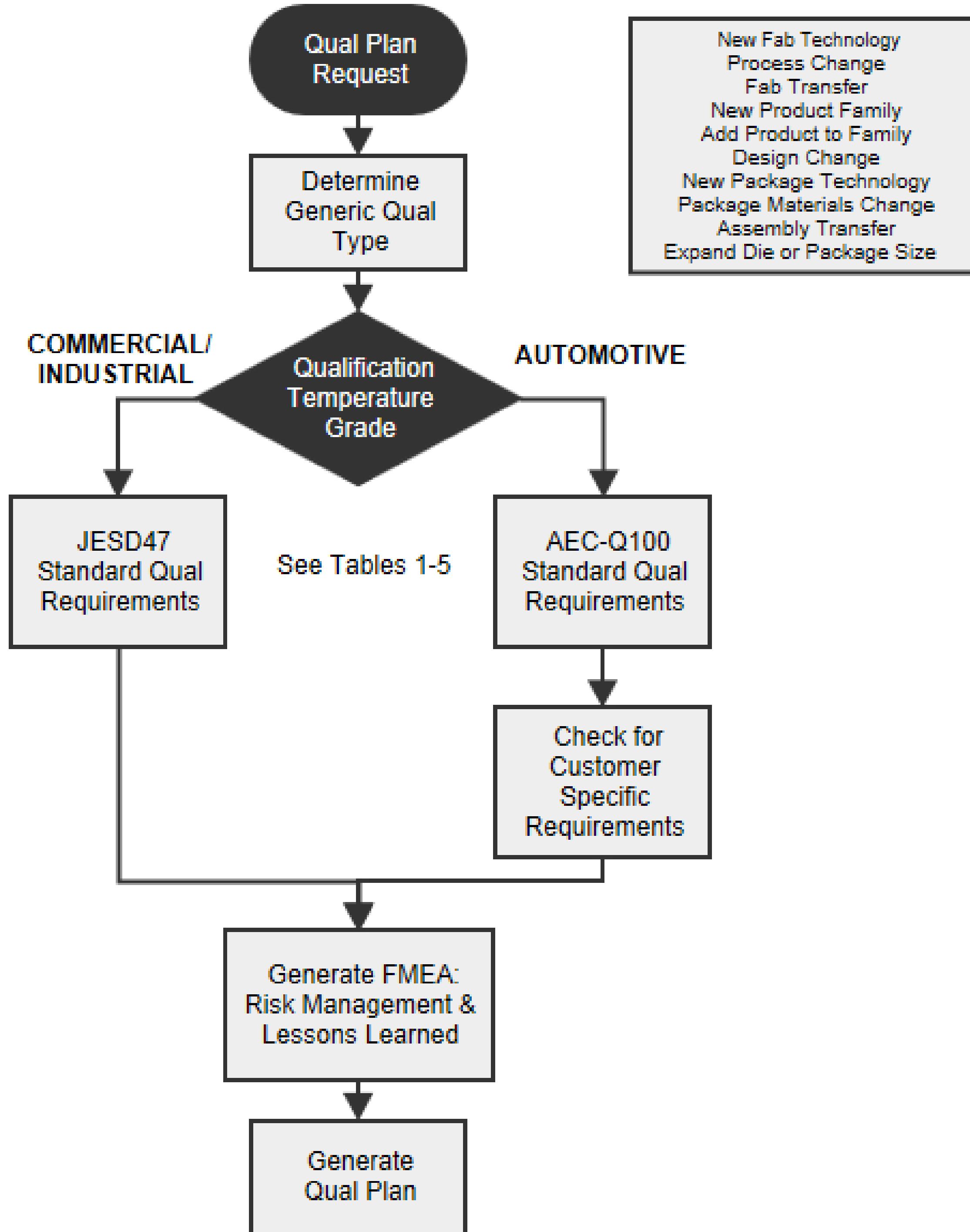
If failures occur during qualification, an 8D process is used to find root cause and eliminate the failure mode from the design, materials, or process. The effectiveness of any fix or change is validated through additional testing as required. Final testing results are reported in the qualification reports.

Product families are qualified based upon the requirements outlined in Table 2.0.1. In general, Lattice Semiconductor follows the current JEDEC Solid State Technology Association JESD47 Stress-Based Qualification testing methods. Package family qualification will include products with a wide range of circuit densities, package types, and package lead counts. Major changes to products, processes, or vendors require additional qualification before implementation in production.

Lattice Semiconductor maintains a regular reliability monitor program. The current Lattice Reliability Monitor Report can be found at Product Reliability Monitor Report.

Figure 2.0.1 Lattice Standard Product Qualification Process Flow

This diagram represents the standard qualification flow used by Lattice to qualify new Product Families. The target end market for the Product Family determines which flow options are used. The CrossLink Product Family was qualified using the Commercial / Industrial Qualification Option.



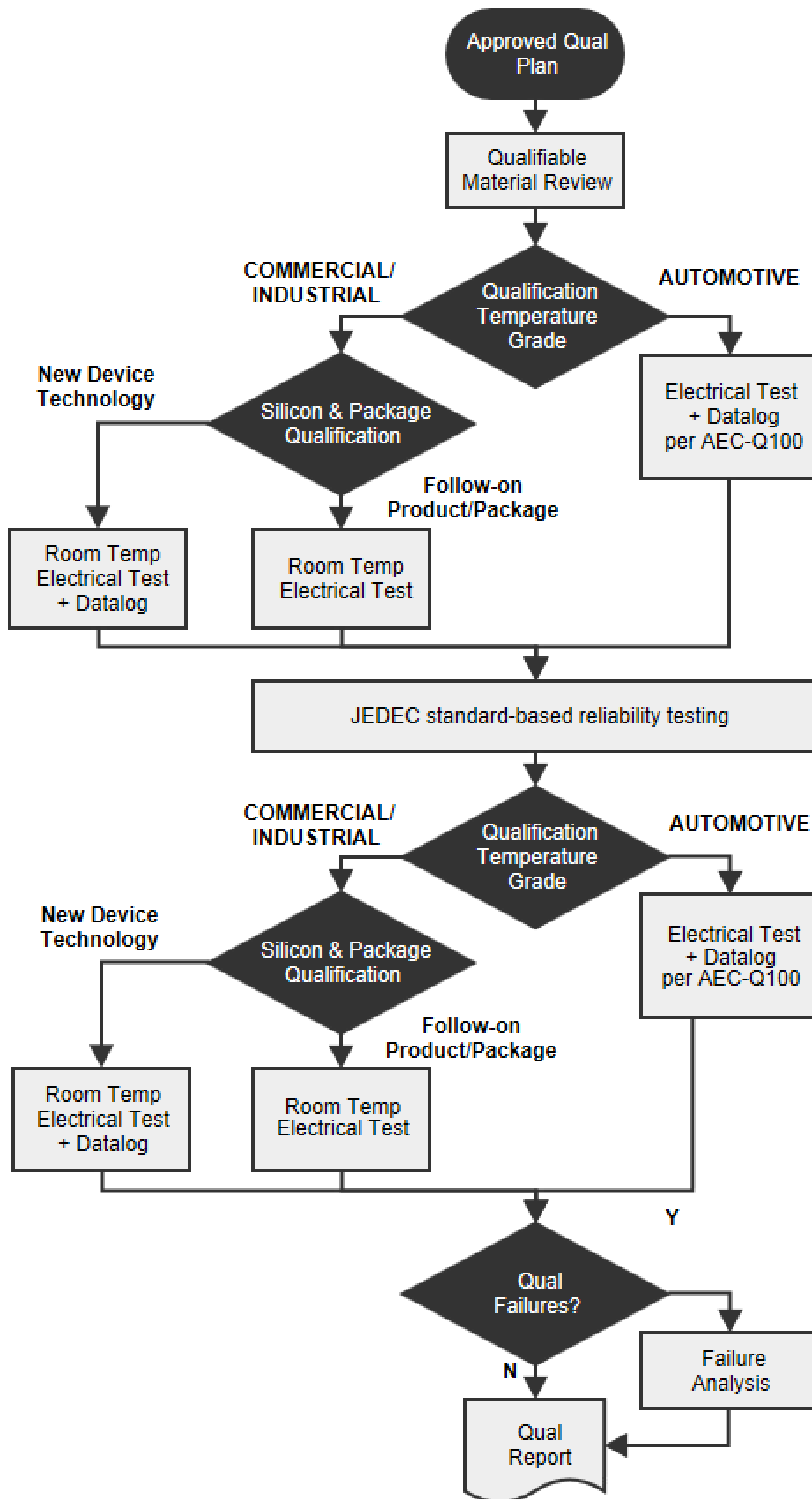

Approved Qual Plan
Qualifiable Material Review
COMMERCIAL/ INDUSTRIAL
Qualification Temperature Grade
AUTOMOTIVE
New Device Technology
Silicon & Package Qualification
Electrical Test + Datalog per AEC-Q100
Follow-on Product/Package
Room Temp Electrical Test + Datalog
Room Temp Electrical Test
JEDEC standard-based reliability testing
COMMERCIAL/ INDUSTRIAL
Qualification Temperature Grade
AUTOMOTIVE
New Device Technology
Silicon & Package Qualification
Electrical Test + Datalog per AEC-Q100
Follow-on Product/Package
Room Temp Electrical Test + Datalog
Room Temp Electrical Test
Y
Qual Failures?
N
Failure Analysis
Qual Report

Table 2.0.1 Qualification Tests for Components in Non-Hermetic Packages

TEST	STANDARD	TEST CONDITIONS
High Temperature Operating Life (HTOL)	JESD22-A108	≥125°C Tj and max operating supplies
Human Body Model ESD (HBM)	JS-001-2014	25°C (Technology/Device dependent Performance Targets)
Charged Device Model ESD (CDM)	JS-002-2014	25°C (Technology/Device dependent Performance Targets)
Latch-Up (LU)	JESD78	Class II, +/-100mA trigger current and AMR operating supplies
Accelerated Soft Error Testing (ASER)	JESD89	25°C, Nominal operating supplies
Surface Mount Pre-conditioning (SMPC)	IPC/JEDEC J-STD-020	Per appropriate MSL level per J-STD-020
High Temp Storage Life (HTSL)	JESD22-A103	Condition B
Temperature Cycling (TC)	JESD22-A104	Condition B, soak mode 2 (typical)
Temperature Humidity Bias, THB (85/85) or Biased HAST (HAST)	JESD22-A101 JESD22-A110	85°C, 85 % RH, max operating supplies or 110°C, 85 % RH, max operating supplies or 130°C, 85 % RH, max operating supplies
Unbiased Temperature/Humidity (UHAST)	JESD22-A118	110°C, 85 % RH or 130°C, 85 % RH

3.0 QUALIFICATION DATA CROSSLINK PRODUCT FAMILY

The Crosslink devices are fabricated at UMC based on Lattice mobile FPGA 40nm technology then assembled and tested at Advanced Semiconductor Engineering, Kaohsiung (ASET). The LIF-MD6000-MG81 is the lead product qualification vehicle for this family.

Product Family: LIF-MD6000

Packages offered: csfBGA

Process Technology Node: 40 nm

3.1 CrossLink Product Family Life (HTOL) Data

High Temperature Operating Life (HTOL) Test

The High Temperature Operating Life test is used to thermally accelerate those wear out and failure mechanisms that would occur as a result of operating the device continuously in a system application. Consistent with EIA/JESD22-A108E "Temperature, Bias, and Operating Life", a pattern specifically designed to exercise the maximum amount of circuitry is programmed into the device and this pattern is continuously exercised at specified voltages as described in test conditions for each device type.

CrossLink Life Test (HTOL) Conditions:

Stress Duration: 1000 hours

Stress Conditions: CrossLink: HTOL Pattern, Vcc=1.32V, Vccio=3.63V, $T_{JUNCTION}$ = $\geq$125°C

Method: EIA/JESD22-A108E

Table 3.1.1 CrossLink Product Family Life Results

Product Name	Foundry	Lot #	Qty	48 Hrs Result	168 Hrs Result	500 Hrs Result	1000 Hrs Result	Cumulative Hours
LIF-MD6000	UMC	1	100	N/A	0	0	0	100,000
LIF-MD6000	UMC	2	100	N/A	0	0	0	100,000
LIF-MD6000	UMC	3	100	N/A	0	0	0	100,000
LIF-MD6000	UMC	4	85	N/A	0	0	0	85,000
LIF-MD6000	UMC	5	85	N/A	0	0	0	85,000
LIF-MD6000	UMC	6	85	N/A	1[1]	0	0	84,000

*Vcc=1.32V (Absolute Maximum Rating for Vcc).

Crosslink HTOL Cumulative Result / Sample Size = 1 / 555
Crosslink Cumulative Life Testing Device Hours = 554,000
Crosslink Long Term Failure Rate < 50 FITs
Crosslink FIT Assumptions: CL=60%, Ea=0.7eV, Tjref=55C

[1] *FAR# 1631: 1 unit with marginal pin leakage failure

3.2 CrossLink Product Family – ESD and Latch UP Data

Electrostatic Discharge-Human Body Model

CrossLink product family was tested per the JS-001-2014 Electrostatic Discharge (ESD) Sensitivity Testing Human Body Model (HBM) procedure.

All units were Class tested at room ambient prior to reliability stress and after reliability stress. No failures were observed within the passing classification.

Table 3.2.1 CrossLink ESD-HBM Data

Product	64 ucfBGA (3.5.5x.3.5mm, 0.5mm pitch)	80 ctfBGA (6.5x6.5mm, 0.5mm pitch)	81 csfBGA (4.5x4.5mm, 0.5mm pitch)
LIF-MD6000	QBS	QBS	HBM>2kV Class 2

HBM classification for Commercial/Industrial products per JS-001-2014.
All HBM levels indicated are dual-polarity (±).
HBM worst-case performance is the package with the smallest RLC parasitics. All other packages for a given product are qualified-by-similarity (QBS).

Electrostatic Discharge-Charged Device Model:

CrossLink product family was tested per the JS-002-2014, Field-Induced Charged-Device Model Test Method for Electrostatic-Discharge-Withstand Thresholds of Microelectronic Components procedure.

All units were Class tested at room ambient prior to reliability stress and after reliability stress. No failures were observed within the passing classification.

Table 3.2.2 CrossLink ESD-CDM Data

Product	64 ucfBGA (3.5.5x.3.5mm, 0.5mm pitch)	80 ctfBGA (6.5x6.5mm, 0.5mm pitch)	81 csfBGA (4.5x4.5mm, 0.5mm pitch)
LIF-MD6000	QBS	QBS	CDM>1kV Class C3

CDM classification for Commercial/Industrial products, per EIA/JESD22-C101.
All CDM levels indicated are dual-polarity (±).
CDM worst-case performance is the package with the largest bulk capacitance. All other packages for a given product are qualified-by-similarity (QBS).

Latch-Up:

CrossLink product family was tested per the JESD78D IC Latch-up Test procedure.

All units were Class tested at room ambient prior to reliability stress and after reliability stress. No failures were observed within the passing classification.

Table 3.2.3 CrossLink I/O Latch Up >100mA @ HOT (105°C) Data

Product	64 ucfBGA (3.5.5x.3.5mm, 0.5mm pitch)	80 ctfBGA (6.5x6.5mm, 0.5mm pitch)	81 csfBGA (4.5x4.5mm, 0.5mm pitch)
LIF-MD6000	QBS	QBS	> +/-100mA Class II

I-Test LU classification for Commercial/Industrial products, per JESD78D.
All IO-LU levels indicated are dual-polarity (±).
IO-LU worst-case performance is the package with access to the most IOs. All other packages for a given product are qualified-by-similarity (QBS).

Table 3.2.4 CrossLink Vcc Latch Up >1.5X @ HOT (105°C) Data

Product	64 ucfBGA (3.5.5x.3.5mm, 0.5mm pitch)	80 ctfBGA (6.5x6.5mm, 0.5mm pitch)	81 csfBGA (4.5x4.5mm, 0.5mm pitch)
LIF-MD6000	QBS	QBS	> 1.5x Vcc Class II

Vsupply Over-voltage Test LU classification for Commercial/Industrial products, per JESD78D.
Vcc-LU worst-case performance is the package with access to the most individual power rails. All other packages for a given product are qualified-by-similarity (QBS).

4.0 PACKAGE QUALIFICATION DATA FOR CROSSLINK PRODUCT FAMILY

The CrossLink devices are assembled and tested at Advanced Semiconductor Engineering, Kaohsiung Taiwan (ASET). Package qualification tests include Surface Mount Pre-Conditioning (SMPC), Temperature Cycling (T/C), Biased HAST (BHAST), Unbiased HAST (UHAST) and High Temperature Storage (HTSL). Electrical test is performed pre- and post-stress. Mechanical evaluation tests include Scanning Acoustic Tomography (SAT) and Visual Package Inspection.

Table 4.0.1 Summary of Package Reliability Test Conditions and Results

Assembly Site	Test	Stress Conditions	Test Vehicle	Package Type	Lot Quantity	Cumulative Device Units/Hours/Cycles	# of Fails
ASET	SMPC	3x 260°C reflow	LIF-MD6000	81-csfBGA	6	1,628 units	0
				64-ucfBGA	Q4'17		
				80-ctfBGA	Q4'17		
				36-WLCSP	Q4'17		
ASET	TC	-55°C to 125°C	LIF-MD6000	81-csfBGA	6	441,000 cycles	0
				64-ucfBGA	Q4'17		
				80-ctfBGA	Q4'17		
				36-WLCSP	Q4'17		
ASET	BHAST	85%RH, 110°C, 264 hours	LIF-MD6000	81-csfBGA	6	140,184 hours	0
				64-ucfBGA	Q4'17		
				80-ctfBGA	Q4'17		
		85%RH, 130°C, 96 hours		36-WLCSP	Q4'17		
ASET	UHAST	85%RH, 110°C, 264 hours	LIF-MD6000	81-csfBGA	6	140,184 hours	0
				64-ucfBGA	Q4'17		
				80-ctfBGA	Q4'17		
		85%RH, 130°C, 96 hours		36-WLCSP	Q4'17		
ASET	HTSL	150°C, 1000 hours	LIF-MD6000	81-csfBGA	6	435,000 hours	0
				64-ucfBGA	Q4'17		
				80-ctfBGA	Q4'17		
				36-WLCSP	Q4'17		

4.1 Surface Mount Preconditioning Testing

The Surface Mount Preconditioning (SMPC) Test is used to model the surface mount assembly conditions during component solder processing. All devices stressed through High Temperature Storage, Temperature Cycling, Un-biased HAST and Biased HAST were preconditioned. This preconditioning is consistent with J-STD-020D and JEDEC JESD22-A113F "Preconditioning Procedures of Plastic Surface Mount Devices Prior to Reliability Testing".

Surface Mount Preconditioning (MSL3): (5cyc TC condition B, 24 hours bake @ 125°C; 30°C/60% RH soak for 192 hours; 3X passes of reflow simulation) performed before all package stresses.

MSL3 Packages: csfBGA

Method: J-STD-020D and JESD22-A113F

Table 4.1.1 Surface Mount Precondition Data

Product Name	Package	Assembly Site	Lot Number	Moisture Soak Level	3X Reflow Temperature	Quantity	# of Fails
LIF-MD6000	81-csfBGA	ASET	Lot #1	MSL3	260°C	400	0
LIF-MD6000	81-csfBGA	ASET	Lot #2	MSL3	260°C	400	0
LIF-MD6000	81-csfBGA	ASET	Lot #3	MSL3	260°C	400	0
LIF-MD6000	81-csfBGA	ASET	Lot #4	MSL3	260°C	276	0
LIF-MD6000	81-csfBGA	ASET	Lot #5	MSL3	260°C	276	0
LIF-MD6000	81-csfBGA	ASET	Lot #6	MSL3	260°C	276	0

Cumulative SMPC Failure Rate = 0 / 1,628

4.2 Temperature Cycling (TC)

The Temperature Cycling test is used to accelerate those failures resulting from mechanical stresses induced by differential thermal expansion of adjacent films, layers and metallurgical interfaces in the die and package. Devices are tested at 25°C after exposure to repeated cycling between -55°C and +125°C in an air environment consistent with JEDEC JESD22-A104D "Temperature Cycling", Condition B temperature cycling requirements. Prior to Temperature Cycling testing, all devices are subjected to Surface Mount Preconditioning.

MSL3 Packages: csfBGA

Stress Duration: 700 cycles, 1000cycles

Stress Conditions: Temperature cycling between -55°C to 125°C

Method: JESD22-A104D, Condition B

Table 4.2.1 Temperature Cycling Data

Product Name	Package	Assembly Site	Lot Number	Stress Temperature	1x Stress Duration	Quantity	# of Fails
LIF-MD6000	81-csfBGA	ASET	Lot #1	-55°C to 125°C	700 cycles	100	0
LIF-MD6000	81-csfBGA	ASET	Lot #2	-55°C to 125°C	700 cycles	100	0
LIF-MD6000	81-csfBGA	ASET	Lot #3	-55°C to 125°C	700 cycles	100	0
LIF-MD6000	81-csfBGA	ASET	Lot #4	-55°C to 125°C	1000 cycles	77	0
LIF-MD6000	81-csfBGA	ASET	Lot #5	-55°C to 125°C	1000 cycles	77	0
LIF-MD6000	81-csfBGA	ASET	Lot #6	-55°C to 125°C	1000 cycles	77	0

Cumulative Temp Cycle Failure Rate = 0 / 531
Cumulative Device Temp Cycles = 441,000

4.3 Biased HAST

Highly Accelerated Stress Test (HAST) testing uses both pressure and temperature to accelerate penetration of moisture into the package and to the die surface. The Biased HAST test is used to accelerate threshold shifts in the MOS device associated with moisture diffusion into the gate oxide region as well as electrochemical corrosion mechanisms within the device package. Consistent with JEDEC JESD22-A110E "Highly-Accelerated Temperature and Humidity Stress Test (HAST)", the biased HAST conditions are either 96 hours exposure at 130°C and 85% relative humidity, or 264 hours exposure at 110°C and 85% relative humidity. Prior to High Temperature Storage, all Pb-free wirebonded devices are subjected to Surface Mount Preconditioning.

MSL3 Packages: csfBGA

Stress Conditions: Vcc= Max operating condition, 110°C, and 85% RH

Stress Duration: 264 Hrs

Method: JESD22-A110E

Table 4.3.1 Biased HAST Data

Product Name	Package	Assembly Site	Lot Number	Stress Temperature	Stress Duration	Quantity	# of Fails
LIF-MD6000	81-csfBGA	ASET	Lot #1	110°C	264 Hrs	100	0
LIF-MD6000	81-csfBGA	ASET	Lot #2	110°C	264 Hrs	100	0
LIF-MD6000	81-csfBGA	ASET	Lot #3	110°C	264 Hrs	100	0
LIF-MD6000	81-csfBGA	ASET	Lot #4	110°C	264 Hrs	77	0
LIF-MD6000	81-csfBGA	ASET	Lot #5	110°C	264 Hrs	77	0
LIF-MD6000	81-csfBGA	ASET	Lot #6	110°C	264 Hrs	77	0

Cumulative BHAST failure Rate = 0/ 531
Cumulative BHAST device hours = 140,184

4.4 Unbiased HAST

Unbiased Highly Accelerated Stress Test (UHAST) testing uses both pressure and temperature to accelerate penetration of moisture into the package and to the die surface. The Unbiased HAST test is designed to detect ionic contaminants present within the package or on the die surface, which can cause chemical corrosion. Consistent with JESD22-A118B, "Accelerated Moisture Resistance - Unbiased HAST," the UHAST conditions are 264 hours exposure at 110°C and 85% relative humidity. Prior to Unbiased HAST testing, all devices are subjected to Surface Mount Preconditioning.

MSL3 Packages: csfBGA
Stress Conditions: 110°C, and 85% RH
Stress Duration: 264 Hrs
Method: JESD22-A118B

Table 4.4.1 Unbiased HAST Data

Product Name	Package	Assembly Site	Lot Number	Stress Temperature	Quantity	1x Stress Duration	# of Fails
LIF-MD6000	81-csfBGA	ASET	Lot #1	110°C	264 Hrs	100	0
LIF-MD6000	81-csfBGA	ASET	Lot #2	110°C	264 Hrs	100	0
LIF-MD6000	81-csfBGA	ASET	Lot #3	110°C	264 Hrs	100	0
LIF-MD6000	81-csfBGA	ASET	Lot #4	110°C	264 Hrs	77	0
LIF-MD6000	81-csfBGA	ASET	Lot #5	110°C	264 Hrs	77	0
LIF-MD6000	81-csfBGA	ASET	Lot #6	110°C	264 Hrs	77	0

Cumulative UHAST failure Rate = 0 / 531
Cumulative UHAST device hours = 140,184

4.5 High Temperature Storage Life

The High Temperature Storage Life test is used to determine the effect of time and temperature, under storage conditions, for thermally activated failure mechanisms. Consistent with JEDEC JESD22-A103D, the devices are subjected to high temperature storage Condition B: +150 (-0/+10) °C for 1000 hours. Prior to High Temperature Storage, all devices are subjected to Surface Mount Preconditioning.

MSL3 Packages: csfBGA
Stress Duration: 1000 hours
Temperature: 150°C (ambient)
Method: JESD22-A-103D

Table 4.5.1 High Temperature Storage Life Data

Product Name	Package	Assembly Site	Lot Number	Stress Temperature	Stress Duration	Quantity	# of Fails
LIF-MD6000	81-csfBGA	ASET	Lot #1	150°C	1000 Hrs	100	0
LIF-MD6000	81-csfBGA	ASET	Lot #2	150°C	1000 Hrs	100	0
LIF-MD6000	81-csfBGA	ASET	Lot #3	150°C	1000 Hrs	100	0
LIF-MD6000	81-csfBGA	ASET	Lot #4	150°C	1000 Hrs	45	0
LIF-MD6000	81-csfBGA	ASET	Lot #5	150°C	1000 Hrs	45	0
LIF-MD6000	81-csfBGA	ASET	Lot #6	150°C	1000 Hrs	45	0

Cumulative HTSL failure Rate = 0 / 435
Cumulative HTSL device hours = 435,000

5.0 ADDITIONAL PACKAGE FAMILY DATA

Table 5.0.1 CrossLink Product Family Bills of Material by Package Type and Assembly Site

Attributes	Saw-Singulated BGA
Assembly Site	ASET
Die Family (Product Line)	LIF-MD6000
Fabrication Process Technology	40nm
Package Type	csfBGA
Ball/Lead Counts	81
Bump Pitch	80um
BGA Ball Pitch	0.50um
Mold Compound Supplier/ID	EME-G311SA Type C
Cu Pillar	Sn 98.2/Ag 1.8
Lead Finish Plating or BGA Ball	SAC125

6.0 REVISION HISTORY

Table 6.0.1 CrossLink Product Family Qualification Summary Revisions

Date	Revision	Change Summary
June 2017	A	Initial document release covering LIF-MD6000-MG81

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