Single Event Upset (SEU) Report for MachXO2/MachXO3/MachXO3D

Technical Note

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Contents

Tables

Acronyms in This Document

A list of acronyms used in this document.

Acronym	Definition
CRAM	Configuration RAM
EBR	Embedded Block RAM
ECC	Error Correction Codes
FIT	Failures-in-Time
FPGA	Field-Programmable Gate Array
IP	Intellectual Property
SEC	Soft Error Correction
SED	Soft Error Detect
SEFI	Single Event Functional Interrupt
SER	Soft Error Rate
SEU	Single Event Upset
SRAM	Static Random Access Memory

1. Introduction

This document discusses Single Event Upsets (SEUs), a radiation effect that may be observed during normal operation for Lattice Semiconductor MachXO2™/MachXO3™/MachXO3D™ FPGAs. SEUs, often referred to as Soft Errors, occur when energetic particles interact with memory components, causing what is observed as a random bit flip.

SRAM is susceptible to SEU and requires characterization according to the JEDEC JESD89 set of standards. Lattice FPGAs typically use SRAM memory in two applications: the Logic Configuration RAM (Config; CRAM) and the User Memory (Embedded Block RAM; EBR).

This document provides Lattice's SEU characterization data for the above-mentioned FPGA families and types of memories, which can be used for estimating failure rates due to radiation effects.

Additionally, Lattice's FPGA architecture allows for significant failure derating, primarily due to unused routing resources within designs. Because of these redundant circuits, not all memory bits directly influence design functionality; those that do are known as *critical bits*. Derating guidelines based on critical bit analysis are provided for assessing the Single Event Functional Interrupt (SEFI) rate that is observed during field usage.

Finally, mitigation strategies offered by Lattice for handling SEUs are discussed.

2. Soft Error Rate Data for MachXO2/MachXO3/MachXO3D FPGA Families

Table 2.1 summarizes the SEU data collected for Lattice's 65 nm Flash process used for the MachXO2/MachXO3/MachXO3D families. The Soft Error Rate (SER) is represented in FIT, meaning the number of upset bits (failures) per billion device-hours. This rate is further normalized to FIT/Mbit of memory to allow for scaling across different devices with varying amounts of memory.

The data is divided by radiation and memory type to allow for use-case customization:

- Radiation Type
  - Neutron – Naturally occurring atmospheric neutrons are able to cause SEU. Results are scaled to the industry standard flux of NYC Sea-level (14 n/cm2/hr), and can be further scaled based on latitude, longitude, and altitude.
  - Alpha – Device packaging impurities may produce alpha particles as a decay product, which are able to cause SEU. Results are scaled for Ultra-Low Alpha mold compound flux (0.001 a/cm2/hr), and are considered use-case independent.
- SRAM Type
  - Config – Logic configuration memory for controlling FPGA function.
  - EBR – Embedded user memory.

Table 2.1. SEU Data for 65 nm FPGA

Technology	Radiation Type	SRAM Type	SER (FIT/Mbit)
CS200F 65 nm	Neutron	Config	241.6
		EBR	650.3
	Alpha	Config	176
		EBR	462.5

3. Functional Interrupt Rate

Understanding the field impact of SEU is critical for assessing risk and implementing mitigation strategies. The architecture of Lattice FPGAs allows for derating of the above upset rates:

- Config
  - User logic designs implemented on Lattice FPGAs rely on a small fraction of *critical bits* in the Config memory in order to continue operating properly. A sample of customer design is used to derive typical and worst-case critical bit ratios for assessing the risk of functional failure.
- EBR
  - Lattice FPGAs allow for the implementation of Error Correction Codes (ECC) into the user memory, which can detect and correct flipped bits, eliminating the functional impact of EBR SEU.

Combining these principles allow calculation of the expected field failure rate due to SEU, the SEFI Rate. Table 3.1 shows an example for the MachXO2 family.

Table 3.1. SEFI Rate by Device Density

Device	Config Memory Size (Mbit)	Typical[1] SEFI Rate (FIT)	Worst-Case[2] SEFI Rate (FIT)
LCMXO2-256	0.094	5.9	9.8
LCMXO2-640	0.191	12.0	19.9
LCMXO2-1200	0.360	22.6	37.6
LCMXO2-2000	0.534	33.4	55.7
LCMXO2-4000	0.972	60.9	101.5
LCMXO2-7000	1.534	96.1	160.1

Notes:

1. Typical designs range from 50-70% LUT Utilization based on sample benchmark designs.
2. Worst-Case designs range from 70-90% LUT Utilization based on sample benchmark designs.

4. Customer Down-Time Calculation

You can enable SED function to detect soft error events. SED scan happens in the background mode and the duration is variable but does not impact normal device functionality until SED error is detected.

Once SED error is detected, developers can arrange to flag the error to the system level or to reconfigure the FPGA. The MachXO2/MachXO3/MachXO3D families take from 0.6 ms to 5.2 ms to reconfigure the device depending on the density.

5. Soft Error Event and Repair Sequences

The SED feature detects errors that are inserted by SEI or actual soft bit errors. Depending on the available features of the FPGA family and the customer pattern architecture, the soft error correction (SEC) can be done off line, or while still running the customer pattern. The following sections discuss the SED and repair sequences for the MachXO2 and MachXO3 families.

The MachXO2/MachXO3/MachXO3D devices have a hardware implemented SED circuit, which is used to detect Config SRAM errors and allow them to be corrected. The on-chip error detection CRC circuitry allows you to perform these operations without any impact on the fitting or performance of the device.

The MachXO2/MachXO3/MachXO3D allows SED, and correction of soft errors require the part to be taken offline. The SED feature can be user controlled by the pattern implementation, or it can be one shot that executes upon first configuration. When a soft error is detected, the part can be reconfigured if desired by toggling the PROGRAMN pin low or issuing a REFRESH instruction. The SED run time is under 100 ms across the family, but will not add to the amount of time the device is offline. Reconfiguration will take 5.2 ms or less. Thus, the total offline time is less than a few milliseconds. For further details of hardware-based SRAM CRC Error Detect (SED) approach, refer to documents in the References section.

References

- MachXO2 SED Usage Guide (TN1206)
- MachXO3 SED/SEC Usage Guide (TN1292)
- MachXO3D SED/SEC Usage Guide (FPGA-TN-02124)

Technical Support Assistance

Submit a technical support case through www.latticesemi.com/techsupport.

Revision History

Revision 1.0, December 2019

Section	Change Summary
All	Initial release

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