

Introduction

The Power/Platform Management Device TrimCell DAC outputs are designed to interface with DC power supply circuits in order to fine-tune their output voltages. In most cases, this adjustment is made by gently influencing the feedback node of the DC power supply control circuit. This application note addresses typical concerns regarding DC power supply stability when connected to a Power/Platform Management Device TrimCell DAC output. Some typical concerns that arise when adding circuitry to the feedback node include the following: control-loop stability, output noise or ripple, and the settling time. This application note shows that the control-loop stability is not affected by the addition of the Power/Platform Management device trim circuitry.

Table 1. Applicable Power/Platform Management Device Summary

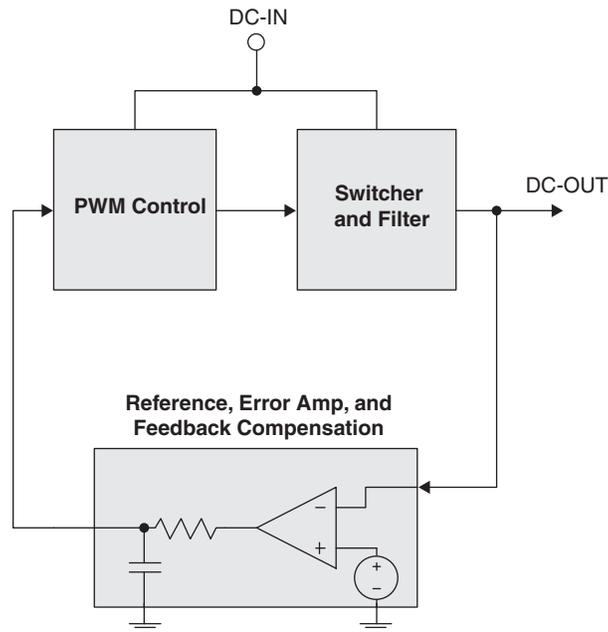
Device	VMONs	Digital Inputs	HVOUTs	Open Drain Outputs	Trim DAC Outputs	Digital I/O	CPLD Macrocells	FPGA LUTs
ispPAC-POWR6AT6	6	—	—	—	6	—	—	—
ispPAC-POWR1220AT8	12	6	4	16	8	—	48	—
LPTM10-1247	12	4	4	12	6	31	48	640
LPTM10-12107	12	4	4	12	8	91	48	640
LPTM21	10	—	4	10 ¹	4	95 ²	—	1280
L-ASC10	10	—	4	9 ¹	4	—	—	—

1. Platform Manager 2 Open Drain Outputs can be configured as inputs.
2. Platform Manager 2 Digital I/O count does not include SDA_M, SCL_M, or JTAGENB pins.

DC-DC Converter Control Theory

DC-DC power supplies are available in a wide range of voltage, amperage, power, and physical sizes. Regardless of the specific supply, all are based on the same type of power and control circuitry. Some form of pulse width modulation (PWM) is used to drive a switcher and filter circuit. The switcher filter circuitry usually consists of a power switch, an inductor, rectification, and filtering. The output voltage from the switcher converter circuitry is fed back around to control the PWM circuitry. The feedback loop includes a reference, error amplifier, and feedback compensation as shown in Figure 1. One of the design objectives of the control loop is to have ample phase and gain margins to provide stable operation over a wide range of conditions. Proper design of the control loop not only affects the stability but also transient response time and the noise level (the AC component of the DC output).

Figure 1. Simplified Block Diagram of DC-DC Converter Circuit

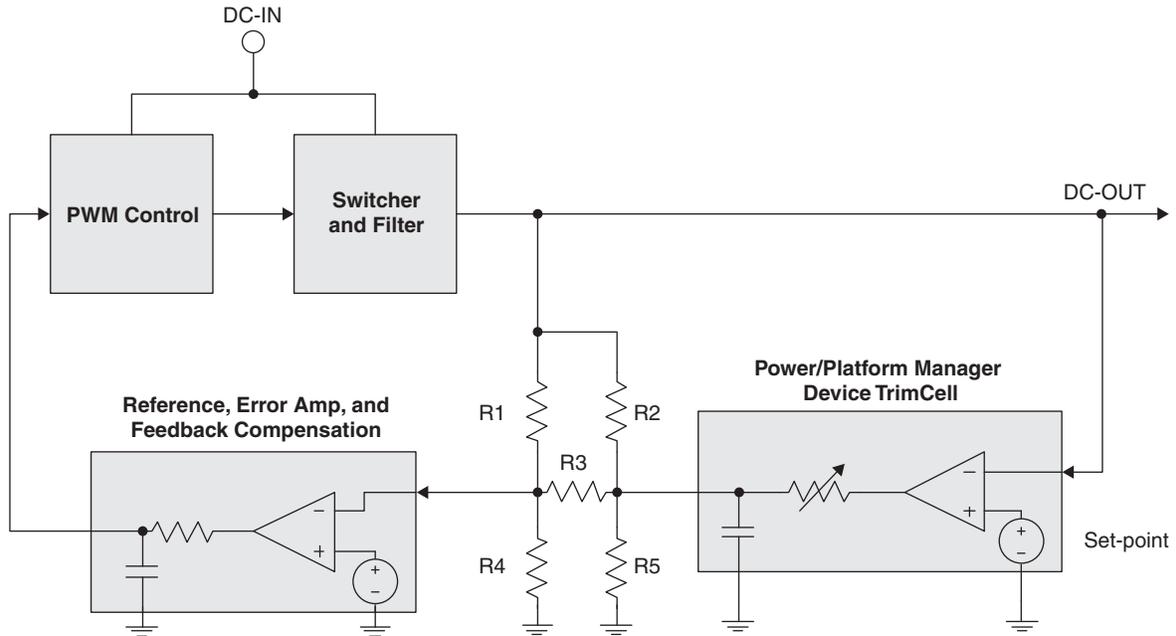


Power/Platform Management Device TrimCell Function

The Power/Platform Management device closed loop trim feature is needed in systems utilizing inexpensive DC-DC converters to improve the accuracy of their output voltage. The ability of these devices to trim several different supplies at once also decreases the cost but increases the accuracy of the entire system.

In Figure 2, a block diagram of the device TrimCell is shown with the block diagram of a generic DC-DC converter. The output of the DC-DC converter is monitored by the device VMON input and compared with the setpoint in the TrimCell; the difference between the two, results in an error signal. This error signal is filtered and injected into the summing node of the DC-DC converter using an interface circuit (shown using R1-R5). The actual interface circuit between the TrimCell output and the DC-DC converter trim pin depends on the actual converter and the range of adjustment and generally uses only one to three resistors. The Power/Platform Management design tool (Platform Designer or PAC-Designer, depending on device generation) calculates the resistor value and displays the interface configuration for a given DC-DC converter and the desired range of trim. The TrimCell DAC output current is limited to only $\pm 200 \mu\text{A}$ to prevent overdriving DC-DC trim pins. Furthermore, the programmable low-pass filter that is implemented within the TrimCell is significantly slower than the filter of the DC-DC converter. The TrimCell filter consists of a programmable DAC update delay that will be discussed in more detail in the next section. In the frequency domain the two feedback loops are in parallel and not in series. Thus, the DC-DC loop can still respond to transients in load or supply with little or no change to its specified performance. Meanwhile, the slower TrimCell loop adjusts for static offsets such as the DC-DC reference value, voltage drop from PC-board traces and/or connectors.

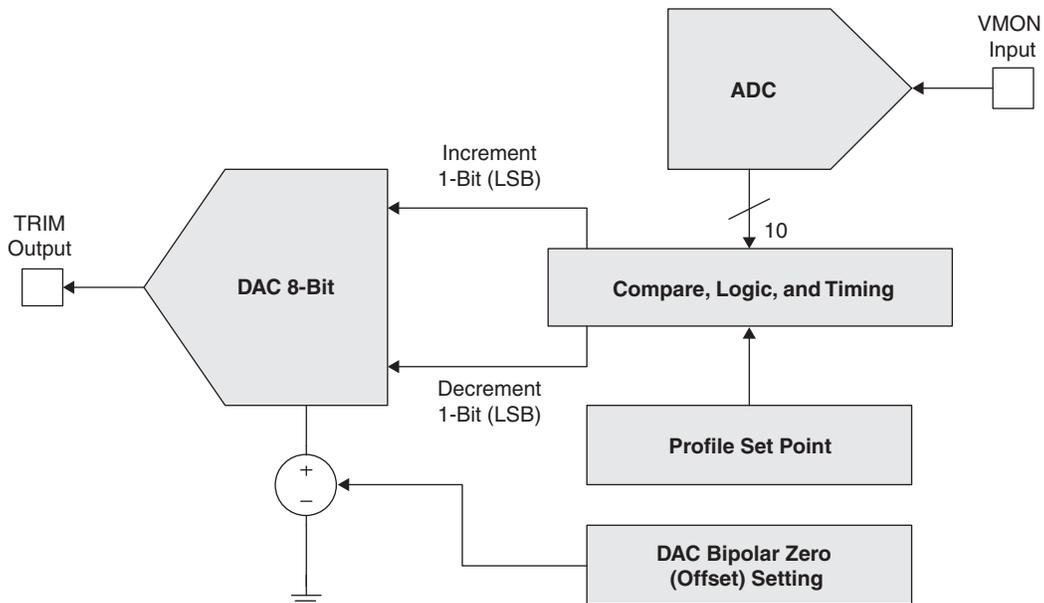
Figure 2. Block Diagram of DC-DC Converter with Power/Platform Management Device TrimCell



Details of the TrimCell

In reality, the device TrimCell and circuitry is significantly more complex than shown in Figure 2. Within the Power/Platform Management devices, the output of the DC-DC converter is digitized with an ADC. During a trim cycle (programmable to different intervals depending on device) this digital value is compared to a set-point that is stored in the device. The comparison results in either incrementing or decrementing the DAC by one LSB depending upon the error. If the DC-DC converter output voltage is equal to the set-point, the DAC is left unaltered (see Figure 3).

Figure 3. Block Diagram of Power/Platform Management Device TrimCell



The cycle time of the Power Manager closed loop trim circuitry updates the trim DAC at a rate that in most cases is an order of magnitude or two slower than the loop response time of the DC-DC converter that it is trimming.

The update delay for the closed loop trim for the Power/Platform Management device is set in the design tools. The applicable design tool and available settings per device tool are listed below:

- PAC-Designer (See Figure 4)
 - Devices Supported
 - ispPAC-POWR6AT6
 - ispPAC-POWR1220AT8
 - LPTM10-1247
 - LPTM10-12107
 - Available Update Delay Settings
 - 580 μ s, 1.5 ms, 9.2 ms, 18.5 ms
- Platform Designer (See Figure 5)
 - Devices Supported
 - LPTM21
 - L-ASC10
 - Available Update Delay Settings
 - 860 μ s, 1.72 ms, 13.8 ms, 27.6 ms

Since this delay time is for a single DAC update cycle of one LSB the total number of cycles required to reach a static operation may range from 1 to 128. This further emphasizes the low frequency adjustment of the trim process.

Figure 4. PAC-Designer Dialog for Setting ispPAC-POWR1220AT8 Update Delay

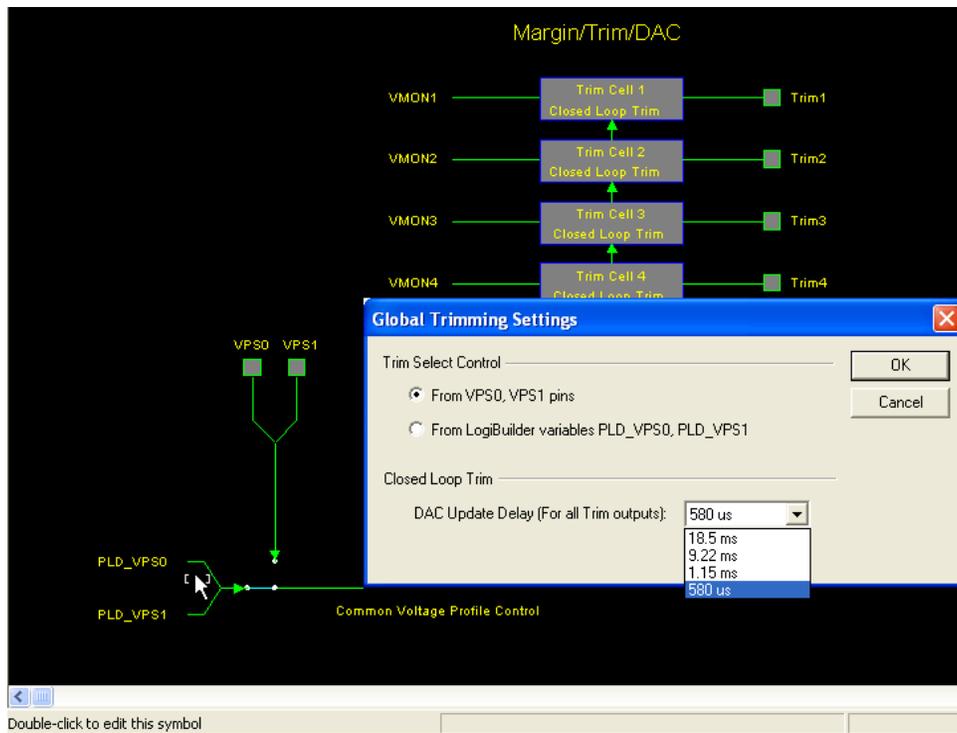
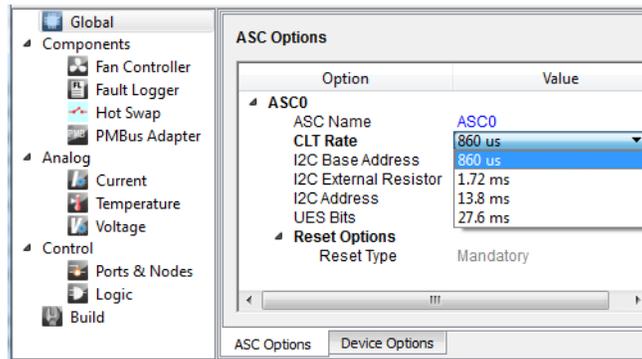


Figure 5. Platform Designer Dialog for Setting L-ASC10 Update Delay



Layout Tips

In an ideal layout the load, the DC-DC converter, the Power/Platform Management device, and the interface circuit would all be located close to each other to minimize voltage drop and noise pick-up. Generally, one should concentrate on keeping the interface circuit (R1-R5 in Figure 2) as close to the DC-DC converter trim pin as possible.

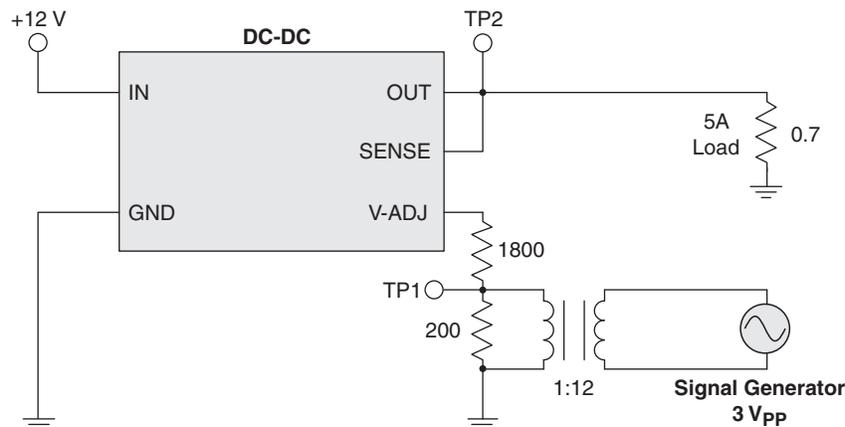
Measuring Loop Stability

In this section we look at gain and phase margins as related to DC-DC control loops and stability. Actual bench measurements on a state of the art DC-DC converter are presented in a Bode plot both with and without the Power/Platform Management device TrimCell. (The ispPAC-POWR1220AT8 device was used for these measurements. The results can be applied to all devices in the Power/Platform Management family).

For stable operation two conditions are generally accepted, which are when the gain is near zero dB and when the phase is near 180 degrees. The gain margin is the gain below zero dB when the phase is 180 degrees. A good gain margin is around -20dB. The phase margin is the absolute difference in the phase from 180 degrees when the gain is at zero dB. A good phase margin is about 45 degrees.

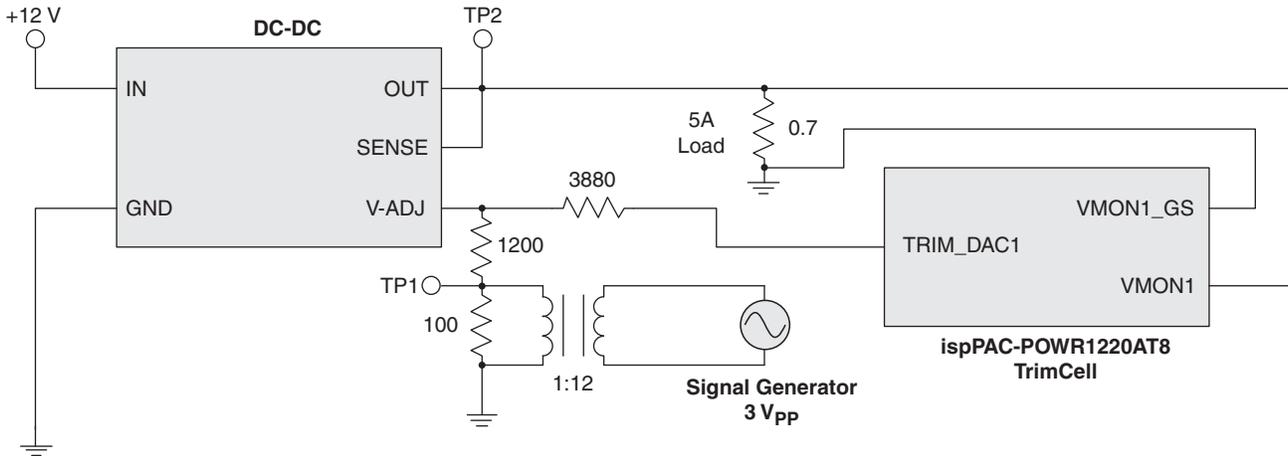
In Figure 6, the test points TP1 and TP2 are connected to an oscilloscope to measure gain and phase data as a function of frequency. A small audio transformer steps the signal generator output down to a small disturbance that is injected into the DC-DC control loop.

Figure 6. Measuring the Phase and Gain of a DC-DC Converter



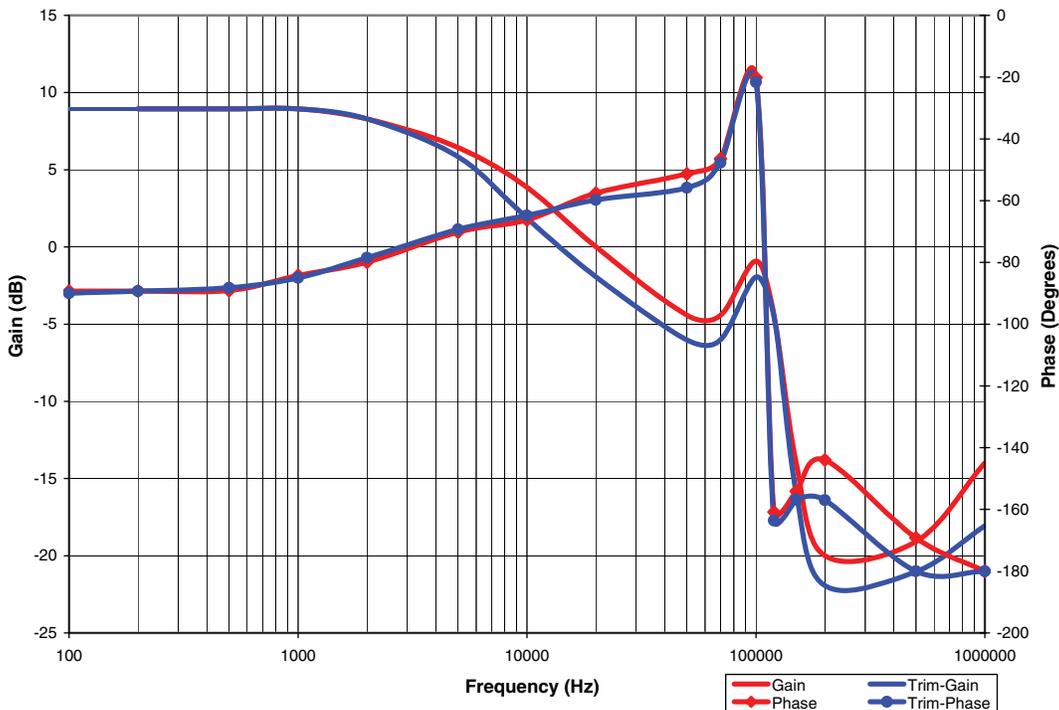
The circuit in Figure 7 is used to measure the gain and phase of the system with the ispPAC-POWR1220AT8 Trim-Cell adjusting the DC-DC converter. The closed loop trim was set to update at 580 μ s with a target voltage of 3.3 V. The bipolar offset was set at 0.6 V and the programming resistor network was changed to keep the same output voltage. The VMON sense wires were placed close to the load bank to compensate for line loss (I-R voltage drop).

Figure 7. Measuring the Phase and Gain of a Trimmed DC-DC Converter



The plot in Figure 8 clearly shows that the before and after measurements are essentially the same (or at least within measurement error) and the transfer function of the DC-DC control loop remains unchanged by the addition of the TrimCell to fine tune the voltage. Since the transfer function remains unchanged, the gain margin, phase margin, and transient response also remain unchanged by the addition of the TrimCell.

Figure 8. Gain and Phase Plot for DC-DC Converter with and without TrimCell



Design Examples

The following examples are based on real world state-of-the-art DC-DC converters.

Example 1

In this example we assume that the only timing information we have available on the DC-DC converter is the switching frequency and not the transient response from the data sheet. A typical switching frequency for small compact DC-DC converters is 400 kHz. The control loop for this converter would be designed to adjust the duty cycle over several periods (in order to be stable by itself). A typical adjustment happens over around 10 cycles. Thus, it would take 25 μ s to recover from a transient such as the load shifting from idle to half of full. In this case, the fastest DAC Update Delay (580 μ s in Power Manager II and Platform Manager devices, 860 μ s in LPTM21 and L-ASC10 devices) is at least 23 times slower than the DC-DC control loop. Clearly not fast enough to upset the stability of the DC-DC control loop. Even if it took 20 cycles or 50 μ s for the DC-DC to recover from a step function, the Power/Platform Manager Closed Loop Trim would still be 10 times too slow to cause any stability issues.

Example 2

From the data sheet of a reputable DC-DC supplier, the “Dynamic Characteristics” section has a typical specification for “Settling Time” of 200 μ s. This larger eighth-brick supply has a much slower control loop and thus the minimum DAC Update Delay of 580 μ s or 860 μ s might be cutting it too close. The next slower setting of 1.15 ms or 1.72 ms would provide ample safety margin to insure stable operation.

Summary

This application note has explored both theory and operation of Power/Platform Management device closed loop trimming of DC-DC converters with respect to stable operation. It has been shown with design examples that the closed loop trim delay is significantly slower than the loop response time of typical DC-DC converters. This application note has shown that the transfer function of a high performance DC-DC converter is virtually unchanged when the closed loop trim is enabled. Therefore, it can be concluded that a DC-DC converter output voltage accuracy can be increased when the closed loop trim feature of a Power/Platform Management TrimCell is used without altering its original stability and performance specifications.

Related Literature

- DS1015, [ispPAC-POWR1220AT8 Data Sheet](#)
- DS1016, [ispPAC-POWR6AT6 Data Sheet](#)
- DS1036, [Platform Manager Data Sheet](#)
- DS1043, [Platform Manager 2 Data Sheet](#)
- DS1042, [L-ASC10 Data Sheet](#)

Technical Support Assistance

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Revision History

Date	Version	Change Summary
October 2014	1.1	Updated to include Platform Manager devices.
		Changed document title from “Stable Operation of DC-DC Converters with Power Manager Closed Loop Trim” to “Stable Operation of DC-DC Converters with Power/Platform Management Devices Closed Loop Trim.”
		Updated Related Literature section.
		Updated Technical Support Assistance information.
December 2007	01.0	Initial release.