Introduction

The LatticeXP2™ sysIO™ buffers give the designer the ability to easily interface with other devices using advanced system I/O standards. This technical note describes the sysIO standards available and how they can be implemented using Lattice’s ispLEVER® design software.

sysIO Buffer Overview

The LatticeXP2 sysIO interface contains multiple Programmable I/O Cells (PIC) blocks. Each PIC contains two Programmable I/Os (PIO), PIOA and PIOB, connected to their respective sysIO Buffers. Two adjacent PIOs can be joined to provide a differential I/O pair (labeled as “T” and “C”).

Each Programmable I/O (PIO) includes a sysIO Buffer and I/O Logic (IOLOGIC). The LatticeXP2 sysIO buffers supports a variety of single-ended and differential signaling standards. The sysIO buffer also supports the DQS strobe signal that is required for interfacing with the DDR memory. One of every 16/18 PIOs in the LatticeXP2 contains a delay element to facilitate the generation of DQS signals. The DQS signal from the bus is used to strobe the DDR data from the memory into input register blocks. For more information on the architecture of the sysIO buffer please refer to the LatticeXP2 Family Data Sheet.

The IOLOGIC includes input, output and tristate registers that implement both single data rate (SDR) and double data rate (DDR) applications along with the necessary clock and data selection logic. Programmable delay lines and dedicated logic within the IOLOGIC are used to provide the required shift to incoming clock and data signals and the delay required by DQS inputs in DDR memory. The DDR implementation in the IOLOGIC and the DDR memory interface support are discussed in more detail in TN1138, LatticeXP2 High Speed I/O Interface.

Supported sysIO Standards

The LatticeXP2 sysIO buffer supports both single-ended and differential standards. Single-ended standards can be further subdivided into internally ratioed standard such as LVCMOS, LVTTL and PCI; and externally referenced standards such as HSTL and SSTL. The buffers support the LVTTL, LVCMOS 1.2, 1.5, 1.8, 2.5 and 3.3V standards. In the LVCMOS and LVTTL modes, the buffer has individually configurable options for drive strength, bus maintenance (weak pull-up, weak pull-down, or a bus-keeper latch). Other single-ended standards supported include SSTL and HSTL. Differential standards supported include MLVDS, LVDS, SRLS, BLVDS, LVPECL, differential SSTL and differential HSTL. Tables 1 and 2 list the sysIO standards supported in LatticeXP2 devices.

Table 8-1. Supported Input Standards

<table>
<thead>
<tr>
<th>Input Standard</th>
<th>V_REF (Nom.)</th>
<th>V_CCIO (Nom.)</th>
</tr>
</thead>
<tbody>
<tr>
<td>Single Ended Interfaces</td>
<td></td>
<td></td>
</tr>
<tr>
<td>LVTTL</td>
<td>—</td>
<td>—</td>
</tr>
<tr>
<td>LVCMOS33</td>
<td>—</td>
<td>—</td>
</tr>
<tr>
<td>LVCMOS25</td>
<td>—</td>
<td>—</td>
</tr>
<tr>
<td>LVCMOS18</td>
<td>—</td>
<td>1.8</td>
</tr>
<tr>
<td>LVCMOS15</td>
<td>—</td>
<td>1.5</td>
</tr>
<tr>
<td>LVCMOS12</td>
<td>—</td>
<td>—</td>
</tr>
<tr>
<td>PCI 33</td>
<td>—</td>
<td>3.3</td>
</tr>
<tr>
<td>HSTL18 Class I, II</td>
<td>0.9</td>
<td>—</td>
</tr>
<tr>
<td>HSTL15 Class I</td>
<td>0.75</td>
<td>—</td>
</tr>
<tr>
<td>SSTL3 Class I, II</td>
<td>1.5</td>
<td>—</td>
</tr>
</tbody>
</table>
### Table 8-1. Supported Input Standards (Continued)

<table>
<thead>
<tr>
<th>Input Standard</th>
<th>V_{REF} (Nom.)</th>
<th>V_{CCIO} (Nom.)</th>
</tr>
</thead>
<tbody>
<tr>
<td>SSTL2 Class I, II</td>
<td>1.25</td>
<td>—</td>
</tr>
<tr>
<td>SSTL18 Class I, II</td>
<td>0.9</td>
<td>—</td>
</tr>
</tbody>
</table>

#### Differential Interfaces

<table>
<thead>
<tr>
<th>Differential Interfaces</th>
<th>V_{CCIO} (Nom.)</th>
</tr>
</thead>
<tbody>
<tr>
<td>Differential SSTL18 Class I, II</td>
<td>—</td>
</tr>
<tr>
<td>Differential SSTL2 Class I, II</td>
<td>—</td>
</tr>
<tr>
<td>Differential SSTL3 Class I, II</td>
<td>—</td>
</tr>
<tr>
<td>Differential HSTL15 Class I</td>
<td>—</td>
</tr>
<tr>
<td>Differential HSTL18 Class I, II</td>
<td>—</td>
</tr>
<tr>
<td>LVDS, MLVDS, LVPECL, BLVDS, RSDS</td>
<td>—</td>
</tr>
</tbody>
</table>

1. When not specified, V_{CCIO} can be set anywhere in the valid operating range.

### Table 8-2. Supported Output Standards

<table>
<thead>
<tr>
<th>Output Standard</th>
<th>Drive</th>
<th>V_{CCIO} (Nom.)</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>Single-ended Interfaces</strong></td>
<td></td>
<td></td>
</tr>
<tr>
<td>LVTTL</td>
<td>4mA, 8mA, 12mA, 16mA, 20mA</td>
<td>3.3</td>
</tr>
<tr>
<td>LVTTL, Open Drain</td>
<td>4mA, 8mA, 12mA, 16mA, 20mA</td>
<td>—</td>
</tr>
<tr>
<td>LVCMOS33</td>
<td>4mA, 8mA, 12mA, 16mA, 20mA</td>
<td>3.3</td>
</tr>
<tr>
<td>LVCMOS25</td>
<td>4mA, 8mA, 12mA, 16mA, 20mA</td>
<td>2.5</td>
</tr>
<tr>
<td>LVCMOS18</td>
<td>4mA, 8mA, 12mA, 16mA</td>
<td>1.8</td>
</tr>
<tr>
<td>LVCMOS15</td>
<td>4mA, 8mA</td>
<td>1.5</td>
</tr>
<tr>
<td>LVCMOS12</td>
<td>2mA, 6mA</td>
<td>1.2</td>
</tr>
<tr>
<td>LVCMOS33, Open Drain</td>
<td>4mA, 8mA, 12mA, 16mA, 20mA</td>
<td>—</td>
</tr>
<tr>
<td>LVCMOS25, Open Drain</td>
<td>4mA, 8mA, 12mA, 16mA, 20mA</td>
<td>—</td>
</tr>
<tr>
<td>LVCMOS18, Open Drain</td>
<td>4mA, 8mA, 12mA, 16mA</td>
<td>—</td>
</tr>
<tr>
<td>LVCMOS15, Open Drain</td>
<td>4mA, 8mA</td>
<td>—</td>
</tr>
<tr>
<td>LVCMOS12, Open Drain</td>
<td>2mA, 6mA</td>
<td>—</td>
</tr>
<tr>
<td>PCI33^2</td>
<td>N/A</td>
<td>3.3</td>
</tr>
<tr>
<td>HSTL18 Class I</td>
<td>8mA, 12mA</td>
<td>1.8</td>
</tr>
<tr>
<td>HSTL18 Class II</td>
<td>N/A</td>
<td>1.8</td>
</tr>
<tr>
<td>HSTL15 Class I</td>
<td>4mA, 8mA</td>
<td>1.5</td>
</tr>
<tr>
<td>SSTL3 Class I, II</td>
<td>N/A</td>
<td>3.3</td>
</tr>
<tr>
<td>SSTL2 Class I</td>
<td>8mA, 12mA</td>
<td>2.5</td>
</tr>
<tr>
<td>SSTL2 Class II</td>
<td>16mA, 20mA</td>
<td>2.5</td>
</tr>
<tr>
<td>SSTL18 Class I</td>
<td>N/A</td>
<td>1.8</td>
</tr>
<tr>
<td>SSTL18 Class II</td>
<td>8mA, 12mA</td>
<td>1.8</td>
</tr>
</tbody>
</table>

#### Differential Interfaces

<table>
<thead>
<tr>
<th>Differential Interfaces</th>
<th>V_{CCIO} (Nom.)</th>
</tr>
</thead>
<tbody>
<tr>
<td>Differential SSTL3, Class I, II</td>
<td>N/A</td>
</tr>
<tr>
<td>Differential SSTL2, Class I</td>
<td>8mA, 12mA</td>
</tr>
<tr>
<td>Differential SSTL2, Class II</td>
<td>16mA, 20mA</td>
</tr>
<tr>
<td>Differential SSTL18, Class I</td>
<td>N/A</td>
</tr>
<tr>
<td>Differential SSTL18, Class II</td>
<td>8mA, 12mA</td>
</tr>
<tr>
<td>Differential HSTL15, Class I</td>
<td>N/A</td>
</tr>
<tr>
<td>Differential HSTL18, Class II</td>
<td>8mA, 12mA</td>
</tr>
<tr>
<td>Differential HSTL18, Class II</td>
<td>N/A</td>
</tr>
<tr>
<td>Differential HSTL15, Class I</td>
<td>4mA, 8mA</td>
</tr>
</tbody>
</table>
LatticeXP2 sysIO Banking Scheme

LatticeXP2 devices have eight general purpose programmable sysIO banks. Each of the eight general purpose sysIO banks has a $V_{CCIO}$ supply voltage, and two reference voltages, $V_{REF1}$ and $V_{REF2}$. Figure 8-1 shows the eight general purpose banks.

On the top and bottom banks, the sysIO buffer pair consists of two single-ended output drivers and two sets of single-ended input buffers (both ratioed and referenced). The left and right sysIO buffer pair consists of two single-ended output drivers and two sets of single-ended input buffers (both ratioed and referenced). The referenced input buffer can also be configured as a differential input. True LVDS support is available on only 50% of the left and right I/Os (starting with the topmost pairs). There are no LVDS on the top and bottom I/Os. In 50% of the pairs there is also one differential output driver. The two pads in the pair are described as “true” and “comp”, where the true pad is associated with the positive side of the differential input buffer and the comp (complementary) pad is associated with the negative side of the differential input buffer.

SPI Flash Interface

The SPI pins (master/slave) are multiplexed with the I/Os in Bank 7. The two dedicated pins CFG[0] and TOE are powered by $V_{CC}$ and reside between Banks 6 and 7.

JTAG Interface

The JTAG pins are located between Banks 2 and 3 and are powered by $V_{CCJ}$.

Figure 8-1. LatticeXP2 sysIO Banking

<table>
<thead>
<tr>
<th>Output Standard</th>
<th>Drive</th>
<th>$V_{CCIO}$ (Nom.)</th>
</tr>
</thead>
<tbody>
<tr>
<td>LVDS</td>
<td>N/A</td>
<td>2.5</td>
</tr>
<tr>
<td>MLVDS&lt;sup&gt;1&lt;/sup&gt;</td>
<td>N/A</td>
<td>2.5</td>
</tr>
<tr>
<td>BLVDS&lt;sup&gt;1&lt;/sup&gt;</td>
<td>N/A</td>
<td>2.5</td>
</tr>
<tr>
<td>LVPECL&lt;sup&gt;1&lt;/sup&gt;</td>
<td>N/A</td>
<td>3.3</td>
</tr>
<tr>
<td>RSDS&lt;sup&gt;1&lt;/sup&gt;</td>
<td>N/A</td>
<td>2.5</td>
</tr>
</tbody>
</table>

1. Emulated with external resistors.
2. PCI33 is PCIX compatible.

Table 8-2. Supported Output Standards (Continued)

<table>
<thead>
<tr>
<th>Output Standard</th>
<th>Drive</th>
<th>$V_{CCIO}$ (Nom.)</th>
</tr>
</thead>
<tbody>
<tr>
<td>Bank 0</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Bank 1</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Bank 5</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Bank 4</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Bank 2</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Bank 3</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Bank 6</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Bank 7</td>
<td></td>
<td></td>
</tr>
</tbody>
</table>
There are a total of eight V_CCIO supplies, V_CCIO0 - V_CCIO7. Each bank has a separate V_CCIO supply that powers the single-ended output drivers and the ratioed input buffers such as LVTTL, LVCMOS, and PCI. LVTTL, LVCMOS3.3, LVCMOS2.5 and LVCMOS1.2 also have fixed threshold options allowing them to be placed in any bank. The V_CCIO voltage applied to the bank determines the ratioed input standards that can be supported in that bank. It is also used to power the differential output drivers.

V_CCAUX (3.3V)

In addition to the bank V_CCIO supplies, devices have a V_CC core logic power supply and a V_CCAUX auxiliary supply that powers the differential and referenced input buffers. V_CCAUX is used to supply I/O reference voltage requiring 3.3V to satisfy the common-mode range of the drivers and input buffers.

V_CCJ (1.2V/1.5V/1.8V/2.5V/3.3V)

The JTAG pins have a separate V_CCJ power supply that is independent of the bank V_CCIO supplies. V_CCJ determines the electrical characteristics of the LVCMOS JTAG pins, both the output high level and the input threshold.

Table 8-3 shows a summary of all the required power supplies.

Table 8-3. Power Supplies

<table>
<thead>
<tr>
<th>Power Supply</th>
<th>Description</th>
<th>Value1</th>
</tr>
</thead>
<tbody>
<tr>
<td>V_CC</td>
<td>Core Power Supply</td>
<td>1.2V</td>
</tr>
<tr>
<td>V_CCIO2</td>
<td>Power Supply for the I/O Banks</td>
<td>1.2V/1.5V/1.8V/2.5V/3.3V</td>
</tr>
<tr>
<td>V_CCAUX</td>
<td>Auxiliary Power Supply</td>
<td>3.3V</td>
</tr>
<tr>
<td>V_CCJ2</td>
<td>Power Supply for JTAG Pins</td>
<td>1.2V/1.5V/1.8V/2.5V/3.3V</td>
</tr>
</tbody>
</table>

1. Refer to the LatticeXP2 Family Data Sheet for recommended min. and max. values.
2. If V_CCIO or V_CCJ is set to 3.3V, they MUST be connected to the same power supply as V_CCAUX.

Input Reference Voltage (V_REF1, V_REF2)

Each bank can support up to two separate V_REF input voltages, V_REF1 and V_REF2, that are used to set the threshold for the referenced input buffers. The locations of these V_REF pins are pre-determined within the bank. These pins can be used as regular I/Os if the bank does not require a V_REF voltage.

V_REF1 for DDR Memory Interface

When interfacing to DDR memory, the V_REF1 input must be used as the reference voltage for the DQS and DQ input from the memory. A voltage divider between V_REF1 and GND is used to generate an on-chip reference voltage that is used by the DQS transition detector circuit. This voltage divider is only present on V_REF1, it is not available on V_REF2. For more information on the DQS transition detect logic and its implementation, please refer to Lattice technical note number TN1138, LatticeXP2 High Speed I/O Interface. For DDR1 memory interfaces, the V_REF1 should be connected to 1.25V. Therefore, only SSTL25_II signaling is allowed. For DDR2 memory interfaces this should be connected to 0.9V, and only SSTL18_II signaling is allowed.

Mixed Voltage Support in a Bank

The LatticeXP2 sysIO buffer is connected to three parallel ratioed input buffers. These three parallel buffers are connected to V_CCIO, V_CCAUX and V_CC, giving support for thresholds that track with V_CCIO as well as fixed thresholds for 3.3V (V_CCAUX) and 1.2V (V_CC) inputs. This allows the input threshold for ratioed buffers to be assigned on a pin-by-pin basis rather than tracking with V_CCIO. This option is available for all 1.2V, 2.5V and 3.3V ratioed inputs and is independent of the bank V_CCIO voltage. For example, if the bank V_CCIO is 1.8V, it is possible to have 1.2V and 3.3V ratioed input buffers with fixed thresholds, as well as 2.5V ratioed inputs with tracking thresholds.
Prior to device configuration, the ratioed input thresholds always tracks the bank V_{CCIO}. This option only takes effect after configuration. Output standards within a bank are always set by V_{CCIO}. Table 8-4 shows the sysIO standards that can be mixed in the same bank.

**Table 8-4. Mixed Voltage Support**

<table>
<thead>
<tr>
<th>V_{CCIO}</th>
<th>Input sysIO Standards</th>
<th>Output sysIO Standards</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>1.2V</td>
<td>1.5V</td>
</tr>
<tr>
<td>1.2V</td>
<td>Yes</td>
<td>Yes</td>
</tr>
<tr>
<td>1.5V</td>
<td>Yes</td>
<td>Yes</td>
</tr>
<tr>
<td>1.8V</td>
<td>Yes</td>
<td>Yes</td>
</tr>
<tr>
<td>2.5V</td>
<td>Yes</td>
<td>Yes</td>
</tr>
<tr>
<td>3.3V</td>
<td>Yes</td>
<td>Yes</td>
</tr>
</tbody>
</table>

**sysIO Standards Supported by Bank**

**Table 8-5. I/O Standards Supported by Bank**

<table>
<thead>
<tr>
<th>Description</th>
<th>Top Side Banks 0-1</th>
<th>Right Side Banks 2-3</th>
<th>Bottom Side Banks 4-5</th>
<th>Left Side Banks 6-7</th>
</tr>
</thead>
<tbody>
<tr>
<td>Output Standards Supported</td>
<td>LVTTL</td>
<td>LVCMOS33</td>
<td>LVCMOS25</td>
<td>LVCMOS18</td>
</tr>
<tr>
<td></td>
<td>SSTL18 Class I, II</td>
<td>SSTL25 Class I, II</td>
<td>SSTL33 Class I, II</td>
<td>HSTL15 Class I</td>
</tr>
<tr>
<td></td>
<td>SSTL18D Class I, II</td>
<td>SSTL25D Class I, II</td>
<td>SSTL33D Class I, II</td>
<td>HSTL15D Class I</td>
</tr>
<tr>
<td></td>
<td>MLVDS</td>
<td>LVDS25E1</td>
<td>LVPECL1</td>
<td>BLVDS1</td>
</tr>
<tr>
<td></td>
<td></td>
<td>LVDS</td>
<td>LVDS25E1</td>
<td>LVPECL1</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>LVDS</td>
<td>LVPECL1</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Inputs</td>
<td>All Single-ended, Differential</td>
<td>All Single-ended, Differential</td>
<td>All Single-ended, Differential</td>
<td>All Single-ended, Differential</td>
</tr>
<tr>
<td>Clock Inputs</td>
<td>All Single-ended, Differential</td>
<td>All Single-ended, Differential</td>
<td>All Single-ended, Differential</td>
<td>All Single-ended, Differential</td>
</tr>
<tr>
<td>PCI Support</td>
<td>PCi33 with clamp</td>
<td>PCi33 without clamp</td>
<td>PCi33 with clamp</td>
<td>PCi33 without clamp</td>
</tr>
<tr>
<td>LVDS Output Buffers</td>
<td>LVDS (3.5mA Buffers)</td>
<td>LVDS (3.5mA Buffers)</td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

1. These differential standards are implemented by using a complementary LVCMOS driver with external resistor pack.
2. Available only on 50% of the I/Os in the bank.
LVCMOS Buffer Configurations

All LVCMOS buffer have programmable pull, programmable drive and programmable slew configurations that can be set in the software.

Bus Maintenance Circuit

Each pad has a weak pull-up, weak pull-down and weak buskeeper capability. The pull-up and pull-down settings offer a fixed characteristic, which is useful in creating wired logic such as wired ORs. However, current can be slightly higher than other options, depending on the signal state. The bus-keeper option latches the signal in the last driven state, holding it at a valid level with minimal power dissipation. Users can also choose to turn off the bus maintenance circuitry, minimizing power dissipation and input leakage. Note that in this case, it is important to ensure that inputs are driven to a known state to avoid unnecessary power dissipation in the input buffer. The internal weak pull-up is enabled on all unused pins.

Programmable Drive

Each LVCMOS or LVTTL, as well as some of the referenced (SSTL and HSTL) output buffers, has a programmable drive strength option. This option can be set for each I/O independently. The drive strength settings available are 2mA, 4mA, 6mA, 8mA, 12mA, 16mA and 20mA. Actual options available vary by the I/O voltage. The user must consider the maximum allowable current per bank and the package thermal limit current when selecting the drive strength. Table 8-6 shows the available drive settings for each of the output standards.

Table 8-6. Programmable Drive Values for Single-ended Buffers

<table>
<thead>
<tr>
<th>Single Ended I/O Standard</th>
<th>Programmable Drive (mA)</th>
</tr>
</thead>
<tbody>
<tr>
<td>HSTL15_I</td>
<td>4, 8</td>
</tr>
<tr>
<td>HSTL18_I</td>
<td>8, 12</td>
</tr>
<tr>
<td>SSTL25_I</td>
<td>8, 12</td>
</tr>
<tr>
<td>SSTL25_II</td>
<td>16, 20</td>
</tr>
<tr>
<td>SSTL18_II</td>
<td>8, 12</td>
</tr>
<tr>
<td>LVCMOS12</td>
<td>2, 6</td>
</tr>
<tr>
<td>LVCMOS15</td>
<td>4, 8</td>
</tr>
<tr>
<td>LVCMOS18</td>
<td>4, 8, 12, 16</td>
</tr>
<tr>
<td>LVCMOS25</td>
<td>4, 8, 12, 16, 20</td>
</tr>
<tr>
<td>LVCMOS33</td>
<td>4, 8, 12, 16, 20</td>
</tr>
<tr>
<td>LVTTL</td>
<td>4, 8, 12, 16, 20</td>
</tr>
</tbody>
</table>

Programmable Slew Rate

Each LVCMOS or LVTTL output buffer pin also has a programmable output slew rate control that can be configured for either low noise or high-speed performance. Each I/O pin has an individual slew rate control. This allows designers to specify slew rate control on a pin-by-pin basis. This slew rate control affects both the rising and falling edges.

Open-Drain Control

All LVCMOS and LVTTL output buffers can be configured to function as open drain outputs. The user can implement an open drain output by turning on the OPENDRAIN attribute in the software.

Differential SSTL and HSTL support

The single-ended driver associated with the complementary ‘C’ pad can optionally be driven by the complement of the data that drives the single-ended driver associated with the true pad. This allows a pair of single-ended drivers to be used to drive complementary outputs with the lowest possible skew between the signals. This is used for driving complementary SSTL and HSTL signals (as required by the differential SSTL and HSTL clock inputs on syn-
chronous DRAM and synchronous SRAM devices respectively). This capability is also used in conjunction with off-chip resistors to emulate LVPECL, and BLVDS output drivers.

**Table 8-7. Programmable Drive Values for Differential Buffers**

<table>
<thead>
<tr>
<th>Differential I/O Standard</th>
<th>Programmable Drive (mA)</th>
</tr>
</thead>
<tbody>
<tr>
<td>HSTL15D_I</td>
<td>4, 8</td>
</tr>
<tr>
<td>HSTL18D_I</td>
<td>8, 12</td>
</tr>
<tr>
<td>SSTL25D_I</td>
<td>8, 12</td>
</tr>
<tr>
<td>SSTL25D_II</td>
<td>16, 20</td>
</tr>
<tr>
<td>SSTL18D_II</td>
<td>8, 12</td>
</tr>
</tbody>
</table>

**PCI Support with Programmable PCICLAMP**

Each sysIO buffer can be configured to support PCI33. The buffers on the top and bottom sides of the device have an optional PCI clamp diode that may optionally be specified in the ispLEVER design tools.

Programmable PCICLAMP can be turned ON or OFF. This option is available on each I/O independently on the top and bottom side banks.

**Programmable Input Delay**

Each input can optionally be delayed before it is passed to the core logic or input registers. The primary use for the input delay is to achieve zero hold time for the input registers when using a direct drive primary clock. To arrive at zero hold time, the input delay will delay the data by at least as much as the primary clock injection delay. This option can be turned ON or OFF for each I/O independently in the software using the FIXEDDELAY attribute. This attribute is described in more detail in the software sysIO attribute section. Appendix A shows how this feature can be enabled in the software using HDL attributes.

**Software sysIO Attributes**

sysIO attributes can be specified in the HDL, using the Spreadsheet View of the Design Planner or in the ASCII preference file (.lpf) file directly. Appendices A, B and C list examples of how these can be assigned using each of these methods. This section describes each of these attributes in detail.

**IO_TYPE**

This is used to set the sysIO standard for an I/O. The $V_{CCIO}$ required to set these I/O standards are embedded in the attribute names itself. There is no separate attribute to set the $V_{CCIO}$ requirements. Table 8-8 lists the available I/O types.
Table 8-8. IO_TYPE Attribute Values

<table>
<thead>
<tr>
<th>sysIO Signaling Standard</th>
<th>IO_TYPE</th>
</tr>
</thead>
<tbody>
<tr>
<td>DEFAULT</td>
<td>LVCMOS25</td>
</tr>
<tr>
<td>LVDS 2.5V</td>
<td>LVDS25</td>
</tr>
<tr>
<td>RSDD</td>
<td>RSDS(^1)</td>
</tr>
<tr>
<td>Emulated LVDS 2.5V</td>
<td>LVDS25E(^1)</td>
</tr>
<tr>
<td>Bus LVDS 2.5V</td>
<td>BLVDS25(^1)</td>
</tr>
<tr>
<td>LVPECL 3.3V</td>
<td>LVPECL33(^1)</td>
</tr>
<tr>
<td>HSTL18 Class I and II</td>
<td>HSTL18_I, HSTL18_II</td>
</tr>
<tr>
<td>Differential HSTL 18 Class I and II</td>
<td>HSTL18D_I, HSTL18D_II</td>
</tr>
<tr>
<td>HSTL 15 Class I</td>
<td>HSTL15_I</td>
</tr>
<tr>
<td>Differential HSTL 15 Class I</td>
<td>HSTL15D_I</td>
</tr>
<tr>
<td>SSTL 33 Class I and II</td>
<td>SSTL33_I, SSTL33_II</td>
</tr>
<tr>
<td>Differential SSTL 33 Class I and II</td>
<td>SSTL33D_I, SSTL33D_II</td>
</tr>
<tr>
<td>SSTL 25 Class I and II</td>
<td>SSTL25_I, SSTL25_II</td>
</tr>
<tr>
<td>Differential SSTL 25 Class I and II</td>
<td>SSTL25D_I, SSTL25D_II</td>
</tr>
<tr>
<td>SSTL 18 Class I and II</td>
<td>SSTL18_I, SSTL18_II</td>
</tr>
<tr>
<td>Differential SSTL 18 Class I and II</td>
<td>SSTL18D_I, SSTL18D_II</td>
</tr>
<tr>
<td>LVTTL</td>
<td>LVTTL33</td>
</tr>
<tr>
<td>3.3V LVCMOS</td>
<td>LVCMOS33</td>
</tr>
<tr>
<td>2.5V LVCMOS</td>
<td>LVCMOS25</td>
</tr>
<tr>
<td>1.8V LVCMOS</td>
<td>LVCMOS18</td>
</tr>
<tr>
<td>1.5V LVCMOS</td>
<td>LVCMOS15</td>
</tr>
<tr>
<td>1.2V LVCMOS</td>
<td>LVCMOS12</td>
</tr>
<tr>
<td>3.3V PCI</td>
<td>PCI33</td>
</tr>
<tr>
<td>MLVDS</td>
<td>MLVDS(^1)</td>
</tr>
</tbody>
</table>

1. These differential standards are implemented by using a complementary LVCMOS driver with external resistor pack.

OPENDRAIN

LVCMOS and LVTTL I/O standards can be set to open drain configuration by using the OPENDRAIN attribute.

Values: ON, OFF
Default: OFF

DRIVE

The DRIVE attribute will set the programmable drive strength for the output standards that have programmable drive capability.
Table 8-9. DRIVE Settings

<table>
<thead>
<tr>
<th>Output Standard</th>
<th>DRIVE (mA)</th>
<th>Default (mA)</th>
</tr>
</thead>
<tbody>
<tr>
<td>HSTL15_I/ HSTL15D_I</td>
<td>4, 8</td>
<td>8</td>
</tr>
<tr>
<td>HSTL18_I/ HSTL18D_I</td>
<td>8, 12</td>
<td>12</td>
</tr>
<tr>
<td>SSTL25_I/ SSTL25D_I</td>
<td>8, 12</td>
<td>8</td>
</tr>
<tr>
<td>SSTL25_II/ SSTL25D_II</td>
<td>16, 20</td>
<td>16</td>
</tr>
<tr>
<td>SSTL18_II/SSTL18D_II</td>
<td>8, 12</td>
<td>12</td>
</tr>
<tr>
<td>LVCMOS12</td>
<td>2, 6</td>
<td>6</td>
</tr>
<tr>
<td>LVCMOS15</td>
<td>4, 8</td>
<td>8</td>
</tr>
<tr>
<td>LVCMOS18</td>
<td>4, 8, 12, 16</td>
<td>12</td>
</tr>
<tr>
<td>LVCMOS25</td>
<td>4, 8, 12, 16, 20</td>
<td>12</td>
</tr>
<tr>
<td>LVCMOS33</td>
<td>4, 8, 12, 16, 20</td>
<td>12</td>
</tr>
<tr>
<td>LVTTL</td>
<td>4, 8, 12, 16, 20</td>
<td>12</td>
</tr>
</tbody>
</table>

PULLMODE

The PULLMODE attribute is available for all the LVTTL, LVCMOS and PCI inputs and outputs. This attribute can be enabled for each I/O independently.

Values: UP, DOWN, NONE, KEEPER
Default: UP

Table 8-10. PULLMODE Values

<table>
<thead>
<tr>
<th>PULL Options</th>
<th>PULLMODE Value</th>
</tr>
</thead>
<tbody>
<tr>
<td>Pull-up (Default)</td>
<td>UP</td>
</tr>
<tr>
<td>Pull-down</td>
<td>DOWN</td>
</tr>
<tr>
<td>Bus Keeper</td>
<td>KEEPER</td>
</tr>
<tr>
<td>Pull Off</td>
<td>NONE</td>
</tr>
</tbody>
</table>

PCICLAMP

PCI33 inputs on the top and bottom of the device have an optional PCI clamp that is enabled via the PCICLAMP attribute. The PCICLAMP is also available for all LVCMOS33 and LVTTL inputs.

Values: ON, OFF

Table 8-11. PCICLAMP Values

<table>
<thead>
<tr>
<th>Input Type</th>
<th>PCICLAMP Value</th>
</tr>
</thead>
<tbody>
<tr>
<td>PCI33</td>
<td>ON (default), OFF</td>
</tr>
<tr>
<td>LVCMOS33</td>
<td>OFF (default), ON</td>
</tr>
<tr>
<td>LVTTL</td>
<td>OFF (default), ON</td>
</tr>
</tbody>
</table>

SLEWRATE

The SLEWRATE attribute is available for all LVTTL and LVCMOS output drivers. Each I/O pin has an individual slew rate control. This allows a designer to specify slew rate control on a pin-by-pin basis.

Values: FAST, SLOW
Default: FAST
The FIXEDDELAY attribute is available to each input pin. This attribute, when enabled, is used to achieve zero hold time for the input registers when using global clock. This attribute can only be assigned in the HDL source.

Values: TRUE, FALSE
Default: FALSE

INBUF
By default, all the unused input buffers are disabled. The INBUF attribute is used to enable the unused input buffers when performing a boundary scan test. This is a global attribute and can be globally set to ON or OFF.

Values: ON, OFF
Default: ON

DIN/DOUT
This attribute can be used to assign I/O registers. Using DIN will assert an input register and using the DOUT attribute will assert an output register. By default, the software will try to assign the I/O registers, if applicable. The user can turn this OFF by using the synthesis attribute or by using the Spreadsheet View of the Design Planner. These attributes can only be applied to registers.

LOC
This attribute can be used to make pin assignments to the I/O ports in the design. This attributes is only used when the pin assignments are made in HDL source. Designers can also assign pins directly using the Spreadsheet View of the Design Planner in the ispLEVER software. The appendices explain this in further detail.

Design Considerations and Usage
This section discusses some of the design rules and considerations that must be taken into account when designing with the LatticeXP2 sysIO buffer

Banking Rules
- If $V_{CCIO}$ or $V_{CCJ}$ for any bank is set to 3.3 V, it is recommended that it be connected to the same power supply as $V_{CCAUX}$, thus minimizing leakage.
- If $V_{CCIO}$ or $V_{CCJ}$ for any bank is set to 1.2V, it is recommended that it be connected to the same power supply as $V_{CC}$, thus minimizing leakage.
- When implementing DDR memory interfaces, the $V_{REF}$ of the bank is used to provide reference to the interface pins and cannot be used to power any other referenced inputs.
- Only the top and bottom banks (banks 0, 1, 4 and 5) will support PCI clamps.
- All legal input buffers should be independent of bank $V_{CCIO}$, except for 1.8V and 1.5V buffers, which require a bank $V_{CCIO}$ of 1.8V and 1.5V.

Differential I/O Rules
- All banks can support LVDS input buffers. Only the banks on the right and left sides (Banks 2, 3, 6 and 7) will support True Differential output buffers. The banks on all sides will support the LVDS input buffers. The user can use emulated LVDS output buffers on these banks.
- All banks support emulated differential buffers using external resistor pack and complementary LVCMOS drivers.
- Only 50% of the I/Os on the left and right sides can provide LVDS output buffer capability. LVDS can only be assigned to the TRUE pad. The ispLEVER design tool will automatically assign the other I/Os of the differential pair to the complementary pad. Refer to the device data sheet to see the pin listings for all LVDS pairs.
Differential I/O Implementation

The LatticeXP2 devices support a variety of differential standards as detailed in the following sections.

LVDS

True LVDS (LVDS25) drivers are available on 50% of the I/Os on the left and right side of the devices. LVDS input support is provided on all sides of the device. All four sides of the device support LVDS using complementary LVCMOS drivers with external resistors (LVDS25E). Refer to the LatticeXP2 Family Data Sheet for a detailed explanation of these LVDS implementations.

BLVDS

All single-ended sysIO buffers pairs support the Bus-LVDS standard using complementary LVCMOS drivers with external resistors. Please refer to the LatticeXP2 Family Data Sheet for a detailed explanation of BLVDS implementation.

RSDS

All single-ended sysIO buffers pairs support RSDS standard using complementary LVCMOS drivers with external resistors. Please refer to the LatticeXP2 Family Data Sheet for a detailed explanation of RSDS implementation.

LVPECL

All the sysIO buffers will support LVPECL inputs. LVPECL outputs are supported using complementary LVCMOS driver with external resistors. Please refer to the LatticeXP2 Family Data Sheet for a detailed explanation of LVPECL implementation.

Differential SSTL and HSTL

All single-ended sysIO buffers pairs support differential SSTL and HSTL. Please refer to the LatticeXP2 Family Data Sheet for a detailed explanation of Differential HSTL and SSTL implementation.

MLVDS

All single-ended sysIO buffers pairs support MLVDS standard using complementary LVCMOS drivers with external resistors. Please refer to the LatticeXP2 Family Data Sheet for a detailed explanation of MLVDS implementation.

Technical Support Assistance

Hotline: 1-800-LATTICE (North America)
+1-503-268-8001 (Outside North America)
e-mail: techsupport@latticesemi.com
Internet: www.latticesemi.com

Revision History

<table>
<thead>
<tr>
<th>Date</th>
<th>Version</th>
<th>Change Summary</th>
</tr>
</thead>
<tbody>
<tr>
<td>February 2007</td>
<td>01.0</td>
<td>Initial release.</td>
</tr>
<tr>
<td>April 2008</td>
<td>01.1</td>
<td>Updated Supported Output Standards table.</td>
</tr>
<tr>
<td></td>
<td></td>
<td>Updated sysIO Banking figure.</td>
</tr>
<tr>
<td>February 2009</td>
<td>01.2</td>
<td>Updated I/O Standards Supported by Bank table.</td>
</tr>
<tr>
<td>June 2010</td>
<td>01.3</td>
<td>Added Appendix D - sysIO Attributes Using the Diamond Spreadsheet View User Interface.</td>
</tr>
</tbody>
</table>
**Appendix A. HDL Attributes for Synplicity® and Precision® RTL Synthesis**

Using these HDL attributes, designers can assign the sysIO attributes directly in their source. The attribute definition and syntax for the appropriate synthesis vendor must be used. Below are a list of all the sysIO attributes, syntax and examples for Precision RTL Synthesis and Synplicity. This section only lists the sysIO buffer attributes for these devices. These attributes are available through the ispLEVER software Help system.

**VHDL Synplicity/Precision RTL Synthesis**

This section lists syntax and examples for all the sysIO Attributes in VHDL when using the Precision RTL Synthesis or Synplicity synthesis tools.

**Syntax**

*Table 8-12. VHDL Attribute Syntax for Synplicity and Precision RTL Synthesis*

<table>
<thead>
<tr>
<th>Attribute</th>
<th>Syntax</th>
</tr>
</thead>
<tbody>
<tr>
<td>IO_TYPE</td>
<td>attribute IO_TYPE: string; attribute IO_TYPE of Pinname: signal is &quot;IO_TYPE Value&quot;;</td>
</tr>
<tr>
<td>OPENDRAIN</td>
<td>attribute OPENDRAIN: string; attribute OPENDRAIN of Pinname: signal is &quot;OpenDrain Value&quot;;</td>
</tr>
<tr>
<td>DRIVE</td>
<td>attribute DRIVE: string; attribute DRIVE of Pinname: signal is &quot;Drive Value&quot;;</td>
</tr>
<tr>
<td>PULLMODE</td>
<td>attribute PULLMODE: string; attribute PULLMODE of Pinname: signal is &quot;Pullmode Value&quot;;</td>
</tr>
<tr>
<td>PCICLAMP</td>
<td>attribute PCICLAMP: string; attribute PCICLAMP of Pinname: signal is &quot;PCIClamp Value&quot;;</td>
</tr>
<tr>
<td>SLEWRATE</td>
<td>attribute SLEWRATE: string; attribute SLEWRATE of Pinname: signal is &quot;Slewrate Value&quot;;</td>
</tr>
<tr>
<td>FIXEDDELAY</td>
<td>attribute FIXEDDELAY: string; attribute FIXEDDELAY of Pinname: signal is &quot;Fixeddelay Value&quot;;</td>
</tr>
<tr>
<td>DIN</td>
<td>attribute DIN: string; attribute DIN of Pinname: signal is &quot; &quot;;</td>
</tr>
<tr>
<td>DOUT</td>
<td>attribute DOUT: string; attribute DOUT of Pinname: signal is &quot; &quot;;</td>
</tr>
<tr>
<td>LOC</td>
<td>attribute LOC: string; attribute LOC of Pinname: signal is &quot;pin_locations&quot;;</td>
</tr>
</tbody>
</table>

**Examples**

**IO_TYPE**

```vhdl
--***Attribute Declaration***
ATTRIBUTE IO_TYPE: string;
--***IO_TYPE assignment for I/O Pin***
ATTRIBUTE IO_TYPE OF portA: SIGNAL IS "PCI33";
ATTRIBUTE IO_TYPE OF portB: SIGNAL IS "LVCMOS33";
ATTRIBUTE IO_TYPE OF portC: SIGNAL IS "LVDS25";
```

**OPENDRAIN**

```vhdl
--***Attribute Declaration***
ATTRIBUTE OPENDRAIN: string;
--***DRIVE assignment for I/O Pin***
ATTRIBUTE OPENDRAIN OF portB: SIGNAL IS "ON";
```
DRIVE

--***Attribute Declaration***
ATTRIBUTE DRIVE: string;
--***DRIVE assignment for I/O Pin***
ATTRIBUTE DRIVE OF portB: SIGNAL IS "20";

PULLMODE

--***Attribute Declaration***
ATTRIBUTE PULLMODE : string;
--***PULLMODE assignment for I/O Pin***
ATTRIBUTE PULLMODE OF portA: SIGNAL IS "DOWN";
ATTRIBUTE PULLMODE OF portB: SIGNAL IS "UP";

PCICLAMP

--***Attribute Declaration***
ATTRIBUTE PCICLAMP: string;
--***PULLMODE assignment for I/O Pin***
ATTRIBUTE PCICLAMP OF portA: SIGNAL IS "ON";

SLEWRATE

--***Attribute Declaration***
ATTRIBUTE SLEWRATE : string;
--***SLEWRATE assignment for I/O Pin***
ATTRIBUTE SLEWRATE OF portB: SIGNAL IS "FAST";

FIXEDDELAY

--***Attribute Declaration***
ATTRIBUTE FIXEDDELAY: string;
--***SLEWRATE assignment for I/O Pin***
ATTRIBUTE FIXEDDELAY OF portB: SIGNAL IS "TRUE";

DIN/DOUT

--***Attribute Declaration***
ATTRIBUTE din : string;
ATTRIBUTE dout : string;
--***din/dout assignment for I/O Pin***
ATTRIBUTE din OF input_vector: SIGNAL IS " ";
ATTRIBUTE dout OF output_vector: SIGNAL IS " ";

LOC

--***Attribute Declaration***
ATTRIBUTE LOC : string;
--***LOC assignment for I/O Pin***
ATTRIBUTE LOC OF input_vector: SIGNAL IS "E3,B3,C3 ";
Verilog Synplicity
This section lists syntax and examples for all the sysIO Attributes in Verilog using the Synplicity synthesis tool.

Syntax

**Table 8-13. Verilog Synplicity Attribute Syntax**

<table>
<thead>
<tr>
<th>Attribute</th>
<th>Syntax</th>
</tr>
</thead>
<tbody>
<tr>
<td>IO_TYPE</td>
<td>PinType PinName /* synthesis IO_TYPE=&quot;IO_Type Value&quot;*/;</td>
</tr>
<tr>
<td>OPENDRAIN</td>
<td>PinType PinName /* synthesis OPENDRAIN =&quot;OpenDrain Value&quot;*/;</td>
</tr>
<tr>
<td>DRIVE</td>
<td>PinType PinName /* synthesis DRIVE=&quot;Drive Value&quot;*/;</td>
</tr>
<tr>
<td>PULLMODE</td>
<td>PinType PinName /* synthesis PULLMODE=&quot;Pullmode Value&quot;*/;</td>
</tr>
<tr>
<td>PCICLAMP</td>
<td>PinType PinName /* synthesis PCICLAMP =&quot;PCIClamp Value&quot;*/;</td>
</tr>
<tr>
<td>SLEWRATE</td>
<td>PinType PinName /* synthesis SLEWRATE=&quot;Slewrate Value&quot;*/;</td>
</tr>
<tr>
<td>FIXEDDELAY</td>
<td>PinType PinName /* synthesis FIXEDDELAY=&quot;Fixeddelay Value&quot;*/;</td>
</tr>
<tr>
<td>DIN</td>
<td>PinType PinName /* synthesis DIN=&quot;&quot;*/;</td>
</tr>
<tr>
<td>DOUT</td>
<td>PinType PinName /* synthesis DOUT=&quot;&quot;*/;</td>
</tr>
<tr>
<td>LOC</td>
<td>PinType PinName /* synthesis LOC=&quot;pin_locations&quot;*/;</td>
</tr>
</tbody>
</table>

**Examples**

```
//IO_TYPE, PULLMODE, SLEWRATE and DRIVE assignment
output portB /*synthesis IO_TYPE="LVCMOS33" PULLMODE ="UP" SLEWRATE ="FAST"
DRIVE ="20"*/;
output portC /*synthesis IO_TYPE="LVDS25" */;

//OPENDRAIN
output portA /*synthesis OPENDRAIN ="ON"*/;

//PCICLAMP
output portA /*synthesis IO_TYPE="PCI33" PULLMODE ="PCIClamp"*/;

// Fixeddelay
input load /* synthesis FIXEDDELAY="TRUE" */;

// Place the flip-flops near the load input
input load /* synthesis din="" */;

// Place the flip-flops near the outload output
output outload /* synthesis dout="" */;

//I/O pin location
input [3:0] DATA0 /* synthesis loc="E3,B1,F3"*/;

//Register pin location
reg data_in_ch1_buf_reg3 /* synthesis loc="R40C47" */;

//Vectored internal bus
reg [3:0] data_in_ch1_reg /*synthesis loc ="R40C47,R40C46,R40C45,R40C44" */;
```
Verilog Precision
This section lists syntax and examples for all the sysIO Attributes in Verilog using the Precision RTL Synthesis tool.

Syntax

Table 8-14. Verilog Precision Attribute Syntax

<table>
<thead>
<tr>
<th>Attribute</th>
<th>Syntax</th>
</tr>
</thead>
<tbody>
<tr>
<td>IO_TYPE</td>
<td>//pragma attribute PinName IO_TYPE IO_TYPE Value</td>
</tr>
<tr>
<td>OPENDRAIN</td>
<td>// pragma attribute PinName OPENDRAIN OpenDrain Value</td>
</tr>
<tr>
<td>DRIVE</td>
<td>// pragma attribute PinName DRIVE Drive Value</td>
</tr>
<tr>
<td>PULLMODE</td>
<td>// pragma attribute PinName IO_TYPE Pullmode Value</td>
</tr>
<tr>
<td>PCICLAMP</td>
<td>// pragma attribute PinName PCICLAMP PCIClamp Value</td>
</tr>
<tr>
<td>SLEWRATE</td>
<td>// pragma attribute PinName IO_TYPE Slewrate Value</td>
</tr>
<tr>
<td>FIXEDDELAY</td>
<td>// pragma attribute PinName IO_TYPE Fixeddelay Value</td>
</tr>
<tr>
<td>LOC</td>
<td>// pragma attribute PinName LOC pin_location</td>
</tr>
</tbody>
</table>

Examples

//****IO_TYPE ***
//pragma attribute portA IO_TYPE PCI33
//pragma attribute portB IO_TYPE LVCMOS33
//pragma attribute portC IO_TYPE SSTL25_II

//*** Opendrain ***
//pragma attribute portB OPENDRAIN ON
//pragma attribute portD OPENDRAIN OFF

//*** Drive ***
//pragma attribute portB DRIVE 20
//pragma attribute portD DRIVE 8

//*** Pullmode***
//pragma attribute portB PULLMODE UP

//*** PCIClamp***
//pragma attribute portB PCICLAMP ON

//*** Slewrate ***
//pragma attribute portB SLEWRATE FAST
//pragma attribute portD SLEWRATE SLOW

// ***Fixeddelay***
// pragma attribute load FIXEDDELAY TRUE

//***LOC***
//pragma attribute portB loc E3
Appendix B. sysIO Attributes Using the Design Planner User Interface

Designers can assign sysIO buffer attributes using the Design Planner GUI available in the ispLEVER design tool. If you are using Lattice Diamond™ design software, refer to Appendix D. The Pin Attribute Sheet lists all the ports in a design and all the available sysIO attributes as preferences. By clicking on each of these cells, a list of all the valid I/O preferences for that port is displayed. Each column takes precedence over the next. Therefore, when a particular IO_TYPE is chosen, the DRIVE, PULLMODE and SLEWRATE columns will only list the valid combinations for that IO_TYPE. The pin locations can be locked using the pin location column of the Pin Attribute sheet. Right-clicking on a cell will list the available pin locations. The Spreadsheet View will also conduct a DRC check to search for any incorrect pin assignments.

Designers can enter DIN/DOUT preferences using the Cell Attributes sheet of the Preference Editor. All the preferences assigned using the Preference Editor are written into the preference file (.prf).

Figures 8-2 and 8-3 show the Pin Attribute sheet and the Cell Attribute sheet views of the preference editor. For further information on how to use the Preference Editor, refer to the ispLEVER Help documentation in the Help menu option of the software.

**Figure 8-2. Port Attributes Tab**
Figure 8-3. Cell Attributes Tab
Appendix C. sysIO Attributes Using Preference File (ASCII File)

Designers can enter sysIO attributes directly in the preference (.lpf) file as sysIO buffer preferences. The LPF file is a post-synthesis FPGA constraint file that stores logical preferences that have been created or modified in the Design Planner or Text Editor. It also contains logical preferences originating in the HDL source that have been modified.

Below are a list of sysIO buffer preference syntax and examples.

**IOBUF**

This preference is used to assign the attribute IO_TYPE, PULLMODE, SLEWRATE, PCICLAMP and DRIVE.

**Syntax**

```
IOBUF [ALLPORTS | PORT <port_name> | GROUP <group_name>] (keyword=<value>)+;
```

where:

- `<port_name>` = These are not the actual top-level port names, but should be the signal name attached to the port. PIOs in the physical design (.ncd) file are named using this convention. Any multiple listings or wildcarding should be done using GROUPs.

- **Keyword** = IO_TYPE, OPENDRAIN, DRIVE, PULLMODE, PCICLAMP, SLEWRATE.

**Example**

```
IOBUF PORT "port1" IO_TYPE=LVTTL33 OPENDRAIN=ON DRIVE=8 PULLMODE=UP
PCICLAMP =OFF SLEWRATE=FAST;
DEFINE PORT GROUP "bank1" "in*" "out_[0-31]";
IOBUF GROUP "bank1" IO_TYPE=SSTL18_II;
```

**LOCATE**

When this preference is applied to a specified component, it places the component at a specified site and locks the component to the site. If applied to a specified macro instance, it places the macro’s reference component at a specified site, places all of the macro’s pre-placed components (that is, all components that were placed in the macro’s library file) in sites relative to the reference component, and locks all of these placed components at their sites. Below are some of the LOCATE syntax and examples. For further information, refer to the ispLEVER Help documentation in the Help menu option of the software.

**Syntax**

```
LOCATE [COMP <comp_name> | MACRO <macro_name>] SITE <site_name>;
LOCATE VREF <vref_name> SITE <site_name>;
```

**Note:** If the comp_name, macro_name, or site_name begins with anything other than an alpha character (for example, “11C7”), you must enclose the name in quotes. Wildcard expressions are allowed in <comp_name>.

**Examples**

This command places the port Clk0 on the site A4:

```
LOCATE COMP “Clk0” SITE “A4”;
```

This command places the component PFU1 on the site named R1C7:

```
LOCATE COMP “PFU1” SITE “R1C7”;
LOCATE VREF “ref1” SITE PR29C;
```
USE DIN CELL
This preference specifies the given register to be used as an input flip-flop.

Syntax

USE DIN CELL <cell_name>;

where:

<cell_name> := string

Example

USE DIN CELL "din0";

USE DOUT CELL
Specifies the given register to be used as an output flip-flop.

Syntax

USE DOUT CELL <cell_name>;

where:

<cell_name> := string

Example

USE DOUT CELL "dout1";

GROUP VREF
This preference is used to group all the components that need to be associated to one $V_{REF}$ pin within a bank.

Syntax

LOCATE VREF <vref_name> SITE <site_name>;

Example

IOBUF GROUP <group_name> BANK=<bank_name> VREF=<Vref_name>
LOCATE VREF "ref1" SITE PR29C;
LOCATE VREF "ref2" SITE PR48B;
IOBUF GROUP "group1" IO_TYPE=SSTL18_II BANK=0 VREF=vref1 ;
sysIO buffer attributes can be assigned using the Spreadsheet View available in the Lattice Diamond design software. The Port Assignments Sheet lists all the ports in a design and all the available sysIO attributes in multiple columns. Click on each of these cells for a list of all valid I/O preferences for that port. Each column takes precedence over the next. Therefore, when you choose a particular IO_TYPE, the columns for the DRIVE, PULLMODE, SLEWRATE and other attributes will only list the valid entries for that IO_TYPE.

Pin locations can be locked using the Pin column of the Port Assignments sheet or using the Pin Assignments sheet. You can right-click on a cell and go to Assign Pins to see a list of available pins.

The Spreadsheet View also has an option to run a DRC check to check for any incorrect pin assignments. You can enter the DIN/DOUT preferences using the Cell Mapping Tab. All the preferences assigned using the Spreadsheet View are written into the logical preference file (.lpf).

Figure 8-4 shows the Port Assignments Sheet of the Spreadsheet View. For further information on how to use the Spreadsheet View, refer to the Diamond Help documentation, available in the Help menu option of the software.

Figure 8-4. Port Attributes Tab of Spreadsheet View

Users can create a VREF pin using the Spreadsheet View as shown in Figure 8-5 and then assign VREF for a bank using the VREF Column in the Ports Assignment Tab of the Spreadsheet View as show in Figure 8-6. See the Diamond online help for a more detailed description of this setting.

Figure 8-5. Creating a VREF in Spreadsheet View
Figure 8-6. Assigning VREF for an Input Port in Spreadsheet View

<table>
<thead>
<tr>
<th>Type</th>
<th>Name</th>
<th>Group by</th>
<th>Pin</th>
<th>Bank</th>
<th>Wref</th>
<th>IO_TYPE</th>
<th>FULL MODE</th>
<th>DRIVE</th>
<th>SUBWRT</th>
<th>PDC</th>
<th>CLAMP</th>
<th>OPE</th>
<th>IDRAI</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>Dir</td>
<td>N/A</td>
<td>N/A</td>
<td>N/A</td>
<td>N/A</td>
<td>LVCMOS25</td>
<td>UP</td>
<td>N/A</td>
<td>FAST</td>
<td>OFF</td>
<td>OFF</td>
<td></td>
<td></td>
</tr>
<tr>
<td>2</td>
<td>Input Port</td>
<td>Clk</td>
<td>N/A</td>
<td>N/A</td>
<td>N/A</td>
<td>LVCMOS25</td>
<td>UP</td>
<td>N/A</td>
<td>FAST</td>
<td>OFF</td>
<td>OFF</td>
<td></td>
<td></td>
</tr>
<tr>
<td>3</td>
<td>Input Port</td>
<td>Clk</td>
<td>N/A</td>
<td>N/A</td>
<td>VREF1.5</td>
<td>STL18_J</td>
<td>N/A</td>
<td>N/A</td>
<td>FAST</td>
<td>OFF</td>
<td>OFF</td>
<td></td>
<td></td>
</tr>
<tr>
<td>4</td>
<td>Input Port</td>
<td>OE</td>
<td>N/A</td>
<td>N/A</td>
<td>N/A</td>
<td>LVCMOS25</td>
<td>UP</td>
<td>N/A</td>
<td>FAST</td>
<td>OFF</td>
<td>OFF</td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

Port Assignments | Pin Assignments | Clock Resource | Resource Priority | Cell Mapping | Global Preferences | Timing Preferences | Group | Misc Preferences