Implementing a High Performance Pipelined Multiplier in a Lattice ispLSI® 5512VE Device

Introduction

Hardware multiplication is necessary in any system that contains Digital Signal Processing (DSP) functionalities. Often there is an off-the-shelf component the designer can use to address functionality issues like filtering, modulation, video processing, etc. However, in some designs, the expense of a dedicated DSP chip is not justified. Use of complex programmable logic devices (CPLDs) in these cases is a more viable solution since they provide more flexibility and higher performance at a lower cost than off-the-shelf solutions.

This application note describes some of the techniques available for performing high-speed signed multiplication in a Lattice ispLSI 5512VE-80LF256 device. A brief discussion on the basics of digital multiplication will be introduced, followed by implementation techniques and design requirements. The implementation is a complete four-stage pipelined design for high-speed performance using VHDL. The design can be easily modified to suit a particular designer's criteria.

ispLSI5512VE-80LF256

The ispLSI 5512VE-80LF256 has 512 macrocells and registers and 16 Generic Logic Blocks (GLBs). The outputs of the GLBs drive the Global Routing Pool (GRP). The GLB has 32 logic macrocells with dual output functions that can be both registered and combinatorial. There are five PTs per macrocell. The product term sharing array (PTSA) is comprised of 35 PTs that come from the three adjacent macrocells. The five PT-bypass path can bypass the PTSA. In addition, the GLB has 68 inputs that are fed from the GRP and drive 165 PTs. Each PT can contain all 68 inputs. Of the 165 PTs, five can perform extra control functions. The output of the macrocell can be configured to a D-type register, D-type latch, JK-type flip-flop or T-type flip-flop. The reset and preset available in a GLB can either be global or PT. There are six global PT output enable signals. Each cell is configurable to operate at 3.3V or 2.5V. The open drain, slow slew, and pull-up options are available on all pins in the device. JTAG programming and testing is supported.

Combinatorial vs. Pipelined Multipliers

Combinatorial logic multipliers are faster, but significantly larger, than their sequential/synchronous counterparts for wider inputs. A tradeoff exists between the long delay and the long latency. The advantage of the pipelined design is that glitches can be eliminated at the synchronized outputs, resulting in a significant improvement in performance.

Signed Combinatorial Shift-Add Multiplier

Current synthesis tools do not synthesize combinational multiplier/divider circuits well using the '*' and '/' arithmetic operators. The resulting synthesized circuits are typically very large for input bits with widths greater than four or five bits. This makes the optimizer's job particularly difficult. Modeling the structure of the shift-add multiplication algorithm can produce a more efficient combinational multiplier.

The Multiplier Theory

The binary multiplier, like its decimal counterpart, consists of a multiplicand (X), a multiplier (Y) and a product (P). The result is the product of the multiplier and the multiplicand (P = X * Y). The multiplication of two binary numbers is achieved by a process of successive shift and add operations. The multiplication of 23 (X) and 25 (Y), where the product (P) is 575, is illustrated in Figure1.

Figure 1. Binary Multiplication Example

				1	0	1	1	1		Multiplicand (X)
				1	1	0	0	1		Multiplier (Y)
				1	0	1	1	1		PP 1
			0	0	0	0	0			PP 2
		0	0	0	0	0				PP 3
	1	0	1	1	1					PP 4
1	0	1	1	1						PP 5
1	0	0	0	1	1	1	1	1	1	PP = sum of PP
										PP - Partial Prod.

The process consists of looking at each bit of the multiplier in succession, starting with the least significant bit (LSB). If the multiplier bit is logic '1', the multiplicand is copied down; otherwise, zeros are copied down. The numbers copied down in successive lines are shifted one position to the left from the previous number. Finally, the numbers are added and their sum provides the product.

When multiplying two signed numbers, the algorithm is modified slightly to cope with the sign bits. The sign of the product is determined from the signs of the multiplicand (X) and multiplier (Y). If they are alike, the sign of the

product is positive; if they are not alike, the sign of the product is negative.

Implementation

The main operation in the process of multiplication of two numbers is addition of the partial products. Therefore, the performance and speed of the multiplier depends on the performance of the adder that forms the core of the multiplier.

Pipelining: To achieve higher performance, the multiplier must be pipelined. Throughput is often more critical than the cycle response in DSP designs. In this case, latency in the multiply operation is the price for a faster clock rate. This is accomplished in a multiplier by breaking the carry chain and inserting flip-flops at strategic locations. Care must be taken that all inputs to the adder are created by signals at the same stage of the pipeline. Delay at this point is referred to as latency.

Design: The 11 by 11 signed multiplier is designed structurally using VHDL with lower level models described behaviorally. Since this is a shift and add pipelined multiplier, the main component is the pipelined adder. Multiplication is done with the 10 LSB bits; the MSB bit (11) is used for finding the sign of the product. The block diagram of an 11 by 11 multiplier is shown in Figure 2.

The carry of the adder must be a lookahead because, the shift-add operation needs the carry for the MSB in the multiplication. The carry of the lookahead full adder of each stage, C_{i+1}, is expressed as a function of the inputs A_I and B_I and C_I. The Boolean functions of the adder can be expressed in one-level logic, which can be fit in one GLB in a Lattice 5512VE device. The functions can be described with the help of a carry generate G_I and carry propagate P_I. Hence, the equations are :

$$\text{Generate} = G_I = A_I B_I$$

$$\text{Propagate} = P_I = A_I \oplus B_I$$

$$\text{Sum} = S_I = A_I \oplus B_I \oplus C_I = P_I \oplus C_I$$

$$\text{Carry} = C_{Ii+1} = A_I B_I + A_I C_I + B_I C_I$$

$$C_{Ii+1} = G_I + C_I P_I$$

When the carry is '1', then either carry is internally generated within the stage ($G_{I)}$) or the carry-in is '1', and it is propagated ($P_{I)}$) through the stage. Each bit is shifted and a '1' or '0' is copied, depending upon the logic value of the bit. After the bit is shifted, the pipelined adder performs addition. The same process is repeated for each bit of the multiplier, with a one-bit shift left in each case. The MSBs of the multiplicand and the multiplier are XORed to get the sign of the product, which is the MSB of the final product.

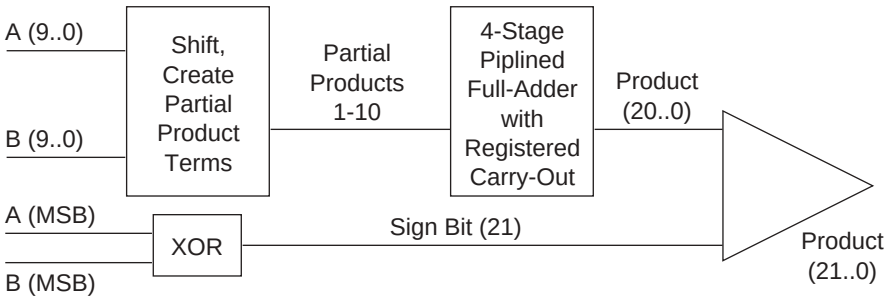
Results

The results from the Lattice ispLEVER™ software are given in Table 1 for the multiplier applications.

Table 1. Implementation Results for Lattice and Altera

Parameter	Lattice ispLSI 5512V	Altera EPM7512AE
Logic Cells	443/512	543/512
Resource Utilization	87%	>100%
I/Os	42	No Fit
Delay for Sign Bit (tpd)	12ns	No Fit
Clock to Out (tco)	7.0ns	No Fit
Frequency	105.3MHz	No Fit

Figure 2. Sample Multiplier Block Diagram



Competitive Analysis

The same challenges associated with implementing an 11-bit pipelined multiplier with a carry lookahead in a Lattice ispLSI 5512VE-80LF256 also exist for an Altera CPLD, EPM7512AEFC256-7. The Altera device has 512 macrocells and is a part of the 7000 family. The results of MAX+ Fitter v 9.01 are provided in Table 1.

Analysis of the results shows that the 11 by 11 multiplier will not fit in an Altera CPLD because the number of logic cells needed (543) exceeds the available logic cells (512). The results show that Lattice CPLDs are a clear winner in all operating parameters.

Conclusion

Using a CPLD for hardware multiplication in the DSP area provides flexibility and required performance.

The results indicate that the Lattice SuperWIDE™ ispLSI 5000VE family architecture is suitable for hardware multiplication. An 11 by 11 signed multiplier fits in an ispLSI 5512VE device with operating frequency of 105.3MHz.