Single Event Upset (SEU) Report for CrossLink-NX

Technical Note

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Acronyms in This Document

A list of acronyms used in this document.

Acronym	Definition
CRAM	Configuration RAM
EBR	Embedded Block RAM
ECC	Error Correction Codes
FIT	Failures-in-Time
FPGA	Field-Programmable Gate Array
IP	Intellectual Property
SEC	Soft Error Correction
SED	Soft Error Detect
SEFI	Single Event Functional Interrupt
SER	Soft Error Rate
SEU	Single Event Upset
SRAM	Static Random Access Memory

1. Introduction

This document discusses Single Event Upsets (SEUs), a radiation effect that may be observed during normal operation for Lattice Semiconductor CrossLink-NX™ FPGA. SEUs, often referred to as Soft Errors, occur when energetic particles interact with memory components, causing what is observed as a random bit flip.

SRAM is susceptible to SEU and requires characterization according to the JEDEC JESD89 set of standards. Lattice FPGAs typically use SRAM memory in two applications: the Logic Configuration RAM (Config; CRAM) and the User Memory (Embedded Block RAM; EBR).

This document provides Lattice's SEU characterization data for the above-mentioned FPGA families and types of memories, which can be used for estimating failure rates due to radiation effects.

Additionally, Lattice's FPGA architecture allows for significant failure derating, primarily due to unused routing resources within designs. Because of these redundant circuits, not all memory bits directly influence design functionality; those that do are known as *critical bits*. Derating guidelines based on critical bit analysis are provided for assessing the Single Event Functional Interrupt (SEFI) rate that is observed during field usage.

Finally, mitigation strategies offered by Lattice for handling SEUs are discussed.

2. Soft Error Rate Data for CrossLink-NX FPGA

Table 2.1 summarizes the SEU data collected for Lattice's 28 nm FD-SOI process used for the CrossLink-NX. The Soft Error Rate (SER) is represented in FIT, meaning the number of upset bits (failures) per billion device-hours. This rate is further normalized to FIT/Mbit of memory to allow for scaling across different devices with varying amounts of memory.

The data is divided by radiation and memory type to allow for use-case customization:

- Radiation Type
  - Neutron – Naturally occurring atmospheric neutrons are able to cause SEU. Results are scaled to the industry standard flux of NYC Sea-level (14 n/cm2/hr), and can be further scaled based on latitude, longitude, and altitude.
  - Alpha – Device packaging impurities may produce alpha particles as a decay product, which are able to cause SEU. Results are scaled for Ultra-Low Alpha mold compound flux (0.001 a/cm2/hr), and are considered use-case independent.
- SRAM Type
  - Config – Logic configuration memory for controlling FPGA function.
  - EBR – Embedded user memory.

Table 2.1. SEU Data for 28 nm FD-SOI FPGA

Technology	Radiation Type	SRAM Type	SER (FIT/Mbit)
28FDSOI 28 nm	Neutron –LP Mode	Config	2.7
		EBR	6.9
	Alpha – LP Mode	Config	0.4
		EBR	3.35
	Neutron –HP Mode	Config	3.4
		EBR	6.9
	Alpha – HP Mode	Config	0.8
		EBR	3.35

3. Functional Interrupt Rate

Understanding the field impact of SEU is critical for assessing risk and implementing mitigation strategies. The architecture of Lattice FPGAs allows for derating of the above upset rates:

- Config
  - User logic designs implemented on Lattice FPGAs rely on a small fraction of *critical bits* in the Config memory in order to continue operating properly. A sample of customer design is used to derive typical and worst-case critical bit ratios for assessing the risk of functional failure.
- EBR
  - Lattice FPGAs allow for the implementation of Error Correction Codes (ECC) into the user memory, which can detect and correct flipped bits, eliminating the functional impact of EBR SEU.

Combining these principles allow calculation of the expected field failure rate due to SEU, the SEFI Rate. Table 3.1 shows an example for the CrossLink-NX family.

Table 3.1. SEFI Rate by Device Density

Device	Config Memory Size (Mbit)	Typical[1] SEFI Rate (FIT)	Worst-Case[2] SEFI Rate (FIT)
LIFCL-40 LP Mode	6.237	3.9	6.8
LIFCL-40 HP Mode		5.2	9.2
LIFCL-17 LP Mode	TBD	TBD	TBD
LIFCL-17 HP Mode		TBD	TBD

Notes:

1. Typical designs range from 50-70% LUT Utilization based on sample benchmark designs.
2. Worst-Case designs range from 70-90% LUT Utilization based on sample benchmark designs.

4. Customer Down-Time Calculation

You can enable SED function to detect soft error events. SED scan happens in the background mode and the duration is variable but does not impact normal device functionality until SED error is detected. Once SED error is detected, CrossLink-NX device has the feature to auto correct single bit error within a frame via SEC feature. In addition to having an extremely low SEFI rate the SEC feature of the CrossLink-NX device made these devices virtually immune to single event upsets due to Alpha and Neutron particles.

5. Soft Error Event and Repair Sequences

For technical details SED and SEC features, refer to documents in the References section.

References

CrossLink-NX Soft Error Detection (SED)/Correction (SEC) Usage Guide (FPGA-TN-02076)

Technical Support Assistance

Submit a technical support case through www.latticesemi.com/techsupport.

Revision History

Revision 1.0, December 2019

Section	Change Summary
All	Initial release

www.latticesemi.com