Introduction

This document describes how to meet board timing requirements for DDR signals. The Lattice DDR SDRAM Controller IP core, non-pipelined version (DDR-NP) is used as an example.

Figure 17-1 describes the timing diagram for the DDR signals. A total of five clocks are used in the DDR board design using the Lattice DDR IP core. The following is the clock description:

- **clk**: Input clock for PLL (max. frequency of 133MHz for DDR NP)
- **ddr_clk**: Output clock going to DDR (max. frequency of 133MHz for DDR NP)
- **ddr_clk_n**: Negated version of **ddr_clk**
- **pll_mclk (clkx)**: Same as **ddr_clk**, used inside the FPGA only.
- **pll_nclk (clk2x)**: A 266MHz clock for DDR NP, used inside the FPGA only.

*Figure 17-1. DDR Signal Timing Diagram*
As shown in Figure 17-1, input to PLL is CLK (133MHz for DDR NP). The PLL generates \( \text{pll} \_\text{mclk} \) (133MHz) and \( \text{pll} \_\text{nclk} \) (266MHz). The clocks \( \text{ddr} \_\text{clk} \) and \( \text{ddr} \_\text{clk} \_\text{n} \) go to DDR memory and are delayed by I/O pad delay with respect to \( \text{pll} \_\text{mclk} \). The clocks \( \text{pll} \_\text{mclk} \) and \( \text{pll} \_\text{nclk} \) are internal to the FPGA. Command and address signals are clocked by a negative edge of \( \text{pll} \_\text{mclk} \). The signal \( \text{dqs} \_\text{out} \) acts as a clock for DDR write and is generated by negative edge of \( \text{pll} \_\text{nclk} \). The signal \( \text{ddr} \_\text{dq} \_\text{out} \) is the DDR write data bus and generated by positive edge of \( \text{pll} \_\text{nclk} \). The flops \( \text{ddr} \_\text{dq} \_\text{out} \) latch the read data and are clocked by positive edge of \( \text{pll} \_\text{nclk} \).

**Read Operation**

Figure 17-2 shows the timing of the DDR read operation. Table 17-1 describes the timing arcs of the read operation.

*Figure 17-2. Read Timing Diagram*
### Table 17-1. Read Operation Timing Arcs

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Description</th>
<th>Example: DDR-NP on ORCA 4</th>
</tr>
</thead>
<tbody>
<tr>
<td>tCK</td>
<td>Clock period of ddr_clk</td>
<td>7.5ns</td>
</tr>
<tr>
<td>tDDR_CLK (max)</td>
<td>Delay from the CLK input of the FPGA to the ddr_clk pad including Feedback compensation (Clock Path Delay - Feedback Path).</td>
<td>2.47(^1)</td>
</tr>
<tr>
<td>tDDR_CLK (min)</td>
<td>Delay from the CLK input of the FPGA to the ddr_clk pad including Feedback compensation (Clock Path Delay - Feedback Path).</td>
<td>1.138(^1)</td>
</tr>
<tr>
<td>tBDC</td>
<td>Board delay of ddr_clk from FPGA to DRR SDRAM.</td>
<td>—</td>
</tr>
<tr>
<td>tAC(MAX)</td>
<td>Time from the rising edge of ddr_clk after which the data is available at DDR output pins (max.).</td>
<td>0.75ns</td>
</tr>
<tr>
<td>tAC(MIN)</td>
<td>Time from the rising edge of ddr_clk after which the data is available at DDR output pins (min.).</td>
<td>-0.75ns</td>
</tr>
<tr>
<td>tBDD</td>
<td>Board delay from DRR SDRAM data pad to the FPGA ddr_dq pad.</td>
<td>—</td>
</tr>
<tr>
<td>tPD</td>
<td>Propagation delay from FPGA input pad to the ddr_dq_in flip-flop input pin (Data Path Delay).</td>
<td>0.0ns(^1)</td>
</tr>
<tr>
<td>tFDS</td>
<td>Set-up time required by the ddr_dq_in flip-flop (INREG_SET).</td>
<td>3.195ns(^1)</td>
</tr>
<tr>
<td>tFDH</td>
<td>Hold time required by the ddr_dq_in flip-flop (INREG_HLD).</td>
<td>-1.609ns(^1)</td>
</tr>
<tr>
<td>tSKEW</td>
<td>Skew of the PLL.</td>
<td>0.3ns</td>
</tr>
<tr>
<td>tFPGA_CLK (max)</td>
<td>Delay from the CLK input of the FPGA to the ddr_dq_in flip-flop clock input including feedback compensation (Clock Out Path Delay - Feedback Path).</td>
<td>2.935ns(^1)</td>
</tr>
<tr>
<td>tFPGA_CLK (min)</td>
<td>Delay from the CLK input of the FPGA to the ddr_dq_in flip-flop clock input including feedback compensation (Clock Out Path Delay - Feedback Path).</td>
<td>1.239ns(^1)</td>
</tr>
</tbody>
</table>

1. \(t_FPGA_{\text{CLK}}, t_{\text{DDR_CLK}}, t_{\text{PD}} \) and \(t_{\text{FDS}}\) can be easily obtained from the PNR time reports.

### Set-up Time Calculation for the Data Input (Max. Case)

The DDR Controller IP core uses the positive edge of pll_nclk to latch in the data.

Table 17-1 timing arcs are used to calculate the following:

Max. delay of clock to ddr_dq_in flops = \(t_{\text{FPGA_CLK}} \times \text{max} + (t_{\text{CK}} \times 1/2) - t_{\text{SKEW}} - t_{\text{FDS}}\)

Max. delay of DDR read data to ddr_dq_in flops = \(t_{\text{DDR_CLK}} \times \text{max} + t_{\text{BDC}} + t_{\text{AC}} \times \text{max} + t_{\text{BDD}} + t_{\text{PD}}\)

To meet set-up time at ddr_dq_in flops, Clock Delay - Data Delay > 0

Therefore:

\[t_{\text{FPGA_CLK}} \times \text{max} + (t_{\text{CK}} \times 1/2) - t_{\text{SKEW}} - t_{\text{FDS}} - t_{\text{DDR_CLK}} \times \text{max} - t_{\text{BDC}} - t_{\text{AC}} \times \text{max} - t_{\text{BDD}} - t_{\text{PD}} > 0\]

Isolating the board delays, we get:

\[(t_{\text{BDD}} + t_{\text{BDC}}) < t_{\text{FPGA_CLK}} \times \text{max} + (t_{\text{CK}} \times 1/2) - t_{\text{SKEW}} - t_{\text{FDS}} - t_{\text{DDR_CLK}} \times \text{max} - t_{\text{AC}} \times \text{max} - t_{\text{PD}}\]

\[(t_{\text{BDD}} + t_{\text{BDC}}) < 3.75 - 0.3 - 3.195 - 2.47 + 2.935 - 0.75 - 0.0\]

\[(t_{\text{BDD}} + t_{\text{BDC}}) < -0.03 \text{ ns}\]

### Hold Time Calculation for the Data Input (Min. Case)

As shown in Figure 17-2, the min data is available at DDR output pins after \(t_{\text{AC}} \times \text{min}\) time from the rising edge of ddr_clk. Since \(t_{\text{AC}} \times \text{min}\) is generally a negative number, data appears before the rising edge. This data will incur board delay \(t_{\text{BDD}}\) and propagation delay from FPGA input pad to the flip-flop input pin \(t_{\text{PD}}\).

Min. Delay of DDR read Data = \(t_{\text{DDR_CLK}} \times \text{min} + t_{\text{BDC}} + t_{\text{AC}} \times \text{min} + t_{\text{BDD}} + t_{\text{PD}}\)
Min. Delay of Clock to \( ddr\_dq\_in \) flops = \( t_{\text{FPGA_CLK}} \) (min) + \( t_{\text{SKEW}} \) + \( t_{\text{FDH}} \)

To meet hold time at \( ddr\_dq\_in \) flops, Data Delay - Clock Delay > 0

Therefore:

\[ t_{\text{DDR_CLK}} \text{(min)} + t_{\text{BDC}} + t_{\text{AC}} \text{(min)} + t_{\text{BDD}} + t_{\text{PD}} - t_{\text{FPGA_CLK}} \text{(min)} - t_{\text{SKEW}} - t_{\text{FDH}} > 0 \]

Isolating the board delays, we get:

\( (t_{\text{BDD}} + t_{\text{BDC}}) > t_{\text{FPGA_CLK}} \text{(min)} + t_{\text{SKEW}} + t_{\text{FDH}} - t_{\text{DDR_CLK}} \text{(min)} - t_{\text{AC}} \text{(min)} - t_{\text{PD}} \)

\( (t_{\text{BDD}} + t_{\text{BDC}}) > (1.239) \text{ ns} + 0.3 + (-1.609) \text{ ns} - (1.138) \text{ ns} - (-0.75) \text{ ns} - 0 \)

\( (t_{\text{BDD}} + t_{\text{BDC}}) > -0.458 \text{ ns} \)

Conclusion: To meet read set-up and hold timing, board delay for \( ddr\_dq\), \( ddr\_clk \) and \( ddr\_clk\_n \) should be:

\(-0.458 \text{ ns} < (t_{\text{BDD}} + t_{\text{BDC}}) < -0.03 \text{ ns}\)

Write Operation

For a proper write operation, data (\( ddr\_dq \)) should meet set-up (\( t_{DS} \)) and hold (\( t_{DH} \)) time requirements of DDR SDRAM with respect to \( ddr\_dqs \) signal. The \( ddr\_dqs \) signal is generated with respect to negative edge of \( pll\_nclk \) and data \( ddr\_dq \) out is generated with respect to positive edge of \( pll\_nclk \) as shown in Figure 17-3. As a result, 1/2 \( clk2x \) (3.75ns/2) is provided as set-up and hold for \( ddr\_dq\_out \) with respect to \( dqs\_out \).

For maximum set-up and hold margin, the \( ddr\_dqs \) and \( ddr\_dq \) traces on the board should be matched.

Table 17-2. Write Operation Timing Arcs

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Description</th>
<th>ORCA 4</th>
</tr>
</thead>
<tbody>
<tr>
<td>( t_{DS} )</td>
<td>Set-up time required by the DQ with respect to DQS for DDR SDRAM.</td>
<td>0.75ns</td>
</tr>
<tr>
<td>( t_{DH} )</td>
<td>Hold time required by the DQ with respect to DQS for DDR SDRAM.</td>
<td>0.75 ns</td>
</tr>
<tr>
<td>( t_{CDQ} )</td>
<td>Clock-to-out timing for ( ddr_dq ) with respect to ( pll_nclk ).</td>
<td>—</td>
</tr>
<tr>
<td>( t_{CDQS} )</td>
<td>Clock-to-out timing for ( ddr_dqs ) with respect to ( pll_nclk ).</td>
<td>—</td>
</tr>
<tr>
<td>( t_{BDDS} )</td>
<td>Board delay of ( ddr_dqs ) from FPGA to DDR SDRAM pins.</td>
<td>—</td>
</tr>
</tbody>
</table>

Figure 17-3. Write Timing Diagram

Write Set-up

\[ \text{Clock Delay} = t_{\text{CDQS}} + \frac{1}{2} \text{ clk2x} - t_{DS} + t_{\text{BDDS}} \]

\[ \text{Data Delay} = t_{\text{CDQ}} + t_{\text{BDD}} \]
Clock Delay - Data Delay > 0
Therefore:
\[ t_{CDQS} + \frac{1}{2} \text{clk2x} \cdot t_{DS} + t_{BDDS} \cdot t_{CDQ} - t_{BDD} > 0 \]

Assumptions for write set-up and hold equations:
1. \( t_{BDDS} \) and \( t_{BDD} \) are equal (board delays are same both for \( \text{dqs\_out} \) and \( \text{ddr\_dq\_out} \)).
2. \( t_{CDQ} \) and \( t_{CDQS} \) are equal (both are output delays from I/O flop).
Therefore:
\[ \frac{1}{2} \text{clk2x} - t_{DS} > 0 \]
\[ 3.75/2 - 0.75 > 0 \]
\[ 1.125 > 0 \]

**Write Hold**
Data Delay = \( t_{CDQ} + t_{BDD} \)
Clock Delay = \( t_{CDQS} + \frac{1}{2} \text{clk2x} + t_{DH} + t_{BDDS} \)
Data Delay - Clock Delay > 0
Therefore:
\[ t_{CDQS} + \frac{1}{2} \text{clk2x} \cdot t_{DH} + t_{BDDS} \cdot t_{CDQ} - t_{BDD} > 0 \]

Assumptions for write set-up and hold equations:
1. \( t_{BDDS} \) and \( t_{BDD} \) are equal (board delays are same both for \( \text{dqs\_out} \) and \( \text{ddr\_dq\_out} \)).
2. \( t_{CDQ} \) and \( t_{CDQS} \) are equal (both are output delays from I/O flop).
Therefore:
\[ \frac{1}{2} \text{clk2x} - t_{DH} > 0 \]
\[ 3.75/2 - 0.75 > 0 \]
\[ 1.125 > 0 \]

**Address and Command Signals**
Address (\( \text{ddr\_ad} \)) and command signals (\( \text{ddr\_cas}, \text{ddr\_ras}, \text{ddr\_we} \)) should meet set-up (\( t_{DS} \)) and hold (\( t_{DH} \)) timings at DDR interface with respect to positive edge of \( \text{ddr\_clk} \). Address and command signals are clocked using negative edge of \( \text{pll\_mclk} \) inside the FPGA as shown below. The \( \text{ddr\_clk} \) signal is a delayed by pad delay and board delay at DDR interface compared to \( \text{pll\_mclk} \) inside the FPGA. As a result, \( \frac{1}{2}\text{clkx} \) of set-up and hold is provided by design.
Table 17-3. Timing Arcs for Address and Command Signals

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Description</th>
<th>ORCA4</th>
</tr>
</thead>
<tbody>
<tr>
<td>t_{CCTRL} (max)</td>
<td>Is the clock-to-out time for ddr_ad and command signals. ( (\text{Clock Path Delay} - \text{Feedback Path}) + \text{Data Path Delay} )</td>
<td>4.834 ns</td>
</tr>
<tr>
<td>t_{CCTRL} (min)</td>
<td>Is the clock-to-out time for ddr_ad and command signals. ( (\text{Clock Path Delay} - \text{Feedback Path}) + \text{Data Path Delay} )</td>
<td>2.147 ns</td>
</tr>
<tr>
<td>t_{BDCTRL}</td>
<td>Is the board delay of ddr_ad and command signals from FPGA pins to DDR SDRAM pins.</td>
<td>—</td>
</tr>
</tbody>
</table>

Figure 17-4. Timing Diagram for Address and Command Signals

Set-up Calculation

Max Delay of Clock to DDR = \( t_{DDR,CLK} \) (max) + \( t_{BDC} \) + \( t_{CK} \) * 1/2 - \( t_{SKEW} \) - \( t_{DS} \)

Max Delays of command signals Data to DDR = \( t_{CCTRL} \) (max) + \( t_{BDCTRL} \)

To meet set up time at DDR memory, Clock Delay - Data Delay > 0

Therefore:

\[ t_{DDR,CLK} \) (max) + \( t_{BDC} \) + \( t_{CK} \) * 1/2 - \( t_{SKEW} \) - \( t_{DS} \) - \( t_{CCTRL} \) (max) - \( t_{BDCTRL} \) > 0 \]

Isolating the board delays, we get:

\[ t_{BDCTRL} - \( t_{BDC} \) < t_{DDR,CLK} \) (max) + \( t_{CK} \) * 1/2 - \( t_{SKEW} \) - \( t_{DS} \) - \( t_{CCTRL} \) (max) \]

\[ t_{BDCTRL} - \( t_{BDC} \) < 2.47 + 3.75 - 0.3 - 0.75 - 4.834 \]

\[ t_{BDCTRL} - \( t_{BDC} \) < 0.336 \text{ ns} \]
Hold Calculation

Min Delay of command signals Data to DDR = \( t_{CCTRL} \) (min) + \( t_{BDCTRL} \) + \( t_{CK} \times 1/2 \)

Min Delay of Clock to DDR = \( t_{DDR\_CLK} \) (min) + \( t_{BDC} \) + \( t_{SKEW} \) + \( t_{DH} \)

To meet hold time at DDR memory, Data Delay - Clock Delay > 0

Therefore:

\[ t_{CCTRL} \) (min) + \( t_{BDCTRL} \) + \( t_{CK} \times 1/2 \) - \( t_{DDR\_CLK} \) (min) - \( t_{BDC} \) - \( t_{SKEW} \) - \( t_{DH} \) > 0 \]

Isolating the board delays, we get:

\[ t_{BDCTRL} - t_{BDC} > - t_{CCTRL} \) (min) - \( t_{CK} \times 1/2 + t_{DDR\_CLK} \) (min) - \( t_{SKEW} \) + \( t_{DH} \) \]

\[ t_{BDCTRL} - t_{BDC} > -2.147 - 3.75 + (1.138) + 0.3 + 0.75 \]

\[ t_{BDCTRL} - t_{BDC} > -3.709 \]

\[ t_{BDCTRL} - t_{BDC} > -3.709 \text{ ns} \]

Conclusion: To meet set-up and hold timings of command signals, board delay of command signals \( ddr\_clk \) and \( ddr\_clk\_n \) should be:

\[-3.709 \text{ ns} < (t_{BDCTRL} - t_{BDC}) < 0.336 \text{ ns} \]

Board Design Guidelines

- The \( ddr\_clk \) and \( ddr\_clk\_n \) pads should be placed adjacent to each other in the FPGA to get similar internal FPGA delays.

- The \( ddr\_clk \) and \( ddr\_clk\_n \) trace delays on the board should be matched.

- The DQ trace delays can be calculated using the following formula, for memory reads:

\[ t_{SKEW} + t_{FDH} - t_{AC} \) (min) - \( t_{PD} - t_{DDR\_CLK} + t_{FPGA\_CLK} < (t_{BDD} + t_{BDC}) < (t_{CK} \times 1/2) - t_{SKEW} - t_{FDS} - t_{AC} \) (max) - \( t_{PD} - t_{DDR\_CLK} + t_{FPGA\_CLK} \]

- The DQ and DQS trace lengths should be balanced and matching to get maximum set-up/hold time during memory writes.

- The address and control signals for the DDR SDRAM are generated on the negative edge of the FPGA clock. The trace lengths for address and control lines are calculated using following equation:

\[-t_{CCTRL} - t_{CK} \times 1/2 + t_{DDR\_CLK} + t_{SKEW} + t_{DH} < (t_{BDCTRL} - t_{BDC}) < t_{DDR\_CLK} + t_{CK} \times 1/2 - t_{SKEW} - t_{DS} - t_{CCTRL} + t_{BDC} \]

- As shown in Figure 17-1, both FPGA internal clock and \( ddr\_clk \) are generated by a single PLL. It may be difficult to meet read data Set-up and hold timing with a single PLL. As shown in Figure 17-5, a two-PLL clocking scheme is proposed to meet read data set-up and hold timing. Adjusting feedback delay of PLL2 can control delay of \( pll\_mclk \). Increasing delay on \( pll\_mclk \) can increase the read set-up margin but it also decreases the hold margin. To get better timing, skew between \( ddr\_clk \) and \( pll\_mclk \) has to be minimized.
Figure 17-5. Two PLL Clocking Scheme

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+1-503-268-8001 (Outside North America)
e-mail: techsupport@latticesemi.com
Internet: www.latticesemi.com

Revision History

<table>
<thead>
<tr>
<th>Date</th>
<th>Version</th>
<th>Change Summary</th>
</tr>
</thead>
<tbody>
<tr>
<td>—</td>
<td>—</td>
<td>Previous Lattice releases.</td>
</tr>
<tr>
<td>September 2012</td>
<td>01.1</td>
<td>Updated document with new corporate logo.</td>
</tr>
</tbody>
</table>
Appendix A. Example Extractions of Delays from Timing Reports

From the Set-up Report below, which was run for MAX conditions:

- $t_{PD} = 0.0$ ns
- $t_{FDS} = 3.195$ ns
- $t_{FPGA_CLK} (max) = 6.206 - 3.271 = 2.935$ ns

===============================================================
Preference: INPUT_SETUP PORT "ddr_dq_*" 2.000000 ns CLKNET "pll_nclk" ;
32 items scored, 0 timing errors detected.

Passed: The following path meets requirements by 1.740ns

Logical Details: Cell type Pin type Cell name (clock net +/-)
Source: Port Pad ddr_dq_23
Destination: O-FF In Data in U1_ddrctl_np_o4_1_008/U3_databusif/ddr_dqoeZ0Z_23 (to pll_nclk +)

Data Path Delay: 0.000ns (0.0% logic, 0.0% route), 0 logic levels.
Clock Path Delay: 6.206ns (29.3% logic, 70.7% route), 2 logic levels.

Constraint Details:

0.000ns delay ddr_dq_23 to ddr_dq_23 less
2.000ns offset ddr_dq_23 to clk (totaling -2.000ns) meets
6.206ns delay clk to ddr_dq_23 less
3.271ns feedback compensation less
3.195ns INREG_SET requirement (totaling -0.260ns) by 1.740ns

Physical Path Details:

Data path ddr_dq_23 to ddr_dq_23:

Name Fanout Delay (ns) Site Resource
-------- ------- --------- ------------
       0.000 (0.0% logic, 0.0% route), 0 logic levels.

Clock path clk to ddr_dq_23:

Name Fanout Delay (ns) Site Resource
------- ------- --------- ------------
IN_DEL --- 1.431 AB4.PAD to AB4.INCK clk
ROUTE 1 0.816 AB4.INCK to LLHPLL.CLKIN clk_c
NCLK_DEL --- 0.385 LLHPLL.CLKIN to LLHPLL.NCLK U2_ddr_pll_orca/ddr_pll_0_0
ROUTE 136 3.574 LLHPLL.NCLK to N24.SC pll_nclk
-------- ------- --------- ------------
       6.206 (29.3% logic, 70.7% route), 2 logic levels.
Feedback path:

<table>
<thead>
<tr>
<th>Name</th>
<th>Fanout</th>
<th>Delay (ns)</th>
<th>Site</th>
<th>Resource</th>
</tr>
</thead>
<tbody>
<tr>
<td>NCLK_DEL</td>
<td>---</td>
<td>0.385</td>
<td>LLHPPLL.CLKIN to LLHPPLL.NCLK</td>
<td>U2_ddr_pll_orca/ddr_pll_0_0</td>
</tr>
<tr>
<td>ROUTE</td>
<td>136</td>
<td>2.886</td>
<td>LLHPPLL.NCLK to LLHPPLL.FB</td>
<td>pll_nclk</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>---</td>
</tr>
<tr>
<td></td>
<td></td>
<td>3.271</td>
<td></td>
<td>(11.8% logic, 88.2% route), 1 logic levels.</td>
</tr>
</tbody>
</table>

Report: 0.260ns is the minimum offset for this preference.

From the Hold Report below, which was run for MIN conditions:

- \( t_{PD} = 0.0 \) ns
- \( t_{FDH} = -1.609 \) ns
- \( t_{FPGA\_CLK\ (min)} = 3.144 - 1.905 = 1.239 \) ns

=====================================================================================================
Preference: INPUT_SETUP PORT "ddr_dq_*" 2.000000 ns CLKNET "pll_nclk" ;
32 items scored, 0 timing errors detected.
=====================================================================================================

Passed: The following path meets requirements by 0.370ns

Logical Details: Cell type Pin type Cell name (clock net +/-)

Source: Port Pad ddr_dq_31
Destination: IO-FF In Data in Ul_ddrcnt_npi_e41_008/U3_databusif/ddr_dqoeZ0Z_31
(to pll_nclk +)

Data Path Delay: 0.000ns (0.0% logic, 0.0% route), 0 logic levels.

Clock Path Delay: 3.144ns (25.7% logic, 74.3% route), 2 logic levels.

Constraint Details:

- 0.000ns delay ddr_dq_31 to ddr_dq_31 plus
- 0.000ns hold offset ddr_dq_31 to clk (totaling 0.000ns) meets
- 3.144ns delay clk to ddr_dq_31 plus
- 1.905ns feedback compensation less
- \(-1.609\)ns INREG_HLD requirement (totaling \(-0.370\)ns) by 0.370ns

Physical Path Details:

Data path ddr_dq_31 to ddr_dq_31:

<table>
<thead>
<tr>
<th>Name</th>
<th>Fanout</th>
<th>Delay (ns)</th>
<th>Site</th>
<th>Resource</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>0.000</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>(0.0% logic, 0.0% route), 0 logic levels.</td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>
### Clock path clk to ddr_dq_31:

<table>
<thead>
<tr>
<th>Name</th>
<th>Fanout</th>
<th>Delay (ns)</th>
<th>Site</th>
<th>Resource</th>
</tr>
</thead>
<tbody>
<tr>
<td>IN_DEL</td>
<td>---</td>
<td>0.576</td>
<td>AB4.PAD to AB4.INCK clk</td>
<td></td>
</tr>
<tr>
<td>ROUTE</td>
<td>1</td>
<td>0.507</td>
<td>AB4.INCK to LLHPPLL.CLKIN clk</td>
<td></td>
</tr>
<tr>
<td>NCLK_DEL</td>
<td>---</td>
<td>0.231</td>
<td>LLHPPLL.CLKIN to LLHPPLL.NCLK</td>
<td>U2_ddr_pll_orca/ddr_pll_0_0</td>
</tr>
<tr>
<td>ROUTE</td>
<td>136</td>
<td>1.830</td>
<td>LLHPPLL.NCLK to C25.SC pll_nclk</td>
<td></td>
</tr>
</tbody>
</table>

--------

3.144  (25.7% logic, 74.3% route), 2 logic levels.

### Feedback path:

<table>
<thead>
<tr>
<th>Name</th>
<th>Fanout</th>
<th>Delay (ns)</th>
<th>Site</th>
<th>Resource</th>
</tr>
</thead>
<tbody>
<tr>
<td>NCLK_DEL</td>
<td>---</td>
<td>0.231</td>
<td>LLHPPLL.CLKIN to LLHPPLL.NCLK</td>
<td>U2_ddr_pll_orca/ddr_pll_0_0</td>
</tr>
<tr>
<td>ROUTE</td>
<td>136</td>
<td>1.674</td>
<td>LLHPPLL.NCLK to LLHPPLL.FB pll</td>
<td>pll_nclk</td>
</tr>
</tbody>
</table>

--------

1.905  (12.1% logic, 87.9% route), 1 logic levels.

Report: There is no minimum offset greater than zero for this preference.

### From the Set-up Report below, which was run for MAX conditions:

- \( t_{DDR\_CLK (max)} = 5.741 - 3.271 = 2.47 \text{ ns} \)

===========================================================================
Preference: CLOCK_TO_OUT PORT "ddr_cas_n" MAX 5.500000 ns CLKPORT "clk" CLKOUT PORT "ddr_clk"
;
1 item scored, 0 timing errors detected.
===========================================================================

Passed: The following path meets requirements by 3.182ns

Logical Details: Cell type Pin type Cell name (clock net +/-)

Source: Unknown Q U1_ddrct_np_o4_1_008/U1_cmdexe/ddr_cas_n20 (from ddr_clk_c -)

Destination: Port Pad ddr_cas_n

Data Path Delay: 1.713ns (100.0% logic, 0.0% route), 1 logic levels.

Clock Path Delay: 6.346ns (28.6% logic, 71.4% route), 2 logic levels.

Constraint Details:

6.346ns delay clk to ddr_cas_n less
3.271ns feedback compensation
1.713ns delay ddr_cas_n to ddr_cas_n less
2.470ns delay clk to ddr_clk (totaling 2.318ns) meets
5.50ns offset clk to ddr_cas_n by 3.182ns

Physical Path Details:

Clock path clk to ddr_cas_n:
### Name    Fanout   Delay (ns)          Site               Resource

<p>| | | | |</p>
<table>
<thead>
<tr>
<th></th>
<th></th>
<th></th>
<th></th>
</tr>
</thead>
<tbody>
<tr>
<td>IN_DEL</td>
<td>---</td>
<td>1.431</td>
<td>AB4.PAD to</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>AB4.INCK clk</td>
</tr>
<tr>
<td>ROUTE</td>
<td>1</td>
<td>0.816</td>
<td>AB4.INCK to</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>LLHPPLL.CLKIN clk_c</td>
</tr>
<tr>
<td>MCLK_DEL</td>
<td>---</td>
<td>0.385</td>
<td>LLHPPLL.CLKIN to</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>LLHPPLL.MCLK U2_ddr_pll_orca/ddr_pll_0_0</td>
</tr>
<tr>
<td>ROUTE</td>
<td>449</td>
<td>3.714</td>
<td>LLHPPLL.MCLK to</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>AE15.SC ddr_clk_c</td>
</tr>
</tbody>
</table>

**Summary:**

6.346 (28.6% logic, 71.4% route), 2 logic levels.

### Data path ddr_cas_n to ddr_cas_n:

<table>
<thead>
<tr>
<th>Name</th>
<th>Fanout</th>
<th>Delay (ns)</th>
<th>Site</th>
<th>Resource</th>
</tr>
</thead>
<tbody>
<tr>
<td>OUTREG_DEL</td>
<td>---</td>
<td>1.713</td>
<td>AE15.SC to</td>
<td>AE15.PAD ddr_cas_n (from ddr_clk_c)</td>
</tr>
</tbody>
</table>

**Summary:**

1.713 (100.0% logic, 0.0% route), 1 logic levels.

### Clock out path:

<table>
<thead>
<tr>
<th>Name</th>
<th>Fanout</th>
<th>Delay (ns)</th>
<th>Site</th>
<th>Resource</th>
</tr>
</thead>
<tbody>
<tr>
<td>IN_DEL</td>
<td>---</td>
<td>1.431</td>
<td>AB4.PAD to</td>
<td>AB4.INCK clk</td>
</tr>
<tr>
<td>ROUTE</td>
<td>1</td>
<td>0.816</td>
<td>AB4.INCK to</td>
<td>LLHPPLL.CLKIN clk_c</td>
</tr>
<tr>
<td>MCLK_DEL</td>
<td>---</td>
<td>0.385</td>
<td>LLHPPLL.CLKIN to</td>
<td>LLHPPLL.MCLK U2_ddr_pll_orca/ddr_pll_0_0</td>
</tr>
<tr>
<td>ROUTE</td>
<td>449</td>
<td>1.191</td>
<td>LLHPPLL.MCLK to</td>
<td>AF3.OUTDD ddr_clk_c</td>
</tr>
<tr>
<td>OUTDD_DEL</td>
<td>---</td>
<td>1.918</td>
<td>AF3.OUTDD to</td>
<td>AF3.PAD ddr_clk</td>
</tr>
</tbody>
</table>

**Summary:**

5.741 (65.0% logic, 35.0% route), 3 logic levels.

### Feedback path:

<table>
<thead>
<tr>
<th>Name</th>
<th>Fanout</th>
<th>Delay (ns)</th>
<th>Site</th>
<th>Resource</th>
</tr>
</thead>
<tbody>
<tr>
<td>NCLK_DEL</td>
<td>---</td>
<td>0.385</td>
<td>LLHPPLL.CLKIN to</td>
<td>LLHPPLL.NCLK U2_ddr_pll_orca/ddr_pll_0_0</td>
</tr>
<tr>
<td>ROUTE</td>
<td>136</td>
<td>2.886</td>
<td>LLHPPLL.NCLK to</td>
<td>LLHPPLL.FB pll_nclk</td>
</tr>
</tbody>
</table>

**Summary:**

3.271 (11.8% logic, 88.2% route), 1 logic levels.

**Report:**

2.318ns is the minimum offset for this preference.

### From the Hold Report below, which was run for MIN conditions:

- $t_{DDR_CLK (min)} = 3.043 - 1.905 = 1.138$ ns

---

**Preference:**

```
Preference: CLOCK_TO_OUT PORT "ddr_cas_n" MAX 5.500000 ns CLKPORT "clk" CLKOUT PORT "ddr_clk"
```

1 item scored, 0 timing errors detected.

---

**Passed:**

The following path meets requirements by 1.056ns

**Logical Details:**

- **Source:** Unknown Q U1_ddrct_np_o4_1_008/U1_cmdexe/ddr_cas_n20 (from ddr_clk_c)
- **Destination:** Port Pad ddr_cas_n

---

17-12
Data Path Delay: 0.928ns (100.0% logic, 0.0% route), 1 logic levels.

Clock Path Delay: 3.171ns (25.4% logic, 74.6% route), 2 logic levels.

Constraint Details:

- 3.171ns delay clk to ddr_cas_n less
- 1.905ns feedback compensation
- 0.928ns delay ddr_cas_n to ddr_cas_n less
- 1.138ns delay clk to ddr_clk (totaling 1.056ns) meets
- 0.000ns hold offset clk to ddr_cas_n by 1.056ns

Physical Path Details:

Clock path clk to ddr_cas_n:

<table>
<thead>
<tr>
<th>Name</th>
<th>Fanout</th>
<th>Delay (ns)</th>
<th>Site</th>
<th>Resource</th>
</tr>
</thead>
<tbody>
<tr>
<td>IN_DEL</td>
<td>---</td>
<td>0.576</td>
<td>AB4.PAD to</td>
<td>AB4.INCK clk</td>
</tr>
<tr>
<td>ROUTE</td>
<td>1</td>
<td>0.507</td>
<td>AB4.INCK to</td>
<td>LLHPPLL.CLKIN clk_c</td>
</tr>
<tr>
<td>MCLK_DEL</td>
<td>---</td>
<td>0.231</td>
<td>LLHPPLL.CLKIN to</td>
<td>LLHPPLL.MCLK U2_ddr_pll_orca/ddr_pll_0_0</td>
</tr>
<tr>
<td>ROUTE</td>
<td>449</td>
<td>1.857</td>
<td>LLHPPLL.MCLK to</td>
<td>AE15.SC ddr_clk_c</td>
</tr>
</tbody>
</table>

3.171 (25.4% logic, 74.6% route), 2 logic levels.

Data path ddr_cas_n to ddr_cas_n:

<table>
<thead>
<tr>
<th>Name</th>
<th>Fanout</th>
<th>Delay (ns)</th>
<th>Site</th>
<th>Resource</th>
</tr>
</thead>
<tbody>
<tr>
<td>OUTREG_DEL</td>
<td>---</td>
<td>0.928</td>
<td>AE15.SC to</td>
<td>AE15.PAD ddr_cas_n (from ddr_clk_c)</td>
</tr>
</tbody>
</table>

0.928 (100.0% logic, 0.0% route), 1 logic levels.

Clock out path:

<table>
<thead>
<tr>
<th>Name</th>
<th>Fanout</th>
<th>Delay (ns)</th>
<th>Site</th>
<th>Resource</th>
</tr>
</thead>
<tbody>
<tr>
<td>IN_DEL</td>
<td>---</td>
<td>0.576</td>
<td>AB4.PAD to</td>
<td>AB4.INCK clk</td>
</tr>
<tr>
<td>ROUTE</td>
<td>1</td>
<td>0.507</td>
<td>AB4.INCK to</td>
<td>LLHPPLL.CLKIN clk_c</td>
</tr>
<tr>
<td>MCLK_DEL</td>
<td>---</td>
<td>0.231</td>
<td>LLHPPLL.CLKIN to</td>
<td>LLHPPLL.MCLK U2_ddr_pll_orca/ddr_pll_0_0</td>
</tr>
<tr>
<td>ROUTE</td>
<td>449</td>
<td>0.778</td>
<td>LLHPPLL.MCLK to</td>
<td>AF3.OUTDD ddr_clk_c</td>
</tr>
<tr>
<td>OUTDD_DEL</td>
<td>---</td>
<td>0.951</td>
<td>AF3.OUTDD to</td>
<td>AF3.PAD ddr_clk</td>
</tr>
</tbody>
</table>

3.043 (57.8% logic, 42.2% route), 3 logic levels.

Feedback path:

<table>
<thead>
<tr>
<th>Name</th>
<th>Fanout</th>
<th>Delay (ns)</th>
<th>Site</th>
<th>Resource</th>
</tr>
</thead>
<tbody>
<tr>
<td>NCLK_DEL</td>
<td>---</td>
<td>0.231</td>
<td>LLHPPLL.CLKIN to</td>
<td>LLHPPLL.NCLK U2_ddr_pll_orca/ddr_pll_0_0</td>
</tr>
<tr>
<td>ROUTE</td>
<td>136</td>
<td>1.674</td>
<td>LLHPPLL.NCLK to</td>
<td>LLHPPLL.FB pll_nclk</td>
</tr>
</tbody>
</table>

1.905 (12.1% logic, 87.9% route), 1 logic levels.

Report: 1.056ns is the maximum offset for this preference.

===========================================================================
From the Set-up Report below, which was run for MAX conditions. The report shown here is for ddr_ad.

- \( t_{\text{CCTRL}} \text{ (max)} = (6.392-3.271) + 1.713 = 4.834 \text{ ns} \)

Find delays similarly for ddr_ras_n, ddr_cas_n, ddr_we_n, ddr_ba, ddr_cs_n and ddr_cke signals. Then take the max of those delays as \( t_{\text{CCTRL}} \text{ (max)} \).

---

**Preference:** CLOCK_TO_OUT PORT "ddr_ad_*" 5.500000 ns CLKNET "ddr_clk_c" ;
12 items scored, 0 timing errors detected.

Passed: The following path meets requirements by 0.666ns

Logical Details: Cell type Pin type Cell name (clock net +/-)
Source: Unknown Q Ul_ddrct_np_o4_l_008/U1_cmdexe/ddr_adZ0Z_6 (from ddr_clk_c -)
Destination: Port Pad ddr_ad_6

**Data Path Delay:**  1.713ns (100.0% logic, 0.0% route), 1 logic levels.

**Clock Path Delay:**  6.392ns (28.4% logic, 71.6% route), 2 logic levels.

Constraint Details:
- 6.392ns delay clk to ddr_ad_6 less
- 3.271ns feedback compensation
- 1.713ns delay ddr_ad_6 to ddr_ad_6 (totaling 4.834ns) meets
- 5.500ns offset clk to ddr_ad_6 by 0.666ns

Physical Path Details:

**Clock path clk to ddr_ad_6:**

<table>
<thead>
<tr>
<th>Name</th>
<th>Fanout</th>
<th>Delay (ns)</th>
<th>Site</th>
<th>Resource</th>
</tr>
</thead>
<tbody>
<tr>
<td>IN_DEL</td>
<td>---</td>
<td>1.431</td>
<td>AB4.PAD to AB4.INCK clk</td>
<td></td>
</tr>
<tr>
<td>ROUTE</td>
<td>1</td>
<td>0.816</td>
<td>AB4.INCK to LLHPPLL.CLKIN clk_c</td>
<td></td>
</tr>
<tr>
<td>MCLK_DEL</td>
<td>---</td>
<td>0.385</td>
<td>LLHPPLL.CLKIN to LLHPPLL.MCLK U2_ddr_pll_orca/ddr_pll_0_0</td>
<td></td>
</tr>
<tr>
<td>ROUTE</td>
<td>449</td>
<td>3.760</td>
<td>LLHPPLL.MCLK to AE14.SC ddr_clk_c</td>
<td></td>
</tr>
</tbody>
</table>

--------

6.392 (28.4% logic, 71.6% route), 2 logic levels.

**Data path ddr_ad_6 to ddr_ad_6:**

<table>
<thead>
<tr>
<th>Name</th>
<th>Fanout</th>
<th>Delay (ns)</th>
<th>Site</th>
<th>Resource</th>
</tr>
</thead>
<tbody>
<tr>
<td>OUTREG_DEL</td>
<td>---</td>
<td>1.713</td>
<td>AE14.SC to AE14.PAD ddr_ad_6 (from ddr_clk_c)</td>
<td></td>
</tr>
</tbody>
</table>

--------

1.713 (100.0% logic, 0.0% route), 1 logic levels.

**Feedback path:**

<table>
<thead>
<tr>
<th>Name</th>
<th>Fanout</th>
<th>Delay (ns)</th>
<th>Site</th>
<th>Resource</th>
</tr>
</thead>
<tbody>
<tr>
<td>NCLK_DEL</td>
<td>---</td>
<td>0.385</td>
<td>LLHPPLL.CLKIN to LLHPPLL.NCLK U2_ddr_pll_orca/ddr_pll_0_0</td>
<td></td>
</tr>
<tr>
<td>ROUTE</td>
<td>136</td>
<td>2.886</td>
<td>LLHPPLL.NCLK to LLHPPLL.FB pll_nclk</td>
<td></td>
</tr>
</tbody>
</table>

--------

3.271 (11.8% logic, 88.2% route), 1 logic levels.

Report: 4.834ns is the minimum offset for this preference.
From the Hold Report below, which was run for MIN conditions. The report shown here is for ddr_ad* only.

\[ t_{CCTRL} \text{(min)} = (3.124-1.905) + 0.928 = 2.147 \text{ ns} \]

Find delays similarly for ddr_ras_n, ddr_cas_n, ddr_we_n, ddr_ba, ddr_cs_n and ddr_cke signals. Then take the min of those delays as \( t_{CCTRL} \text{(min)} \).

===========================================================================
Preference: CLOCK_TO_OUT PORT "ddr_ad_*" 5.500000 ns CLKNET "ddr_clk_c" ;
12 items scored, 0 timing errors detected.

Passed: The following path meets requirements by 2.147ns

Logical Details:  Cell type  Pin type  Cell name  (clock net +/-)
Source:         Unknown    Q  Ul_ddrct_np_o4_l_008/U1_cmdexe/ddr_adZ0Z_4  (from ddr_clk_c -)
Destination:    Port       Pad  ddr_ad_4

**Data Path Delay:**  0.928ns  (100.0% logic, 0.0% route), 1 logic levels.

**Clock Path Delay:**  3.124ns  (25.8% logic, 74.2% route), 2 logic levels.

Constraint Details:

3.124ns delay clk to ddr_ad_4 less
1.905ns feedback compensation
0.928ns delay ddr_ad_4 to ddr_ad_4 (totaling 2.147ns) meets
0.000ns hold offset clk to ddr_ad_4 by 2.147ns

Physical Path Details:

**Clock path clk to ddr_ad_4:**

Name  Fanout  Delay (ns)  Site  Resource
IN_DEL  ---  0.576  AB4.PAD to  AB4.INCK clk
ROUTE  1  0.507  AB4.INCK to  LLHPPLL.CLKIN clk_c
MCLK_DEL  ---  0.231  LLHPPLL.CLKIN to  LLHPPLL.MCLK U2_ddr_pll_orca/ddr_pll_0_0
ROUTE  449  1.810  LLHPPLL.MCLK to  T26.SC ddr_clk_c
--------
3.124  (25.8% logic, 74.2% route), 2 logic levels.

**Data path ddr_ad_4 to ddr_ad_4:**

Name  Fanout  Delay (ns)  Site  Resource
OUTREG_DEL  ---  0.928  T26.SC to  T26.PAD ddr_ad_4 (from ddr_clk_c)
--------
0.928  (100.0% logic, 0.0% route), 1 logic levels.

**Feedback path:**

Name  Fanout  Delay (ns)  Site  Resource
NCLK_DEL  ---  0.231  LLHPPLL.CLKIN to  LLHPPLL.NCLK U2_ddr_pll_orca/ddr_pll_0_0
ROUTE  136  1.674  LLHPPLL.NCLK to  LLHPPLL.FB pll_nclk
--------
1.905  (12.1% logic, 87.9% route), 1 logic levels.

Report:  2.220ns is the maximum offset for this preference.